## The RF Line **NPN Silicon** RF Power Transistor

Designed for 28 Volt microwave large–signal, common base, Class–C CW amplifier applications in the range 1600 – 1640 MHz.

- Specified 28 Volt, 1.6 GHz Class–C Characteristics Output Power = 30 Watts Minimum Gain = 7.5 dB, @ 30 Watts Minimum Efficiency = 40% @ 30 Watts
- Characterized with Series Equivalent Large–Signal Parameters from 1500 MHz to 1700 MHz
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

# **MRF16030**

30 WATTS, 1.6 GHz RF POWER TRANSISTOR NPN SILICON



#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	VCES	60	Vdc
Emitter-Base Voltage	VEBO	4.0	Vdc
Collector–Current	IC	4.0	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	PD	103 0.58	Watts °C/W
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

#### THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case (1) (2) $R_{\theta JC}$ 1.7°C/W

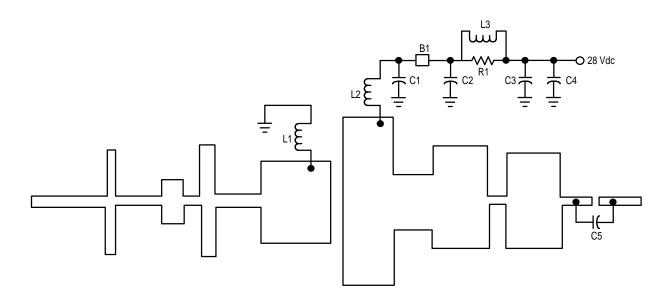
(1) Thermal measurement performed using CW RF operating condition.

(2) Thermal resistance is determined under specified RF operating conditions by infrared measurement techniques.



### **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted)

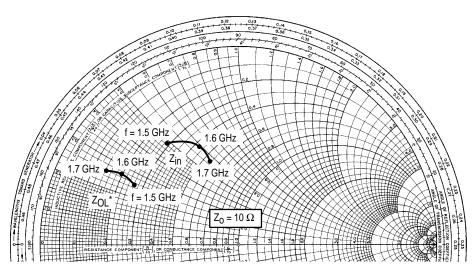
Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I <sub>C</sub> = 100 mAdc, V <sub>BE</sub> = 0)	V(BR)CES	55	_	_	Vdc
Collector–Base Breakdown Voltage ( $I_C = 100 \text{ mAdc}, I_E = 0$ )	V(BR)CBO	55	_	_	Vdc
Emitter–Base Breakdown Voltage ( $I_E = 10 \text{ mAdc}, I_C = 0$ )	V(BR)EBO	4.0	_	_	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 28 Vdc, V <sub>BE</sub> = 0)	ICES	_	_	10	mAdc
ON CHARACTERISTICS	· · ·			•	•
DC Current Gain (I <sub>CE</sub> = 1.0 Adc, V <sub>CE</sub> = 5.0 Vdc)	hFE	20	35	80	—
FUNCTIONAL TESTS				•	•
Collector–Base Amplifier Power Gain (V <sub>CC</sub> = 28 Vdc, P <sub>out</sub> = 30 Watts, f = 1600/1640 MHz)	G <sub>pe</sub>	7.5	7.7	_	dB
Collector Efficiency (V <sub>CC</sub> = 28 Vdc, P <sub>out</sub> = 30 Watts, f = 1600/1640 MHz)	η	40	45	_	%
Input Return Loss (V <sub>CC</sub> = 28 Vdc, P <sub>out</sub> = 30 Watts, f = 1600/1640 MHz)	I <sub>RL</sub>	8.0	_	_	dB
Output Mismatch Stress V <sub>CC</sub> = 28 Vdc, P <sub>out</sub> = 30 Watts, f = 1600 MHz, Load VSWR = 3:1, All phase angles at frequency of test	Ψ	No I	Degradation ir	Output Pow	/er



Board Material – Teflon<sup>®</sup> Glass Laminate Dielectric Thickness = 0.30",  $\epsilon_{\text{f}}$  = 2.55", 2.0 oz. Copper

B1	Fair Rite Bead on #24 Wire	C4	47 μF, 50 V, Electrolytic
C1, C5	100 pF, B Case, ATC Chip Cap	L1, L2	3 Turns, #18, 0.133" ID, 0.15" Long
C2	0.1 μF, Dipped Mica Cap	L3	9 Turns, #24 Enamel
C3	0.1 μF, Chip Cap	R1	82 Ω, 1.0 W, Carbon

#### Figure 1. MRF16030 Test Fixture Schematic



 $V_{CC}$  = 28 Vdc,  $P_{out}$  = 30 W

f MHz	Z <sub>in</sub> Ohms	Z <sub>OL</sub> * Ohms
1500	3.05 + j 4.88	2.66 + j 2.53
1600	4.32 + j 6.00	1.79 + j 2.80
1700	5.62 + j 5.79	1.51 + j 2.64

 $Z_{OL}^*$  = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.



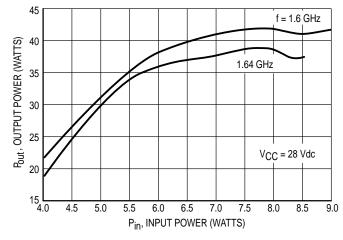
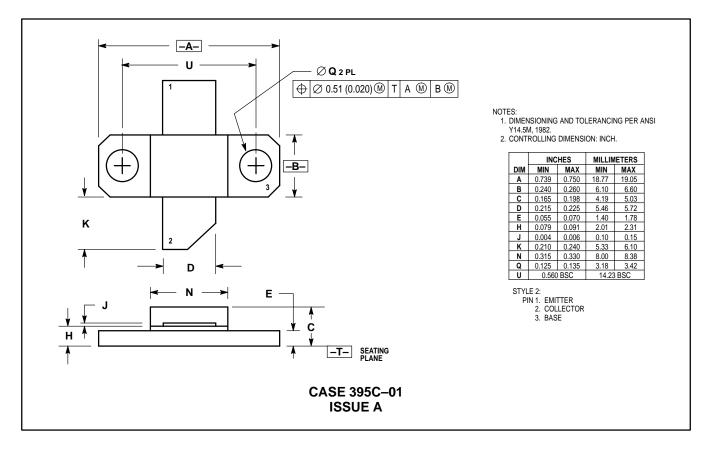


Figure 3. Output Power versus Input Power

#### PACKAGE DIMENSIONS



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