Advance Information

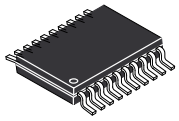
The MRFIC Line Quadrature Modulator

MRFIC0001

QUADRATURE MODULATOR INTEGRATED CIRCUIT

The MRFIC0001 is an integrated Quadrature Modulator designed for operation in the 50 to 260 MHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications include DQPSK for PDC, NADC, and PHS; GMSK for GSM and DCS1800; and QPSK for CATV.

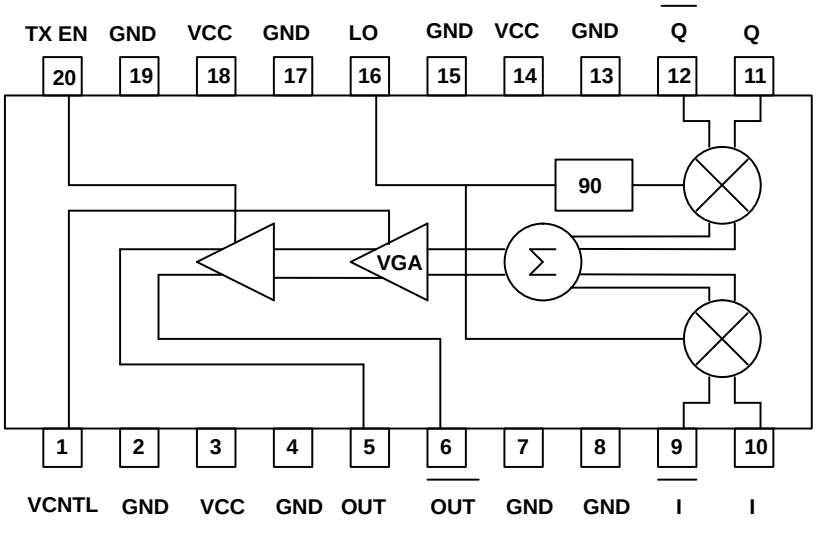
- Linear I/Q Ports
- On Chip LO Phase Shifter
- I/Q Phase Imbalance = 2 degrees (Typ)
- I/Q Amplitude Imbalance = 0.3 dB (Typ)
- Gain Control = 30 dB (Typ)
- Single Source Low Operating Supply Voltage
- Low Power Consumption
- Low–Cost, Low Profile Plastic TSSOP Package
- Order MRFIC0001R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M001



CASE 948D–03
(TSSOP–20)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.5	Vdc
Control Voltages	TX EN, VCNTL	6.5	Vdc
LO Input Power	P_{LO}	0.0	dBm
Differential I/Q Input Voltage	V_D	2.0	V_{pp}
I, $\bar{I}$, Q, and $\bar{Q}$ DC Bias Voltage	V_B	2.0	Vdc
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



Pin Connections and Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.7 to 5.5	Vdc
LO Input Power	P_{LO}	–10	dBm
LO Frequency	f_{LO}	50 to 260	MHz
Differential I/Q Input Voltage	V_D	0 to 1.0	Vdc
I, $\overline{I}$, Q, and $\overline{Q}$ DC Bias Voltage	V_B	1.5 to 1.7	Vdc
Variable Gain Amplifier Control Voltage	V_{cntl}	0 to V_{CC}	Vdc
Transmit Enable Low Voltage	TX EN	0 to 0.2	Vdc
Transmit Enable High Voltage	TX EN	V_{CC} – 0.2 to V_{CC}	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, TX EN = 3.0 V, V_{cntl} = 0.0 V, V_D = 0.8 V_{PP}, V_B = 1.6 V, P_{LO} = –10 dBm, f_{LO} = 248 MHz, f_D = 100 kHz, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Current	–	10	12	mA
Standby Current (TX EN = 0.0V)	–	40	100	μA
Single Sideband Output Power Level	–15	–13	–	dBm
Single Sideband Output Power 1dB Compression Point	–	–10	–	dBm
LO Leakage(2)	–	–55	–45	dBm
Undesired Sideband Level	–	–35	–30	dBc
Output Level Dynamic Range (V_{cntl} = 0 to 2.2V)(2)	–	30	–	dB
Turn–on/off Time	–	2	–	μs
I/Q Data				
Input 3dB Bandwidth	–	5	–	MHz
Amplitude Imbalance	–	0.3	–	dB
Phase Imbalance	–	2	–	degree

(1) All electrical characteristics measured in test circuit schematic shown in Figure 1.
V_B is the bias voltage on the input data ports.
V_D is the sinusoidal differential voltage on the input data ports when testing the part in a single sideband mode.
Above power levels are the single–ended output power.

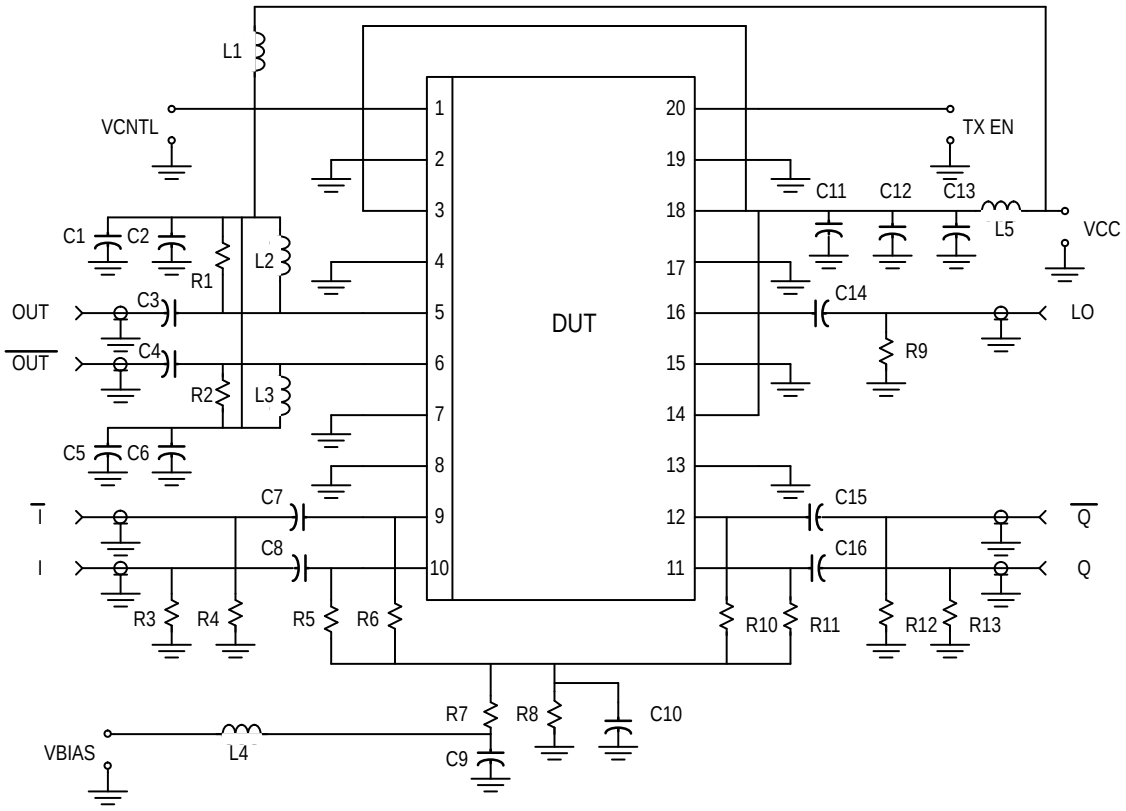
(2) LO leakage power is unaffected by V_{cntl} setting.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

Impedance Ω						
f	LO		IF or –IF		I, –I, Q, –Q	
MHz	R	jX	R	jX	R	jX
50	924	–694	164	–2330	181	–2448
60	825	–716	110	–1913	121	–2003
70	715	–713	83.2	–1661	88.1	–1709
80	635	–690	81.4	–1422	87.0	–1470
90	576	–691	86.8	–1312	93.4	–1361
100	509	–668	69.2	–1172	74.2	–1213
110	453	–651	56.0	–1055	72.2	–1091
120	400	–623	56.9	–969	60.3	–998
130	355	–595	47.3	–884	67.5	–913
140	330	–576	49.4	–835	38.3	–871
150	291	–551	49.8	–784	47.0	–815
160	259	–525	37.7	–730	41.2	–763
170	239	–509	32.5	–678	35.9	–712
180	225	–489	30.0	–651	33.0	–683
190	206	–473	30.4	–613	29.4	–644
200	187	–452	17.0	–579	22.7	–612
210	172	–440	33.1	–544	23.8	–580
220	158	–416	27.7	–521	24.5	–549
230	149	–402	20.5	–503	14.2	–530
240	137	–392	26.1	–482	18.3	–508
250	130	–375	19.5	–461	11.9	–485
260	119	–374	19.5	–437	17.1	–458
270	114	–353	20.1	–423	12.0	–443
280	105	–343	18.7	–408	11.1	–426
290	103	–332	20.7	–394	10.4	–412
300	93.5	–320	19.3	–380	9.65	–397
310	88.0	–312	17.9	–366	8.86	–380
320	84.8	–302	18.0	–354	6.91	–368
330	82.5	–296	19.4	–342	7.71	–354
340	76.1	–288	18.2	–332	6.02	–343
350	72.4	–282	15.0	–322	6.74	–331

Table 1. Selected Port Impedances

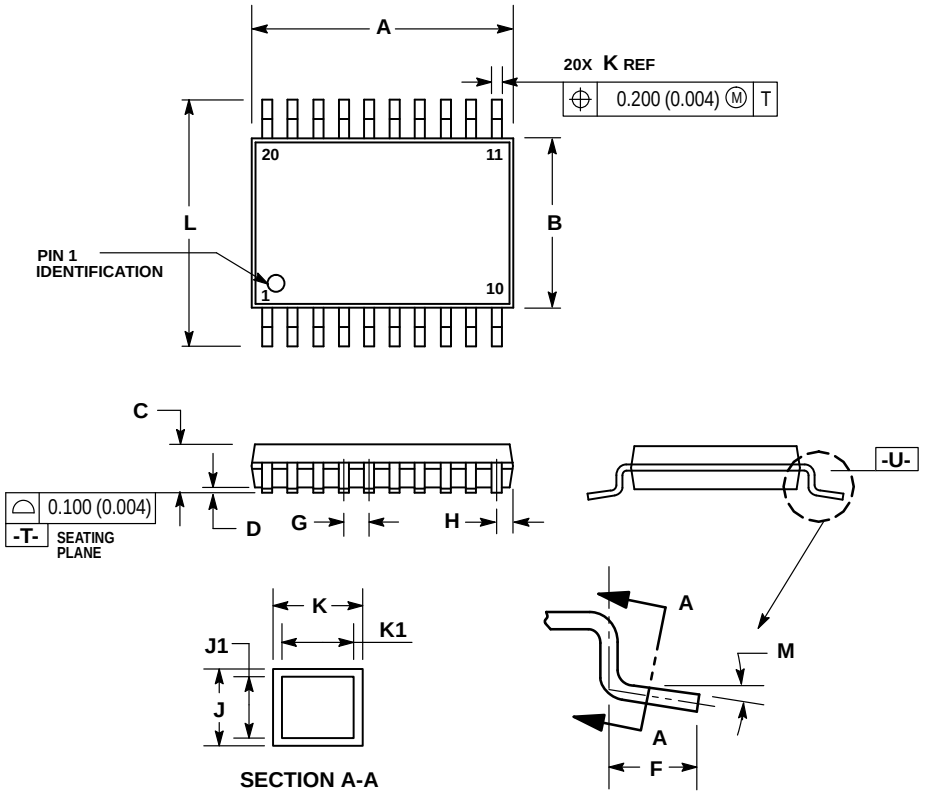


C1, C5, C9, C12 – 10000 pF, Chip Capacitor
C2, C6, C11 – 100 pF, Chip Capacitor
C3, C4 – 3.6 pF, Chip Capacitor
C7, C8, C10, C13, C15, C16 – 1 uF, Chip Capacitor
C14 – 10 pF, Chip Capacitor
L1, L4, L5 – 1.2 μH, Chip Inductor
L2, L3 – 68 nH, Chip Inductor

R1, R2 – 1000 Ω, Chip Resistor
R3, R4, R12, R13 – 510 Ω, Chip Resistor
R5, R6, R10, R11 – 2200 Ω, Chip Resistor
R7, R8, – 5100 Ω, Chip Resistor
R9 – 56 Ω, Chip Resistor

Figure 1. Typical Biasing Configuration

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –U–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	6.60	—	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.275	0.375	0.011	0.015
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

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ISSUE B

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