The MRFIC Line

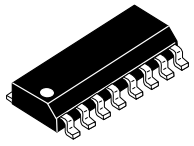
900 MHz LDMOS Integrated Power Amplifier

MRFIC0914

This integrated circuit is intended for two–way paging applications and for other Industrial, Scientific and Medical (ISM) at 900 MHz band applications. The three stage design is implemented in Motorola's low cost, high performance LDMOS process and housed in a low–cost surface mount SOIC package. Input and output matching is implemented off–chip for maximum flexibility while interstage matching is on–chip. A power control pin is included allowing 60 dB dynamic range.

- 30.5 dBm Output Power for 3 dBm Input Power at 900 MHz
- 32 dB Typ Small Signal Gain
- 40% Efficiency Min at 30.5 dBm Output Power
- 4.0 to 5.5 Volt Operation
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC0914R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0914

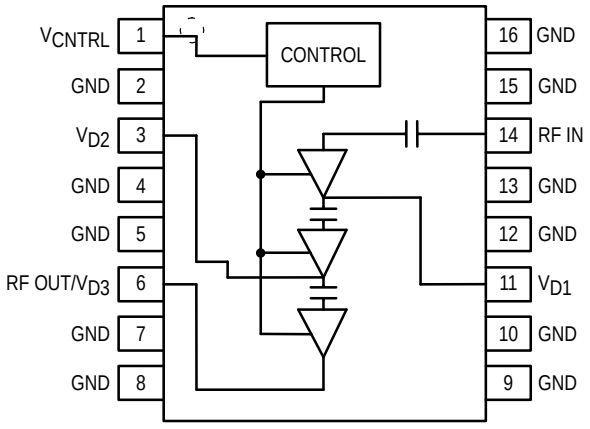
900 MHz PAGING
POWER AMPLIFIER
Si MONOLITHIC
INTEGRATED CIRCUIT



CASE 751B–05
(SOIC–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}, V_{D3}	9	Vdc
Supply Current	I_{Dtotal}	2	Adc
Power Control Voltage	V_{CNTRL}	4.8	Vdc
Input Power	P_{in}	6	dBm
Ambient Operating Temperature	T_A	–30 to +80	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	26	°C/W



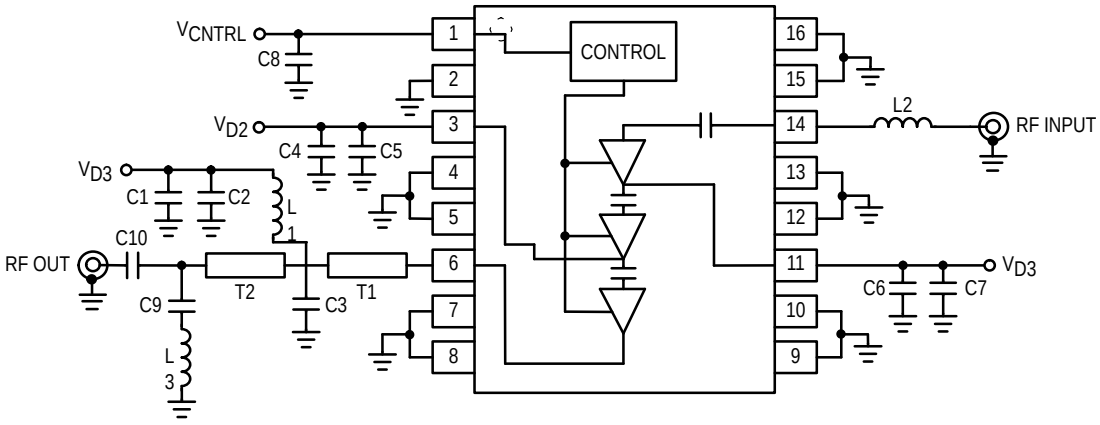
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}, V_{D3}	3.6 to 5.8	Vdc
Power Control Voltage	V_{CNTRL}	0 to 4.8	Vdc
RF Frequency Range	f_{RF}	890 to 928	MHz

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2}, V_{D3} = 4.8 V, f = 900 MHz, P_{in} = 3 dBm, 1 ms, 10% duty cycle, V_{CNTRL} Adjusted for I_{Dtotal} = 583 mA, T_A = 25°C unless otherwise noted. Measured in Circuit Configuration Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Output Power	1.12	—	—	W
Efficiency	40	—	—	%
Output Power at 1 dB Gain Compression	—	29	—	dBm
Saturated Output Power	—	31	—	dBm
Output Third Order Intercept Point	—	36	—	dBm
Dynamic Range (V_{CNTRL} = 0 to 4.8 V)	—	60	—	dB
Input Return Loss	7	12	—	dB
Output Power, Low Voltage (V_{D1}, V_{D2}, V_{D3} = 3.84 V)	0.56	—	—	W
Spurious Output (Load VSWR = 20:1, All Phase Angles)	—	–60	–50	dBc
Harmonic Output (With External Matching Circuit)	—	—	–45	dBc



C1, C7 — 0.01 µf
C2, C6, C8 — 33 pF
C3 — 12 pF
C4 — 1.0 µF
C5, C10 — 100 pF
C9 — 2.1 pF
L1 — 33 nH
L2 — 5.6 nH
L3 — 3.3 nH
T1 — 50 Ω MICROSTRIP, 7.5° @ 900 MHz
T2 — 50 Ω MICROSTRIP, 31.6° @ 900 MHz
BOARD MATERIAL — 18 MIL FR4

Figure 1. Application Circuit Configuration

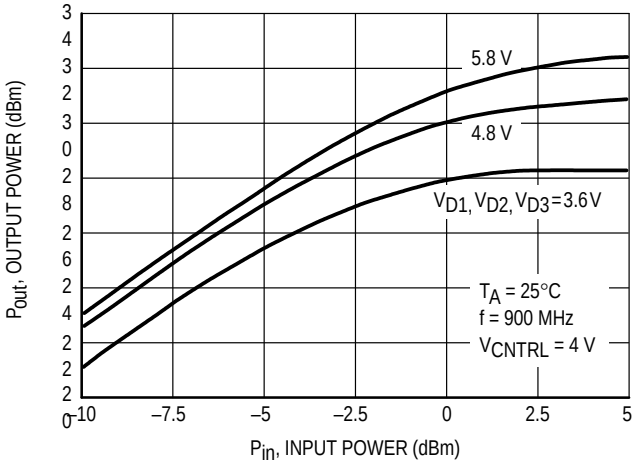


Figure 2. Output Power versus Input Power

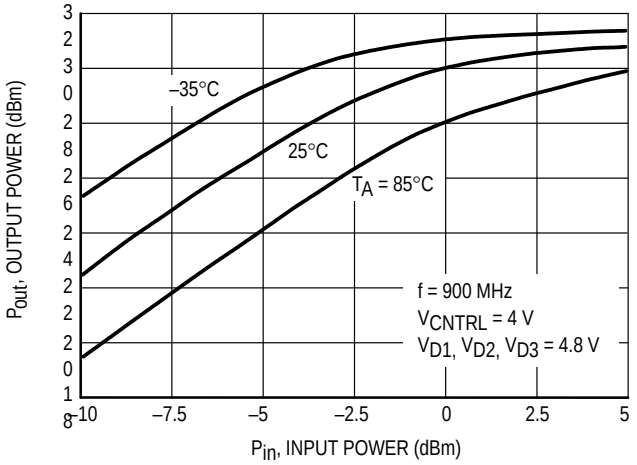


Figure 3. Output Power versus Input Power

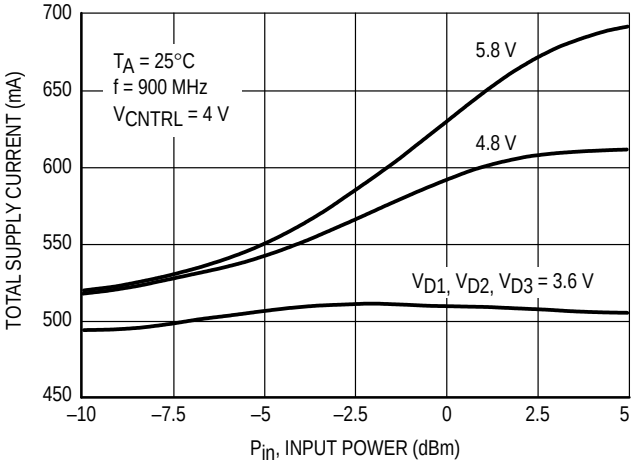


Figure 4. Supply Current versus Input Power

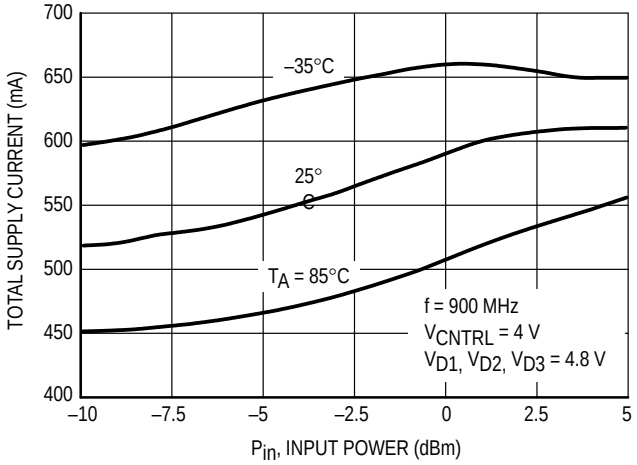


Figure 5. Supply Current versus Input Power

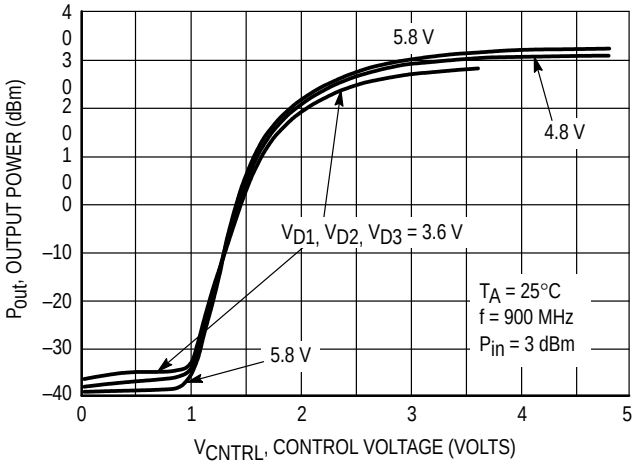


Figure 6. Output Power versus V_{CNTRL}

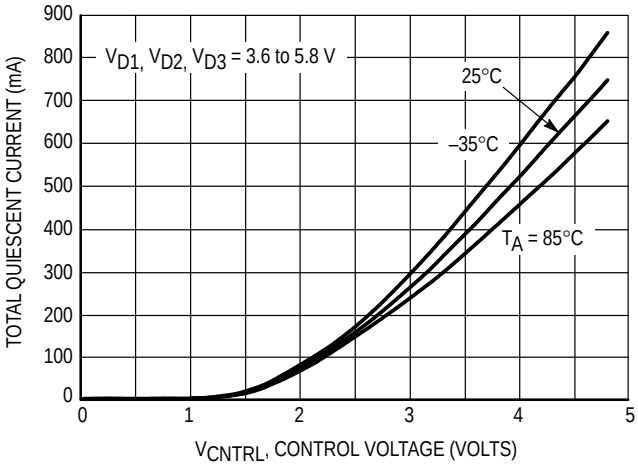


Figure 7. Quiescent Current versus V_{CNTRL}

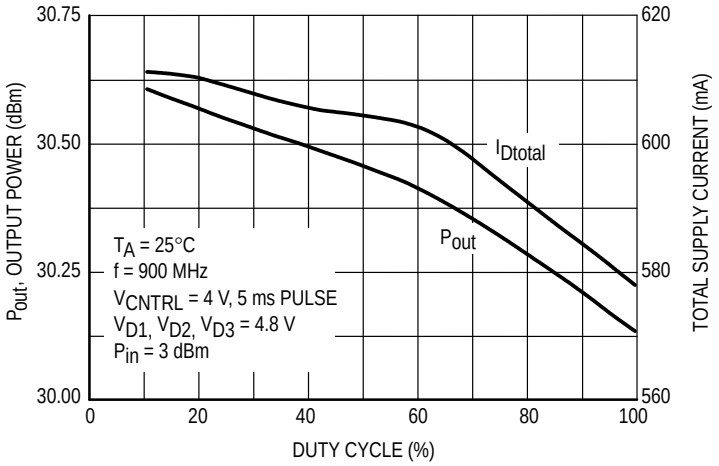


Figure 8. Output Power versus Duty Cycle

f	Z_{in} (Ω)		Z_{OL}^* (Ω)	
MHz	R	jX	R	jX
800	48.8	–16.3	2.56	14.3
850	49.0	–17.9	3.30	14.4
900	49.0	–19.6	2.80	13.1
950	49.4	–21.2	3.94	14.0
1000	49.8	–23.1	3.95	12.6

Table 1. Device Impedances Derived from Circuit Characterization

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC0914 three stage LDMOS integrated power amplifier was designed for low cost and flexibility. While the target application was two–way paging, the device can be used in a variety of 800 to 1000 MHz applications and it is particularly suited to burst mode digital transmissions with constant envelope modulation schemes. Only one supply is required. The V_{CNTRL} pin allows the setting of the gate bias of the three stages simultaneoulsy for optimum gain and efficiency and serves as a transmit control with more than 60 dB dynamic range.

CIRCUIT DETAILS

In Figure 1, the 900 MHz applications circuit, note that each stage has a separate supply pin, including the RF Output for the third stage. Care should be taken in bypassing these supply connections to avoid low frequency oscillation. Chip capacitors should be mounted as close to the leads and ground vias as possible. Ground vias should be provided close to the indicated ground leads as well. L1 is a bias choke supplying the third stage and could be replaced with a quarter wave line or air–wound inductor.

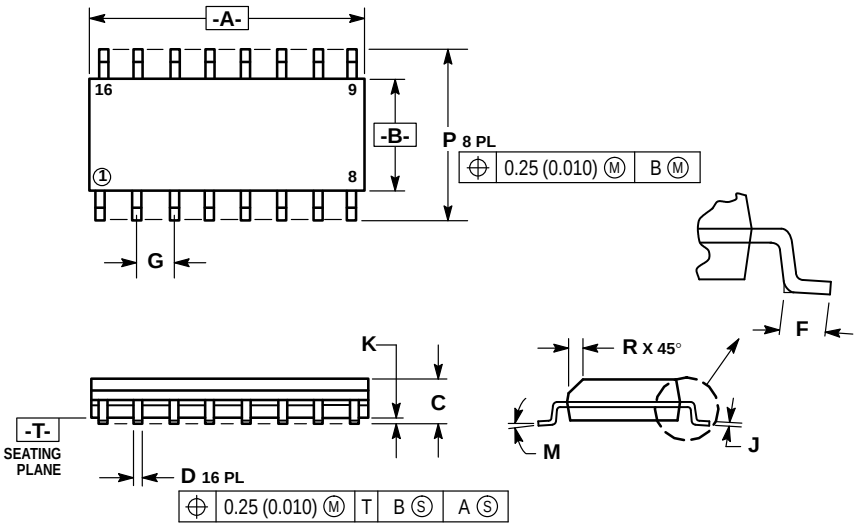
RF performance is sensitive to the output matching network. C9 and L3 form a second harmonic trap which enhances efficiency. Placement of C3 along the 50Ω line at the device output is critical to gain and efficiency. L2, the input matching inductor, is optional. Without this inductor, the input match is still typically better than 2:1 VSWR.

It should be note that Figure 1 does not portray the parasitics of the chip components nor their solder mounting pads. The board material is 18 mil dielectric thickness FR4. The impedances shown in Table 1 were derived from circuit characterization and are given as an aid to original designs.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” to the device type. For a complete list of currently available boards and ones in development for newly introduced products, please consult your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B-05
ISSUE J

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