

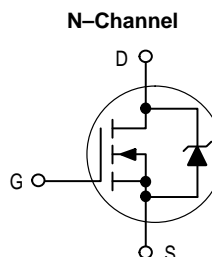
Product Preview

TMOS E-FET™

Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

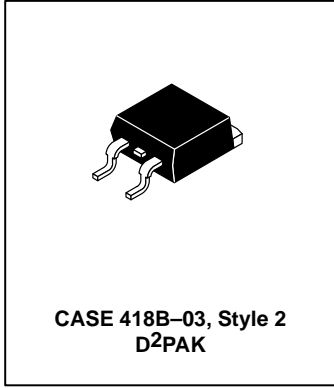
This advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature



MTB29N15E

TMOS POWER FET
29 AMPERES
150 VOLTS
 $R_{DS(on)} = 0.07 \text{ OHM}$



MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	150	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	150	Vdc
Gate-to-Source Voltage — Continuous	V_{GS}	± 20	Vdc
— Non-Repetitive ($t_p \leq 10 \text{ ms}$)	V_{GSM}	± 40	Vpk
Drain Current — Continuous	I_D	29	Adc
— Continuous @ 100°C	I_D	19	
— Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	102	Apk
Total Power Dissipation	P_D	125	Watts
Derate above 25°C		1.0	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (1)		2.5	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — STARTING $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, PEAK $I_L = 29 \text{ Apk}$, $L = 1.0 \text{ mH}$, $R_G = 25 \Omega$)	EAS	421	mJ
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
— Junction to Ambient	$R_{\theta JA}$	62.5	
— Junction to Ambient (1)	$R_{\theta JA}$	50	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	150 —	— TBD	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 150 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 150 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V _{GS} = ± 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	100	nAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 —	2.7 TBD	4.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 14.5 Adc)	R _{DS(on)}	—	0.055	0.07	Ohms
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc) (I _D = 29 Adc) (I _D = 14.5 Adc, T _J = 125°C)	V _{DS(on)}	— —	— —	2.4 2.1	Vdc
Forward Transconductance (V _{DS} = 8.6 Vdc, I _D = 14.5 Adc)	g _{FS}	10	18	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	—	2250	3150	pF
Output Capacitance		C _{oss}	—	455	910	
Transfer Capacitance		C _{rss}	—	133	190	

SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	(V _{DD} = 75 Vdc, I _D = 29 Adc, V _{GS} = 10 Vdc, R _G = 9.1 Ω)	t _{d(on)}	—	17.5	40	ns
Rise Time		t _r	—	108	220	
Turn-Off Delay Time		t _{d(off)}	—	90	180	
Fall Time		t _f	—	85	170	
Gate Charge	(V _{DS} = 120 Vdc, I _D = 29 Adc, V _{GS} = 10 Vdc)	Q _T	—	78	110	nC
		Q ₁	—	12	—	
		Q ₂	—	37	—	
		Q ₃	—	23	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

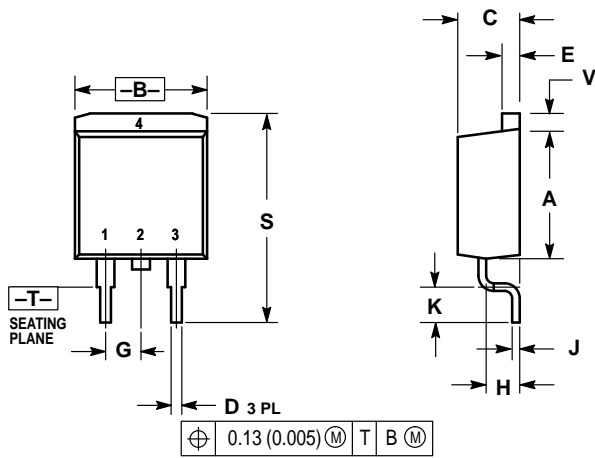
Forward On-Voltage (I _S = 29 Adc, V _{GS} = 0 Vdc) (I _S = 29 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	— —	0.92 TBD	1.3 —	Vdc	
Reverse Recovery Time	(I _S = 29 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	—	174	—	ns
		t _a	—	140	—	
		t _b	—	34	—	
Reverse Recovery Stored Charge	Q _{RR}	—	1.4	—	μC	

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _D	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _S	—	7.5	—	

- (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- (2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

CASE 418B-03
 ISSUE C

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