Order this document by MC44145/D

MOTOROLA

MC44145

Pixel Clock Generator/ Sync Separator

The MC44145, Pixel Clock Generator, is a component of the MC44000 family.

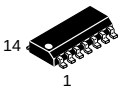
The MC44145 contains a sync separator with composite sync and vertical outputs, and clock generation circuitry for the digitization of any video signal along with the necessary circuitry for clock generation, such as a phase comparator and a divide–by–2 to provide a 50% duty cycle.

The MC44145 is available in a SO–14 package and is fabricated in the Motorola high density, high speed, low voltage, process called MOSAIC 1.5®.

MOSAIC is a trademark of Motorola, Inc.

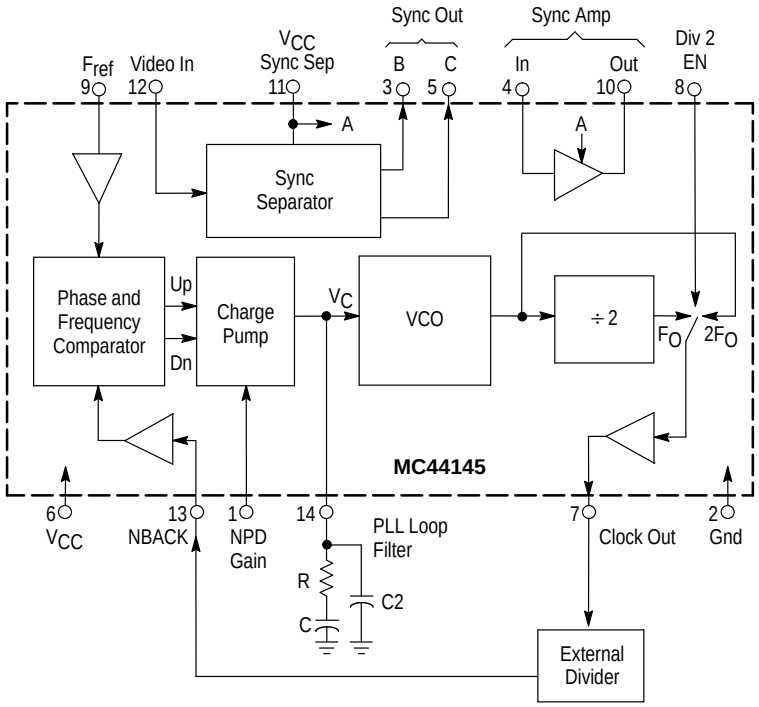
PIXEL CLOCK GENERATOR/ SYNC SEPARATOR

SEMICONDUCTOR TECHNICAL DATA



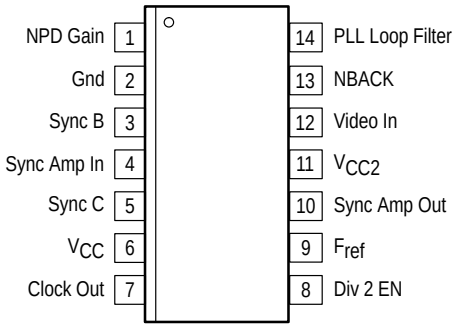
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

Representative Block Diagram



This device contains 214 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44145D	T_A = 0° to +70°C	SO–14

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{CC2}	6.0 6.0	V
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{CC2}	6 11	4.75 4.75	5.0 5.0	5.5 5.5	Vdc
Video Input Amplitude (Note 2)	V_{in}	12	0.4	1.0	2.5	Vpp
NBACK Pulse Width	NBACK	13	100	500	–	ns
F_{ref} Pulse Width	F_{ref}	9	100	500	–	ns
Operating Ambient Temperature	T_A	–	0	–	+70	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Note	Pin	Min	Typ	Max	Unit
POWER SUPPLY							
Supply Current (Note 1)	I_{CC}	–	6	–	15.5	–	mA
Supply Current	I_{CC2}	–	11	–	300	–	µA
SYNC SEPARATOR (V_{CC} = 5.0 V; T_A = 25°C, unless otherwise specified.)							
Sync B Output	–	3	3	–	5.0 to 0	–	V
Sync C Output (1.0 mA Source)	–	4	5	–	0 to 3.3	–	V
Slicing Level (S_L)	–	–	12	–	$V_{CC/2}$	–	V
Video Input Sink Current	–	$V_{Pin\ 12} < S_L$	12	–	18	–	µA
Video Input Source Current	–	$V_{Pin\ 12} > S_L$	12	–	1.2	–	µA

NOTES: 1. Operating current for Pin 6 is dependent on the clock frequency (Pin 7). Values given are specified for Pin 14 = 4.0 V.
2. Positive Video.
3. High impedance output.
4. Low impedance output.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Note	Pin	Min	Typ	Max	Unit
SYNC SEPARATOR (V_{CC} = 5.0 V; T_A = 25°C, unless otherwise specified.)						
VCO (V_{CC} = 5.0 V; T_A = 25°C, unless otherwise specified, divider disabled.)						
F_{min}	1, 5	7, 8, 14	–	–	10	MHz
F_{max}	1, 4	7, 8, 14	39	42	–	MHz
Control Range	2	14	1.0	–	4.0	V
Transfer Function	1	7, 8, 14	–	14	–	MHz/V
Input Resistance	9	14	0.5	–	–	MΩ
Charge Pump	6 7	1, 14	– –	40 80	– –	µA
Phase Jitter	8	7, 9	–	–	3.0	ns
INPUT BUFFERS (F_{ref} AND NBACK) (T_A = 25°C, unless otherwise specified.)						
Threshold (TTL Compatible)	–	9, 13	–	2.5	–	V
Input Current	–	9, 13	–	–	1.0	µA
OUTPUT BUFFER CLOCK (T_A = 25°C, unless otherwise specified.)						
Sync Amplifier Output High Level	1.0 mA Source	10	2.4	3.0	–	V
Sync Amplifier Output Low Level	1.0 mA Sink	10	–	0.2	0.4	V
Rise Time	11	10	–	–	6.0	ns
Fall Time	11	10	–	–	6.0	ns
Load Capacitance	10	10	–	15	–	pF

NOTES: 1. Internal divider disabled.
2. 0 V stops the oscillator.
3. Divider ÷2 active.
4. V_C = 4.0 V.
5. V_C = 1.0 V.
6. PFD gain low.
7. PFD gain high.
8. VCO alone.
9. V_C = 4.0 V, charge pumps off.
10. 2 LSTTL loads.
11. With cap load 15 pF and between 10 and 90% of 0.4 and 2.4 V.

CIRCUIT DESCRIPTION

Composite Sync Separator

The composite sync separation section is comprised of two blocks, a sync slicer and a sync amplifier, which can be used to extract the vertical sync and composite sync information from a video signal.

The sync separator is an adaptive slicer in which the video signal is slightly integrated and then sliced at a ratio of 4.7 to 64 which corresponds to the sync to horizontal ratio. Two outputs are given, one of high impedance and the other low impedance.

A slicing sync inverting amplifier is also on–chip, allowing one output to be used for composite sync and the other output to be integrated and then sliced using the slicing amplifier to extract the vertical sync information.

Clock Generation

The clock generation is made up of a wide ranging emitter–coupled VCO followed by a switchable ÷2 to provide a 50% duty cycle wherever required, or twice the set frequency if an external divider is used. The clock generator is a PLL subsection; its function is the generation of a high frequency, line locked clock that is used for video sampling and digitizing.

The clock output is a LSTTL–like buffer which has a limited drive capability of two LSTTL loads.

The VCO is driven from a charge pump with selectable current. The charge pump is driven by the phase comparator.

The phase comparator is a type IV “phase and frequency comparator” sequential circuit.

The clock generator, the heart of a PLL, is to be closed by means of an external divider, thus setting the synthesized frequency. This divider could be implemented in discrete logic or be a part of an ASIC subsystem.

Phase and Frequency Comparator

The phase comparator is fed from two input buffers, F_{ref} which expects a reference frequency at line rate and that is rising edge sensitive, and NBACK which comes from the external divider and is falling edge sensitive.

Charge pump current and output divider action are controlled by applying suitable voltage on the appropriate pins (respectively, NPD Gain and Div 2 EN).

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	NPD Gain	This pin sets the gain of the phase frequency detector by changing the current of the charge pump output (40 μA or 80 μA). Low current with this pin > 2.0 V, high current for < 0.5 V.
2	Ground	Ground connection common to the PLL and sync separator sections.
3	Sync B	High impedance sync output.
4	Sync Amp In	Sync amplifier input.
5	Sync C	Low impedance sync output.
6	V_{CC}	Power connection to the PLL section.
7	Clock Out	VCO clock output. Capable of limited LSTTL drive. It should not be used to drive high capacitive loads, such as long PCB traces or coaxial lines.
8	Div 2 EN	The divider is switched in with this pin > 2.0 V; switched out for < 0.5 V.
9	F_{ref}	Reference frequency input to the phase and frequency comparator. Typically this will be a 15625 (15750) Hz signal. It is rising edge sensitive. Due to the nature of the phase and frequency comparator, no missing pulses are tolerable on this input. In a typical setup, this signal can be provided by the MC44011.
10	Sync Amp Out	Sync amplifier output.
11	V_{CC2}	Power connection to the sync separator and amplifier.
12	Video In	Video signal input to the sync separator.
13	NBACK	Fed by the external clock divider. Sets the multiplication ratio of the loop in multiples of the F_{ref} frequency. Negative edge sensitive.
14	PLL Loop Filter	See loop filter calculations at the end of this document.

NOTE: The two V_{CC} pins are not independent, as they are internally connected by means of the input protection diodes; they must always be both connected to a suitable V_{CC} line.

CIRCUIT OPERATION

Composite Sync Separator

The sync separator is an adaptive slicer. It will output “raw” sync data. Two outputs are given, thus allowing one output to be used for composite sync and the other output to be integrated and then sliced using the inverting slicing amplifier provided. As the input of the slicing amplifier is external, the amplifier may be driven from either sync output, although normally the high impedance output (Sync B) would be recommended.

The positive video input signal required is nominally 1.0 V sync–to–white, but the circuit supports signals above and below this level and also is resistant to a degree of reflections on the signal. Coupling to the sync separator may be achieved by a simple capacitor of 100 nF, but better results may be obtained with a higher value in series with a resistance of 1.0 kΩ.

Clock Generator

The system is best put to use in a dual loop configuration; a first loop locks to line frequency by means of a type I phase detector (multiplier type) which is insensitive to missing pulses. This PLL is then followed by a second loop using the MC44145, performing frequency multiplication. The phase comparator of the MC44145 is frequency and phase sensitive. It is a type IV (sequential type) phase detector, which does not tolerate missing pulses. The dual loop structure makes up a noise insensitive frequency (and phase) locked loop.

The phase and frequency comparator provides two logical outputs, mutually exclusive – up or down – that are used to source or sink current to and from the loop filter. This current can be user–selected to be 40 μA or 80 μA (typical), thus providing some degree of loop gain control.

The VCO is an emitter–coupled multivibrator type, with an on–chip timing capacitor, and has been designed for low phase noise.

The divide–by–2 is included at the output of the VCO, thus allowing for a precise 50% duty cycle, hence the VCO is operating at twice the required frequency. The divider can be bypassed, bringing the VCO output directly to the output buffer.

The external divider must provide a feedback pulse to close the loop; the falling edge of this pulse will be aligned (when the loop is in lock) with the rising edge of the pulse applied to the F_{ref} input. Operation of the phase comparator is insensitive to the duty cycle of both its inputs. The feedback pulse should have a minimum width of 500 ns. This can be guaranteed if it has a length of at least 16 output clock cycles (highest output frequency with the divider disabled).

APPLICATION INFORMATION

Analog video signals out of the MC44011 are sampled and converted to 8–bits digital in the A/D converter (MC44250 series) by means of the clock provided by the MC44145, pixel clock generator (see Figure 1).

The frame store contains the memory, the necessary logic for the memory addressing, as well as the counter to set the frequency multiplication ratio of the line locked clock generator (H. Count).

Figure 1. Application Block Diagram

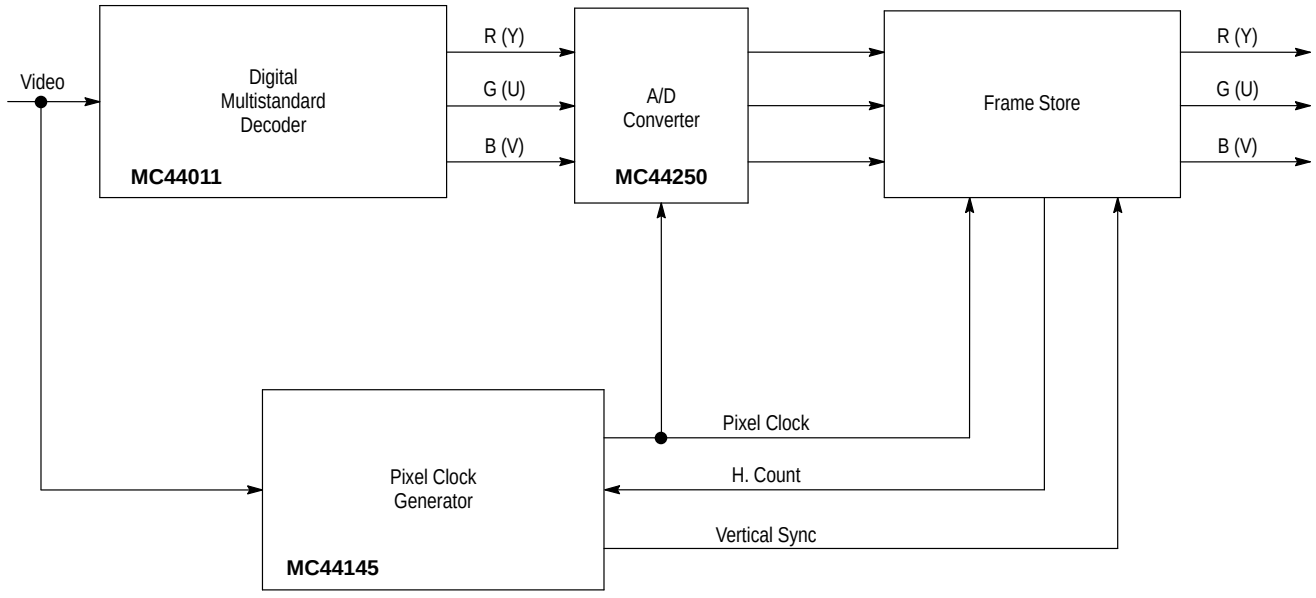


Figure 2.

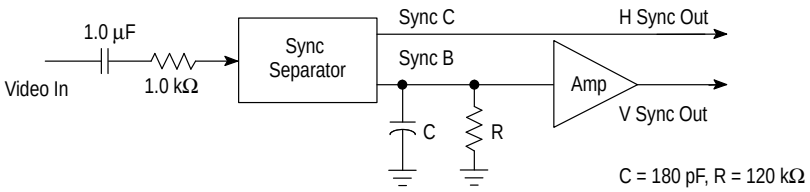


Figure 3. Typical VCO Transfer Characteristics

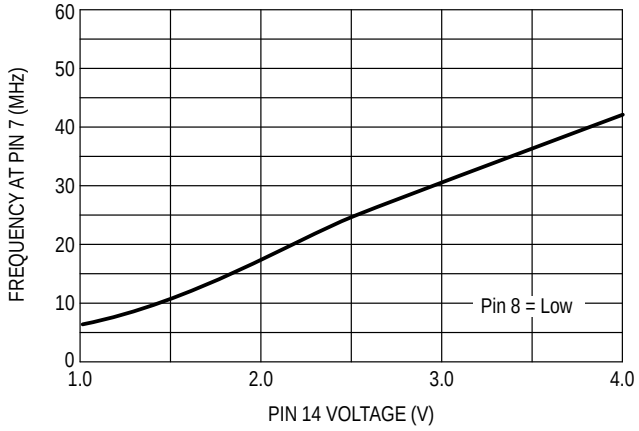
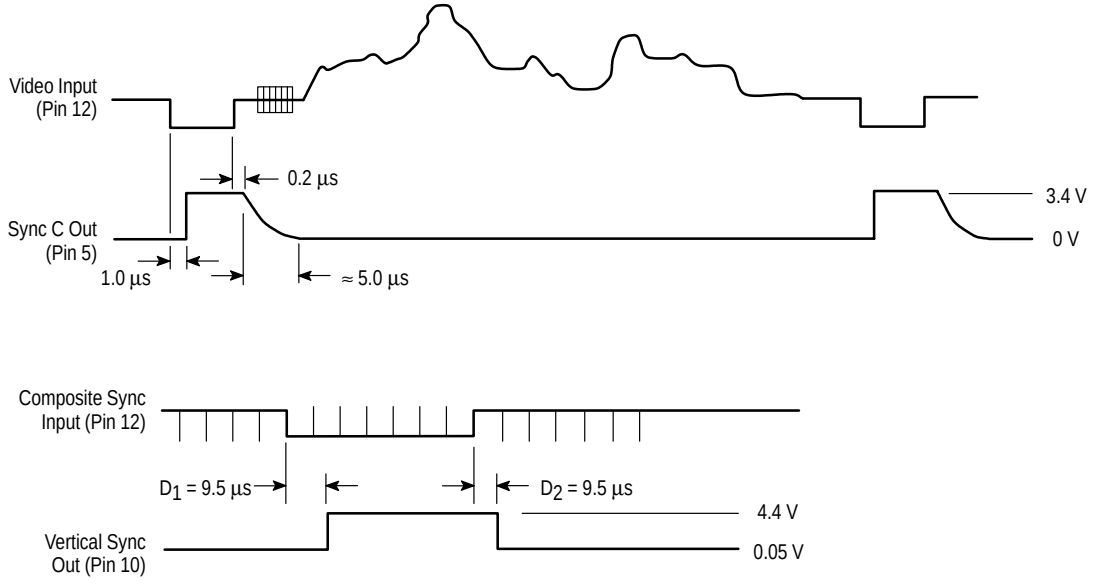


Figure 4. Sync Separator Timing



Note: D_1 and D_2 depend on the value of R and C connected to Pin 3. They are specified here for the values: R = 120 kΩ, and C = 180 pF.

LOOP FILTER CALCULATION

This section is not intended as a complete loop theory; its aim is merely to point out the peculiarities of the loop, and provide the user with enough information for the filter components selection. For a more in–depth covering, the cited reference should be consulted, especially [1].

The following remarks apply to the loop:

- The loop frequency is 15 kHz.
- In spite of the sampled nature of the loop, a continuous time approximation is possible if the loop bandwidth is sufficiently small.
- Ripple on V_C is a function of the loop bandwidth
- The loop is a type II, 3rd order; however, since C2 is small, the pole it creates is far removed from the low frequency dominant poles, and the loop can be analyzed as a 2nd order loop.

These remarks apply to the PFD:

- Phase and frequency sensitive.
- Independent of duty cycle.
- PFD has 3 allowed states: up, down, hi–Z
- The VCO is always pulled in the right direction (during acquisition).
- PFD gain is higher near lock.

The last two remarks imply that only the higher value need be taken into account, as acquisition will be slower, but always in the proper direction, whereas the higher gain will enter the action as soon as the error reaches $\pm 2\pi$.

The following values are selected and defined (see Block Diagram):

C2 = C/10 or less, to satisfy the requirement that the effect of C2 on the low frequency response of the loop be minimal, and similar to a second order loop.

$\zeta = 0.707$ for the damping factor.

$\omega i = 15625 \times 2\pi$ the input pulsation.

$\tau = RC$ as the loop filter.

$K = Ko \times Ip \times R/(2 \times \pi \times N)$ the loop gain.

$K' = K \times \tau = 4\zeta^2$ is the “normalized” loop gain.

$Ko = 57 \times 10^6$ [rad/Vs] (9.0 MHz/V).

Stability analysis, with C2 = C/10 and $K' = 2$ ($\zeta = 0.707$) gives a minimum value of 7.5 for the ratio $\omega i/K$ and to have some margin, a reasonable value can be 15 to 20 or higher [1].

Selecting $\omega i/K = 20$, gives : $K = \omega i/20 \approx 5000$.

With $K' = 2$, $\tau = 2/K = 400\ \mu s$.

Using $K = Ko \times Ip \times R/(2 \times \pi \times N)$ and setting $Ip = 60\ \mu A$, and N an average value of 1000, we get $R = 9.1\ k\Omega$.

Then for $\tau = 400\ \mu s$, C becomes 47 nF and C2, 4.7 nF.

With these values, the loop natural frequency (ωn) and the loop bandwidth ($\omega 3dB$) can be calculated:

$\omega n = [(Ko/N) \times Ip/(2\pi C)]^{1/2} = 3400$ and

$fn = 3400/2\pi = 540$ Hz.

$\omega 3dB = 2 \times \omega n = 1080$ Hz (valid if ζ is close to 0.707).

References:

[1] Charge–Pump Phase–Lock Loops, Floyd M. Gardner, IEEE transactions on communications, vol. com–28 no. 11 November 1980

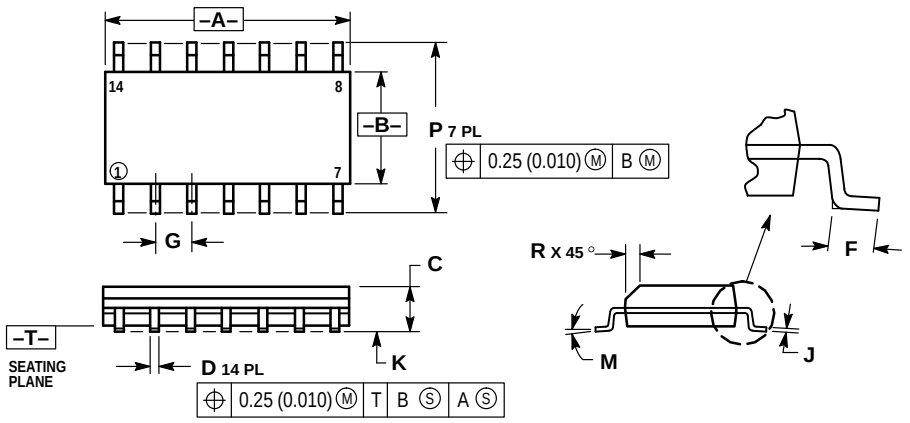
[2] Phaselock Techniques, Floyd M. Gardner, J. Wiley & Sons, 1979

[3] Phase–Locked Loops, Roland E. Best, McGraw–Hill, 1984

[4] Phase–Locked Loop Systems, Motorola

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298