MC145447

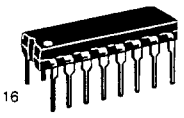
Calling Line Identification (CLID) Receiver with Ring Detector

The MC145447 is a silicon gate HCMOS IC designed to demodulate Bell 202 and V.23 1200–baud FSK asynchronous data. The primary application for this device is in products that will be used to receive and display the calling number, or message waiting indicator sent to subscribers from participating central office facilities of the public switched network. The device also contains a carrier detect circuit and ring detector which may be used to power up the device.

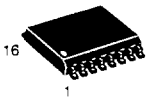
Applications for this device include adjunct boxes, answering machines, feature phones, fax machines, and computer interface products.

The MC145447 offers the following performance features.

- Ring Detector On–Chip
- Ring Detect Output for MCU Interrupt
- Power–Down Mode, Less than 1 μA
- Single Supply: + 3.5 to + 6.0 V
- Pin Selectable Clock Frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz
- Two Stage Power–Up for Power Management Control
- Demodulates Bell 202 and V.23



P SUFFIX
PLASTIC DIP
CASE 648

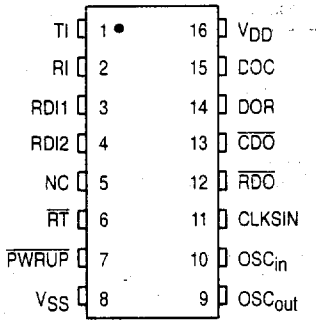


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

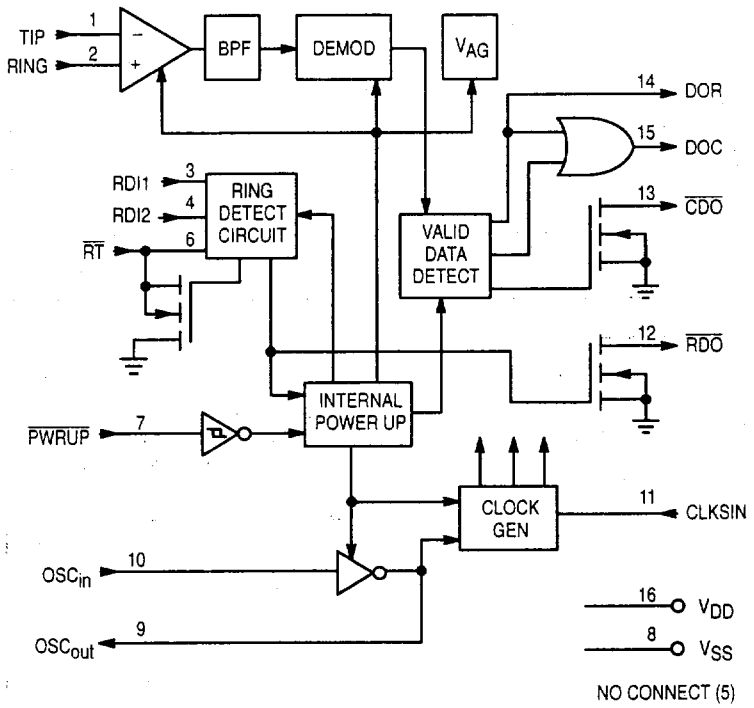
MC145447P	Plastic DIP
MC145447DW	SOG Package

PIN ASSIGNMENT



NC = NO CONNECTION

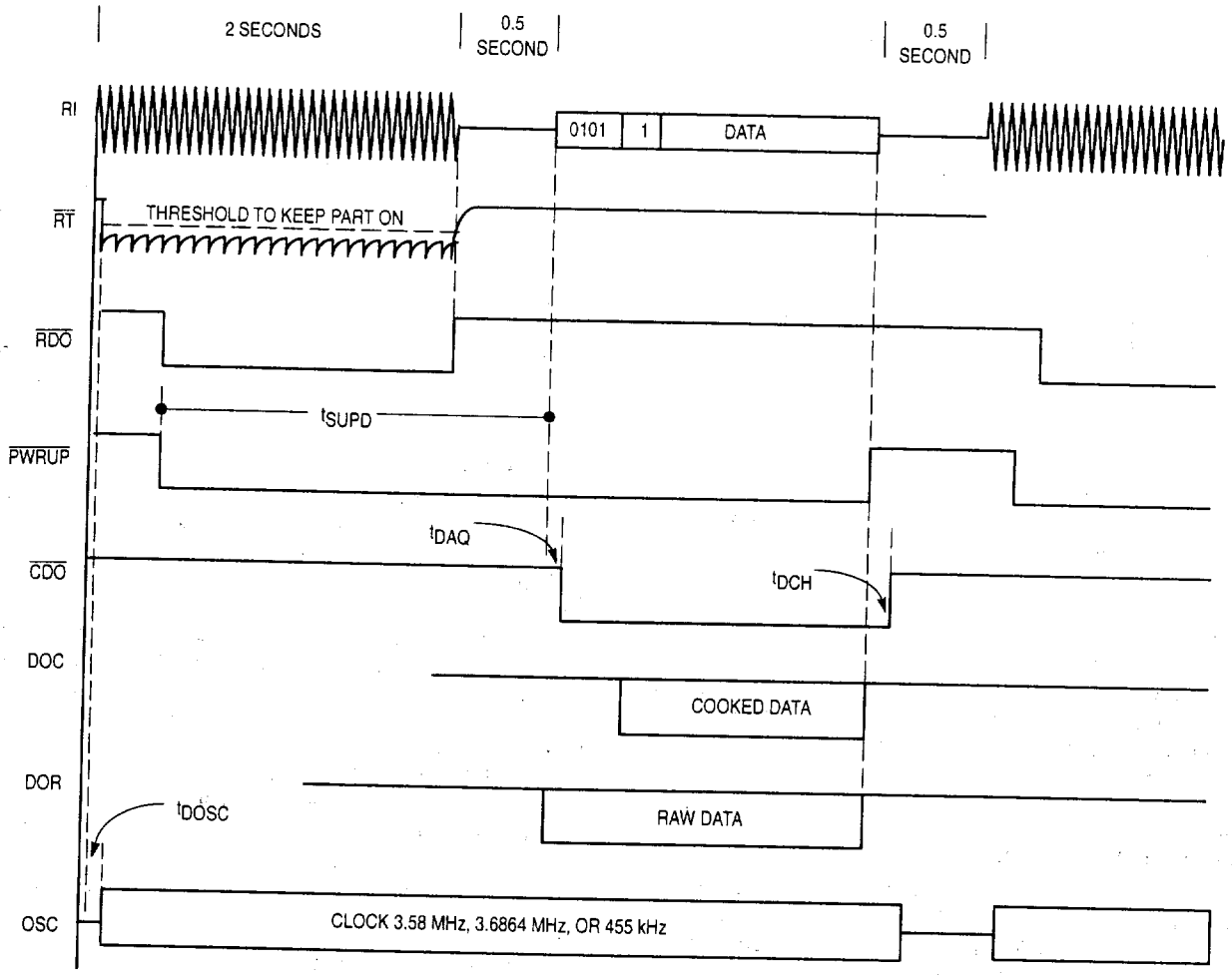
BLOCK DIAGRAM



SWITCHING CHARACTERISTICS (V_{DD} = + 5 V, C_L = 50 pF, T_A = + 25°C)

Description	Symbol	Min	Typ	Max	Unit
OSC Startup	t_{DOSC}	—	2	—	ms
Power–Up Low to FSK (Setup Time)	t_{SUPD}	15	—	—	ms
Carrier Detect Acquisition Time	t_{DAQ}	—	14	—	ms
End of Data to Carrier Detect High	t_{DCH}	8	—	—	ms

TIMING DIAGRAM



$\overline{RT}$	$\overline{PWRUP}$	I_{DD}	OSC_{in}
1	1	1 µA MAX	DISABLE
0	1	2.4 mA TYP	ENABLE
X	0	6.2 mA TYP	ENABLE

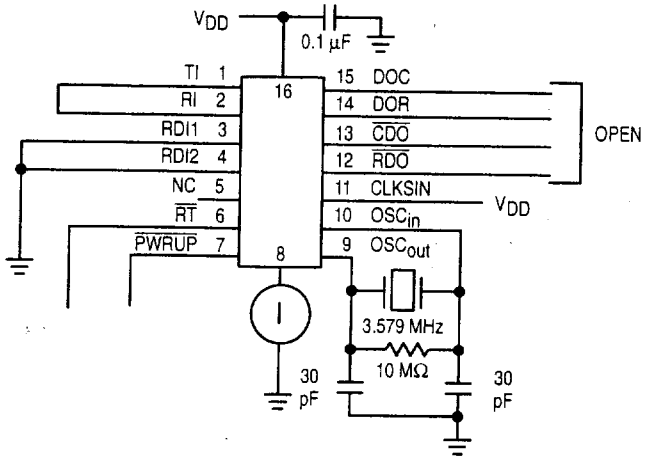


Figure 1. I_{DD} Test Circuit

PIN DESCRIPTIONS

TI
Tip Input (Pin 1)

This input pin is normally connected to the tip side of the twisted pair. It is internally biased to 1/2 supply voltage when the device is in the power–up mode. This pin must be dc isolated from the line.

RI
Ring Input (Pin 2)

This input is normally connected to the ring side of the twisted pair. It is internally biased to 1/2 supply voltage when the device is in the power–up mode. This pin must be dc isolated from the line.

RDI1
Ring Detect Input 1 (Pin 3)

This input is normally coupled to one of the twisted pair wires through an attenuating network. It detects energy on the line and enables the oscillator and precision ring detection circuitry.

RDI2
Ring Detect Input 2 (Pin 4)

This input to the precision ring detection circuit is normally coupled to one of the twisted pair wires through an attenuating network. A valid ring signal as determined from this input sends the $\overline{RDO}$ (Pin 12) to a logic 0.

$\overline{RT}$
Ring Time (Pin 6)

An RC network may be connected to this pin. The RC time constant is chosen to hold this pin voltage below 2.2 V between the peaks of the ringing signal. $\overline{RT}$ is an internal power–up control and activates only the circuitry necessary to determine if the incoming ring is valid.

$\overline{PWRUP}$
Power Up (Pin 7)

A logic 0 on the $\overline{PWRUP}$ input causes the device to be in the active mode ready to demodulate incoming data. A logic 1 on this pin causes the device to be in the standby mode, if the $\overline{RT}$ input pin is at a logic 1. This pin may be controlled by $\overline{RDO}$ and $\overline{CDO}$ for auto power–up operation. For other applications, this pin may be controlled externally.

V_{SS}
Ground (Pin 8)

Ground return pin is typically connected to the system ground.

OSC_{out}
Oscillator Output (Pin 9)

This pin will have either a crystal or a ceramic resonator tied to it with the other end connected to OSC_{in}.

OSC_{in}
Oscillator Input (Pin 10)

This pin will have either a crystal or a ceramic resonator tied to it with the other end connected to OSC_{out}. OSC_{in} may also be driven directly from an appropriate external source.

CLKSIN
Clock Select Input (Pin 11)

A logic 1 on this input configures the device to accept either a 3.579 MHz or 3.6864 MHz crystal. A logic 0 on this pin configures the part to operate with a 455 kHz resonator.

For crystal and resonator specifications see Table 1.

$\overline{RDO}$
Ring Detect Out (Pin 12)

This open–drain output goes low when a valid ringing signal is detected. $\overline{RDO}$ remains low as long as the ringing signal remains valid. This signal can be used for auto power–up, when connected to Pin 7.

$\overline{CDO}$
Carrier Detect Output (Pin 13)

When low, this open drain output indicates that a valid carrier is present on the line. $\overline{CDO}$ remains low as long as the carrier remains valid. An 8 ms hysteresis is built in to allow for a momentary drop out of the carrier. $\overline{CDO}$ may be used in the auto power–up configuration when connected to $\overline{PWRUP}$.

DOR
Data Out Raw (Pin 14)

This pin presents the output of the demodulator whenever $\overline{CDO}$ is low. This data stream includes the alternate 1 and 0 pattern, and the 150 ms of marking, which precedes the data. At all other times, DOR is held high.

DOC
Data Out Cooked (Pin 15)

This output presents the output of the demodulator whenever $\overline{CDO}$ is low, and when an internal validation sequence has been successfully passed. The output does not include the alternate 1 and 0 pattern. At all other times, DOC is held high.

V_{DD}
Positive Power Supply (Pin 16)

The digital supply pin, which is connected to the positive side of the power supply.

APPLICATIONS INFORMATION

The MC145447 has been designed to be one of the main functional blocks in products targeted for the CLASS (Custom Local Area Signaling Service) market. CLASS is a set of subscriber features now being presented to the consumer by the RBOCs (Regional Bell Operating Companies) and independent TELCOs. Among CLASS features, such as distinctive ringing and selective call forwarding, the subscriber will also have available a service known as Calling Number Delivery (CND) and message waiting. With these services, a subscriber will have the ability to display at a minimum, a message containing the phone number of the calling party, the date, and the time. A message containing only this information is known as a single format message, as shown in Figure 9. An extended message, known as multiple format message, can contain additional information as shown in Figure 10.

The interface should be arranged to allow simplex data transmission from the terminating central office, to the CPE (Customer Premises Equipment), only when the CPE is in an on–hook state. The data will be transmitted in the silent period between the first and second power ring after a voice path has been established.

The data signaling interface should conform to Bell 202, which is described as follows:

- Analog, phase coherent, frequency shift keying
- Logical 1 (Mark) = 1200 ± 12 Hz
- Logical 0 (Space) = 2200 ± 22 Hz
- Transmission rate = 1200 bps
- Application of data = serial, binary, asynchronous

The transmission level from the terminating C.O. will be – 13.5 dBm ± 1.0. The expected worst case attenuation through the loop is expected to be – 20 dB. The receiver therefore, should have a sensitivity of approximately – 34.5 dBm to handle the worst case installations.

Additional information on CLASS services can be obtained from:

BELLCORE CUSTOMER SVS.
1–800–521–2673
201–699–5800 FOREIGN CALLS
201–699–0936 FAX

The document number is: TA–NWT–000030
Title: "Voice Band Data Transmission Interface Generic Requirements"

Figure 7 is a conceptual design of how the MC145447 can be implemented into a product which will retrieve the incoming message and convert it to EIA–232 levels for transmission to the serial port of a PC. With this message and appropriate software, the PC can be used to look up the name and any additional information associated with the caller that had been previously stored.

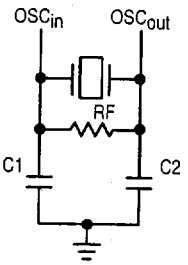
Figure 8 is a conceptual design of an adjunct unit in parallel with an existing phone. This arrangement gives the subscriber CND service without having to replace existing equipment.

Table 1. Oscillator Specifications

Clock Select Pin 11 = 1

Crystal Mode	Parallel
Frequency	3.579 MHz or 3.6864 MHz
R_f	10 MΩ
C1 and C2	30 pF

Source:
Fox Electronics
5570 Enterprise Pkwy.
Ft. Myers, FL 33905
Tel. 813–693–0099



Clock Select Pin 11 = 0

Resonator	#CSB455J
Frequency	455 kHz ± 0.5%
R_f	1.0 MΩ
C1 and C2	100 pF

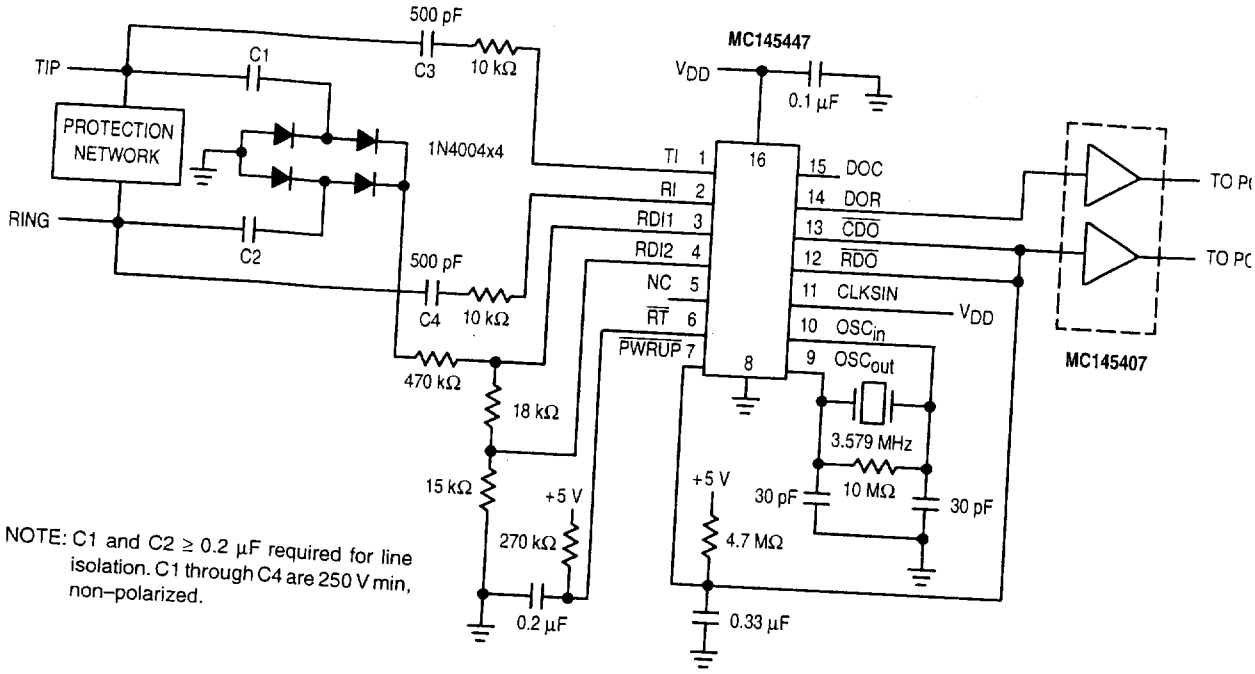
Source:
Murata Manufacturing Co. Ltd.
2200 Lake Park Dr.
Smyma, GA 30080
Tel. 404–436–1300

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing.

FULL–TIME POWER–UP APPLICATION WITH RING DETECTOR CIRCUIT DISABLED

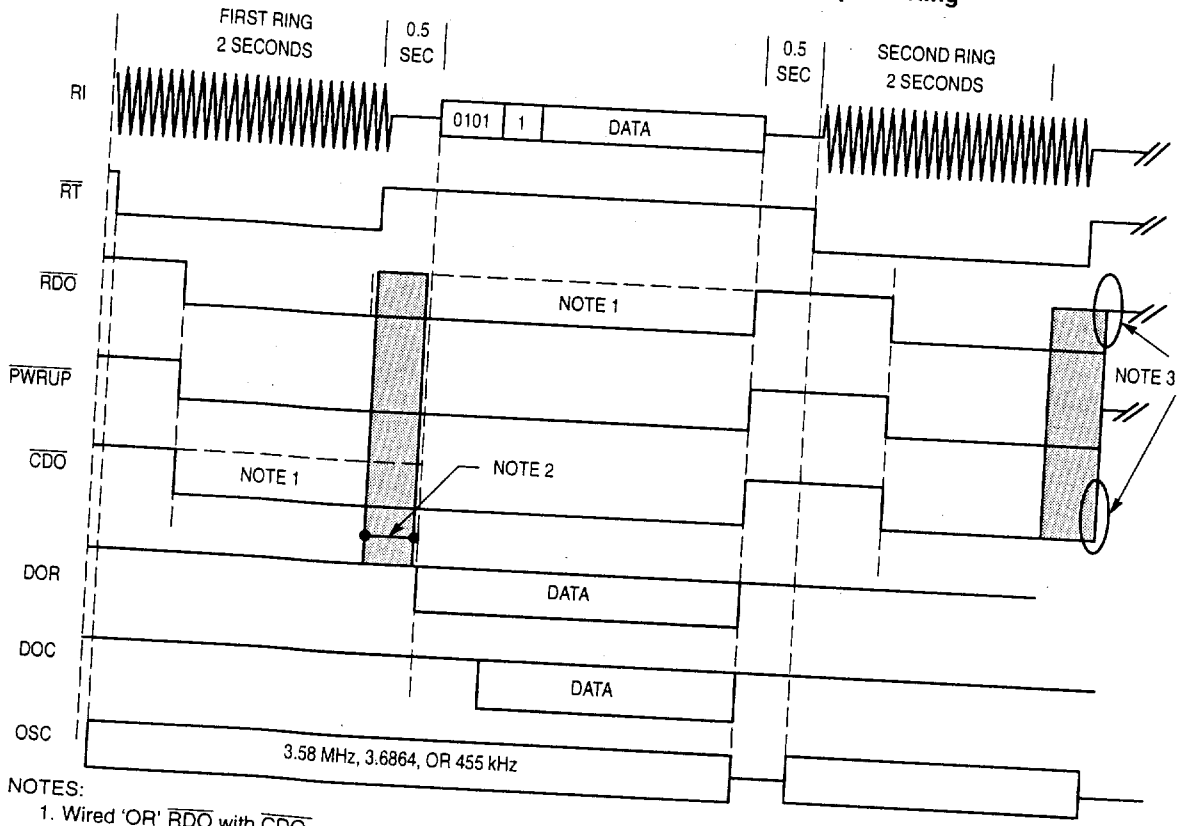
Some MC145447 applications require that the Calling Line Identification Receiver be constantly powered. To ensure that the device is properly reset, a Logic 1 must be applied to $\overline{PWRUP}$ (Pin 7) for a minimum of 10 µs after V_{DD} has reached its full value. It is also necessary that the $\overline{RT}$ pin (Pin 6) be high while $\overline{PWRUP}$ is high. This may be accomplished with an external ring detect signal or MCU generated signal applied to $\overline{PWRUP}$. Alternatively, a power on reset RC network may be used as shown in Figure 6. Rpu and Cpu must be chosen such that the voltage at $\overline{PWRUP}$ meets the logic 1 input threshold requirements for 10 µs after V_{DD} has reached its full value. The power supply rise time on V_{DD} (Pin 16) must also be taken into account when determining Rpu and Cpu. See Figure 3 for a description of the change in input thresholds (V_{T+} and V_{T-}) with respect to V_{DD} for $\overline{PWRUP}$. Also, some applications may not require the ring detect function. In this case, RDI1 (Pin 3) and RDI2 (Pin 4) should be tied to V_{SS} and $\overline{RT}$ tied to V_{DD} as shown in Figure 6.

APPLICATION CIRCUIT



NOTE: C1 and C2 ≥ 0.2 µF required for line isolation. C1 through C4 are 250 V min, non–polarized.

Figure 7. Partial Implementation of PC Interface to Tip and Ring



NOTES:
1. Wired 'OR' $\overline{RDO}$ with $\overline{CDO}$.
2. Overlap of $\overline{RDO}$ edge with $\overline{CDO}$ edge to ensure part stays in $\overline{PWRUP}$ determined by RC time constant on $\overline{RDO}$, $\overline{PWRUP}$, and $\overline{CDO}$ pin.
3. Part reverts to $\overline{PWR\ ON}$, on rising edge of $\overline{RDO}$ since there is no $\overline{CDO}$.

Timing Diagram for Figure 7

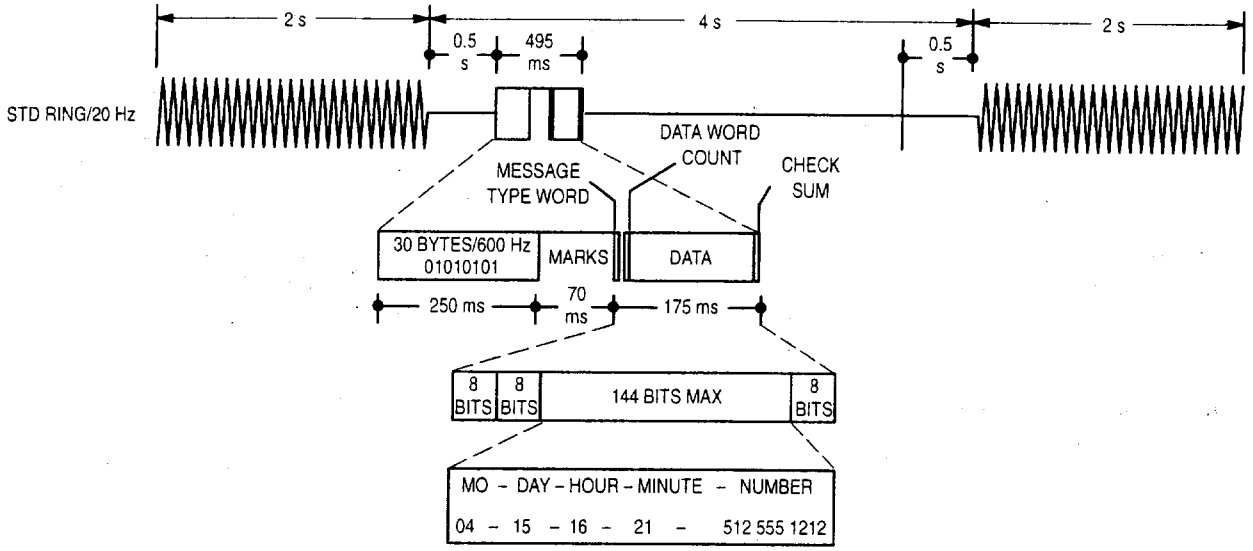


Figure 9. Single Message Format

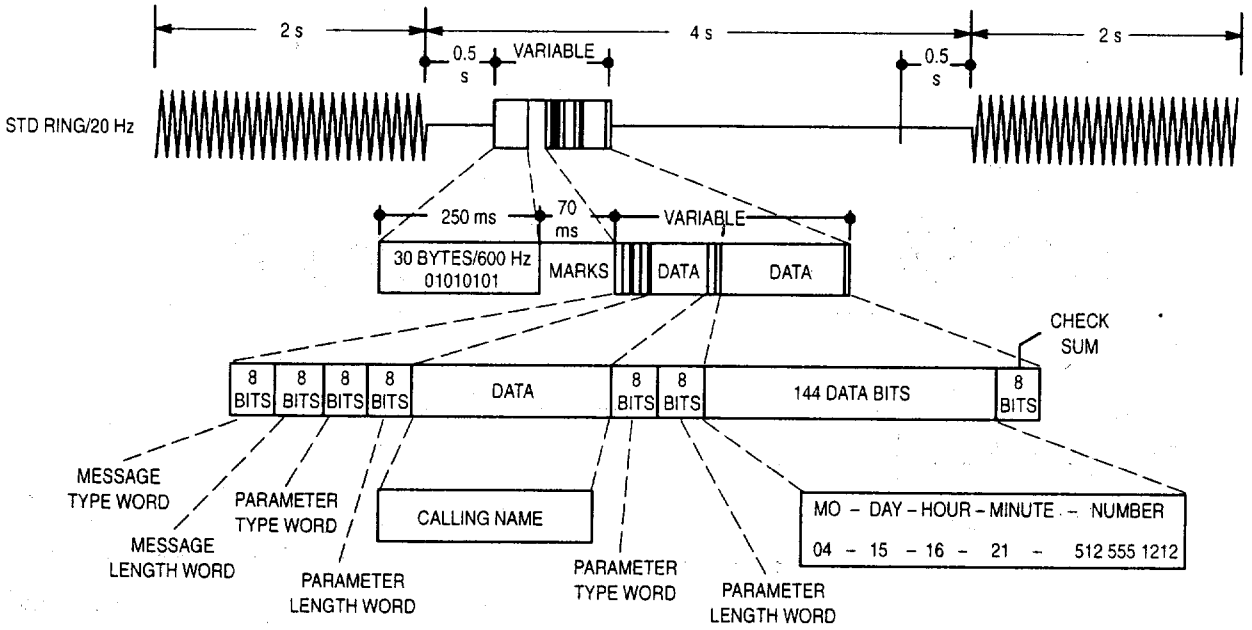


Figure 10. Multiple Message Format