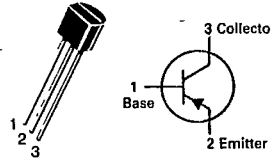


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2N5208CASE 29-04, STYLE 2
TO-92 (TO-226AA)**GENERAL PURPOSE
TRANSISTOR**

PNP SILICON

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	625 12	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA(1)}$	200	°C/W

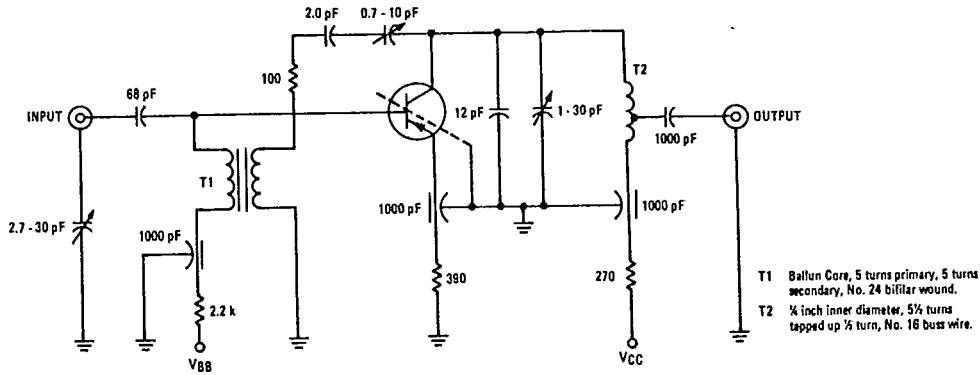
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	25	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 0.1$ mAdc, $I_E = 0$)	$V_{(BR)CBO}$	30	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10$ μ Adc, $I_C = 0$)	$V_{(BR)EBO}$	3.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 10$ Vdc, $I_E = 0$)	I_{CBO}	—	10	nAdc
Emitter Cutoff Current ($V_{BE} = 2.0$ Vdc, $I_C = 0$)	I_{EBO}	—	100	nAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc)	h_{FE}	20	120	—
Base-Emitter On Voltage ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc)	$V_{BE(on)}$	—	0.85	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc, $f = 100$ MHz)	f_T	300	1200	MHz
Input Capacitance ($V_{BE} = 2.0$ Vdc, $I_C = 0$, $f = 1.0$ MHz)	C_{ibo}	—	4.0	pF
Collector-Base Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f = 1.0$ MHz)	C_{cb}	—	1.0	pF
Collector Base Time Constant ($I_E = 2.0$ mAdc, $V_{CB} = 10$ Vdc, $f = 31.8$ MHz)	$rb'C_c$	—	10	ps
Noise Figure ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc, $R_S = 75$ ohms, $f = 100$ MHz, $BW = 1.0$ MHz)	NF	—	3.0	dB
FUNCTIONAL TEST				
Amplifier Power Gain ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc, $f = 100$ MHz)	G_{pe}	22	—	dB

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

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FIGURE 1 - 100 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT



T1 Ballun Core, 5 turns primary, 5 turns secondary, No. 24 bifilar wound.
T2 1/8 inch inner diameter, 5 1/2 turns tapped up 1/2 turn, No. 16 buss wire.

COMMON-EMITTER Y PARAMETERS (Polar Plots)
V_{CE} = 10 Vdc, T_A = 25°C

FIGURE 2 - INPUT ADMITTANCE

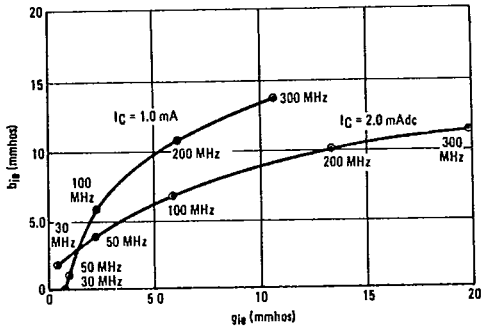


FIGURE 3 - OUTPUT ADMITTANCE

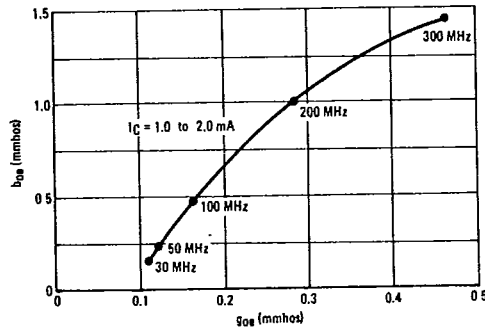


FIGURE 4 - FORWARD TRANSFER ADMITTANCE

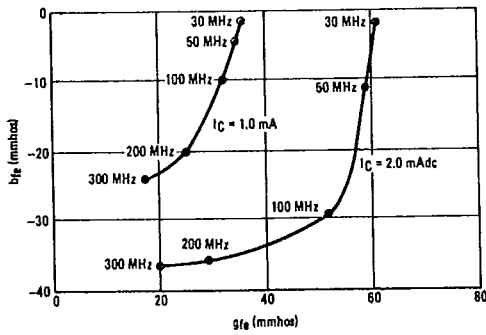
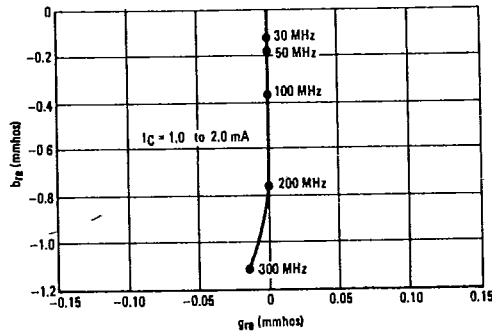


FIGURE 5 - REVERSE TRANSFER ADMITTANCE



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STABILITY FACTOR CURVE

FIGURE 6 - POWER GAIN AND NOISE FIGURE

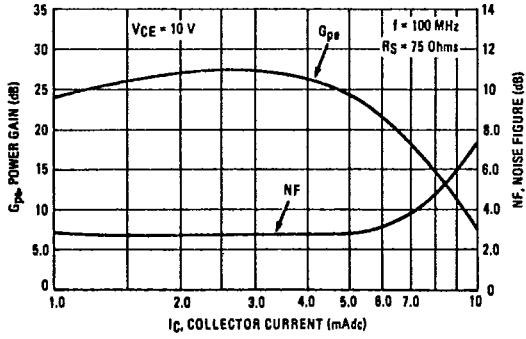
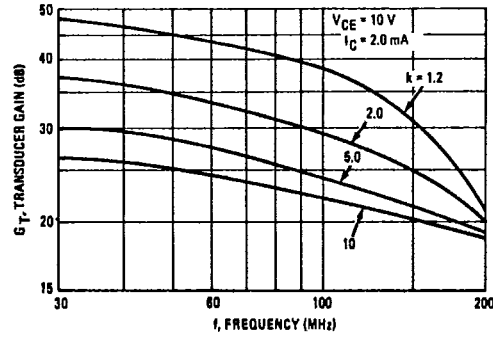


FIGURE 7 - MAXIMUM TRANSDUCER GAIN



COMMON-EMITTER Y PARAMETERS vs FREQUENCY

$V_{CE} = 10\text{ Vdc}$, $T_A = 25^\circ\text{C}$

FIGURE 8 - INPUT ADMITTANCE

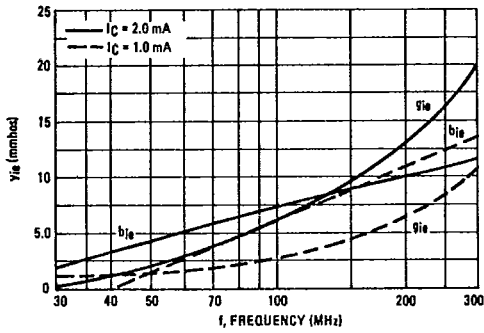


FIGURE 9 - OUTPUT ADMITTANCE

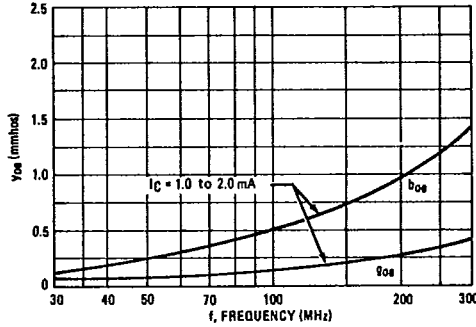


FIGURE 10 - FORWARD TRANSFER ADMITTANCE

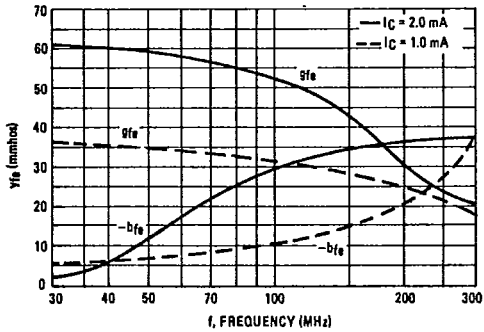
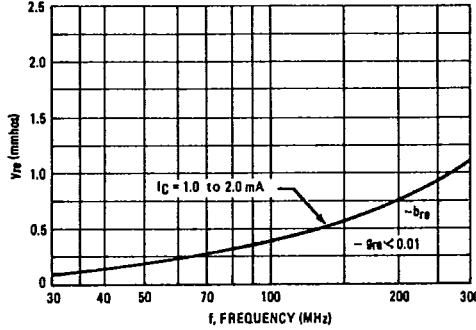


FIGURE 11 - REVERSE TRANSFER ADMITTANCE



STABILITY FACTOR CURVES

FIGURE 12 - OPTIMUM SOURCE ADMITTANCE

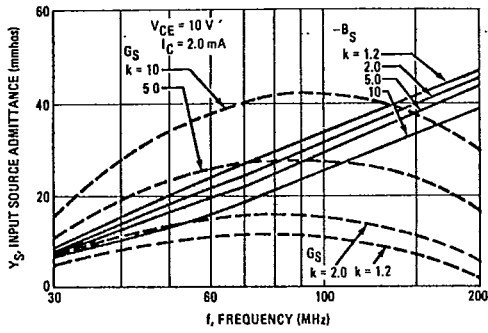
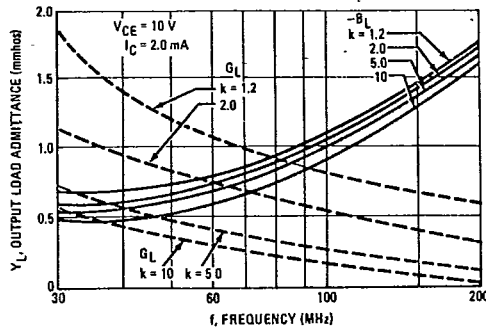


FIGURE 13 - OPTIMUM LOAD ADMITTANCE



When a potentially unstable device is operated without feedback, there is an infinite number of combinations of source and load admittance associated with any given circuit stability factor (k). Equations have been developed for determining the optimum source and load admittance for maximum gain. Figures 7, 12 and 13 provide a solution to the equations for the 2N5208.

NOISE FIGURE

FIGURE 14 - FREQUENCY EFFECTS

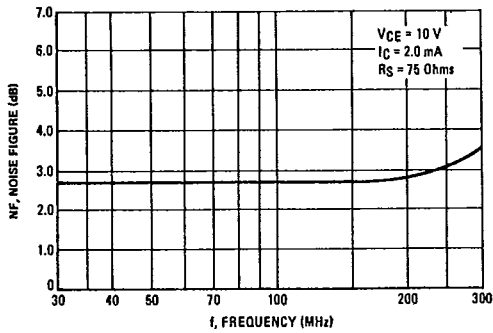


FIGURE 15 - SOURCE RESISTANCE EFFECTS

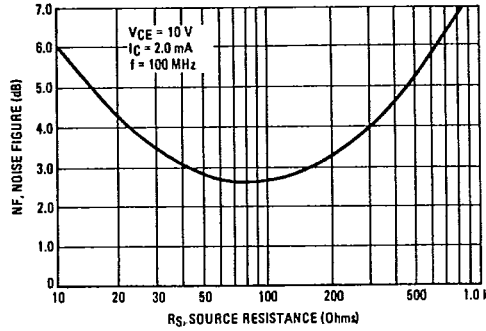


FIGURE 16 - CURRENT-GAIN — BANDWIDTH PRODUCT

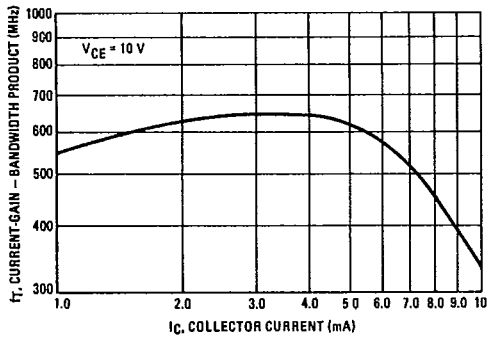
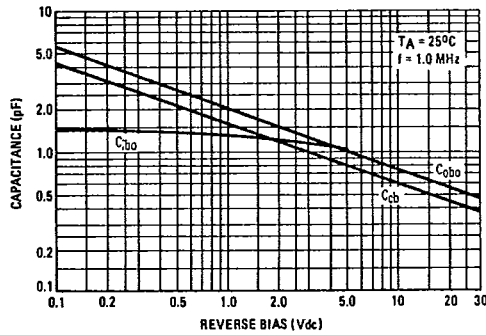


FIGURE 17 - CAPACITANCES



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FIGURE 18 - DC CURRENT GAIN

