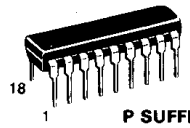
MC14499

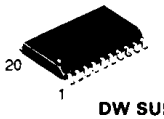
7-Segment LED Display Decoder/ Driver with Serial Interface
CMOS

The MC14499 is a 7-segment alphanumeric LED decoder/driver with a serial interface port to provide communication with CMOS microprocessors and microcomputers. This device features NPN output drivers which allow interfacing to common cathode LED displays through external series resistors.

- High-Current Segment Drivers on Chip
- CMOS MPU Compatible Input Levels
- Wide Operating Voltage Range: 4.5 to 6.5 V
- Operating Temperature Range: 0 to 70°C
- Drives Four Characters with Decimal Points
- Also See MC14489



P SUFFIX
PLASTIC DIP
CASE 707

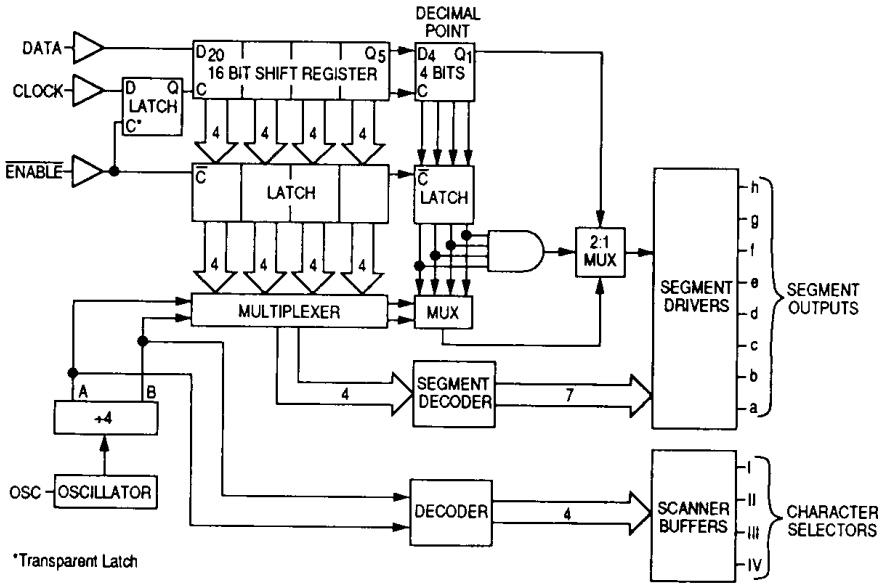


DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

MC14499P	Plastic DIP
MC14499DW	SOG Package

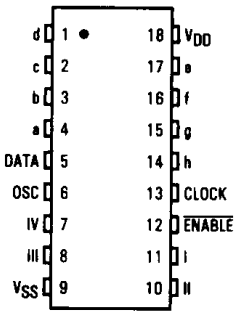
BLOCK DIAGRAM



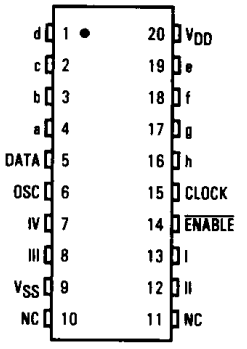
*Transparent Latch

PIN ASSIGNMENTS

PLASTIC DIP



SOG PACKAGE



NC = NO CONNECTION

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +7.0	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
Storage Temperature Range	T_{stg}	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics table or Circuit Operation section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

3

ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 6.5 V)

Characteristic		Symbol	0°		25°		70°		Unit
			Min	Max	Min	Max	Min	Max	
Serial Port Input Voltage	'0' Level	V_{IL}	–	0.3 × V_{DD}	–	0.3 × V_{DD}	–	0.3 × V_{DD}	V
	'1' Level	V_{IH}	0.7 × V_{DD}	–	0.7 × V_{DD}	–	0.7 × V_{DD}	–	
Serial Port Input Current (V_{in} = 0 to V_{DD})		I_{in}	–	±0.1	–	±0.1	–	±1.0	μA
Oscillator Input Voltage	'0' Level	V_{IL}	–	0.25 × V_{DD}	–	0.25 × V_{DD}	–	0.2 × V_{DD}	V
	'1' Level	V_{IH}	0.75 × V_{DD}	–	0.75 × V_{DD}	–	0.8 × V_{DD}	–	
Oscillator Input Current	V_{OSC} = 0	I_{IL}	–	100	30	80	10	–	μA
	V_{OSC} = V_{DD}	I_{IH}	–	−100	−30	−80	−10	–	
Segment Driver Voltage Below V_{DD}									V
I_{out} = 50 mA		ΔV_{OH}	–	1.1	–	1.0	–	1.1	
I_{out} = 10 mA			–	0.8	–	0.75	–	0.8	
Segment Driver Off Leakage	V_{out} = 0	I_{OZ}	–	100	–	50	–	100	μA
Digit Drivers									mA
Source (On)	V_{out} = 0.8 V	I_{OH}	6	–	5.5	–	4	–	
Sink (Off)	V_{out} = 0.5 V	I_{OL}	−0.2	–	−0.2	–	−0.1	–	
Supply Current V_{in} = 0, I_{out} = 0, C_{OSC} = 0.015 μF		I_{DD}	–	1	–	1	–	1	mA
Maximum Power Dissipation		P_D	–	500	–	500	–	500	mW

SWITCHING CHARACTERISTICS (V_{DD} = 5 V ±10%, T_A = 0 to 70°C)

Characteristic	Fig	Symbol	Min	Max	Unit
Clock High Time	2	t_{CH}	2		μs
Clock Low Time	2	t_{CL}	2		μs
Clock Rise Time	2	t_{CR}		2	μs
Clock Fall Time	2	t_{CF}		2	μs
Enable Lead Time	2	$t_{E\ LEAD}$	200		ns
Enable Lag Time	2	$t_{E\ LAG}$	200		ns
Data Set-Up Time	2	$t_{D\ SUP}$	200		ns
Data Hold Time	2	$t_{D\ HOLD}$	1		μs
Scanner Frequency*	4	$1/t_{SCAN}$	50	300	Hz
OSC/Digit Lead Time	4	t_{OD}		10	μs
OSC/Segment Lead Time	4	t_{OS}		10	μs
Digit Overlap	4	t_{OV}		5	μs

*Scanner Capacitance = 0.022 μF.

CIRCUIT OPERATION

The circuit accepts a 20-bit input, 16 bits for the four digit display plus 4 bits for the decimal point—these latter four bits are optional.

The input sequence is the decimal point code followed by the four digits, as shown in Figure 1.

In order to enter data the enable input, $\overline{\text{ENABLE}}$, must be active low. The sample and shift are accomplished on the falling clock edge, see Figure 2. Data are loaded from the shift register to the latches when $\overline{\text{ENABLE}}$ goes high. While the shift register is being loaded the previous data are stored in the latches.

If the decimal point is used, the system requires 20 clock pulses to load data; otherwise only 16 are required.

CASCADING

The circuit may be cascaded in the following manner.

If a 1111 word is loaded into the decimal point latch, the output of the shift register is switched to the decimal point driver, see Figure 3. Therefore, to cascade n four digit display drivers a set-up is used which loads the 1111 cascading word:

1. $\overline{\text{ENABLE}}$ = active low.
2. Load 20-bits, the first four bits being 1, with 20 clock pulses.
3. $\overline{\text{ENABLE}}$ = high, to load the latch.
4. Repeat steps 1 to 3 (n-1) times.
5. (n × 20)-bits can be loaded into n circuits, with 1111 as decimal point word to continue the cascading.

SCANNER

The scanner frequency is determined by an on-chip oscillator, which requires an external frequency-determining capacitor. The capacitor voltage varies between two trigger levels at the oscillator frequency.

An external oscillator signal can be used, within the recommended operating range of 200 to 800 Hz. For test purposes this frequency may be increased up to 10 kHz.

A divide by four counter provides four non-overlapping scanner waveforms corresponding to the four digits—see Figure 4.

SEGMENT DECODER

The code used in this matrix decoders is shown in Figure 5.

OUTPUT DRIVERS

There are two different drivers:

- The segment and decimal point drivers; these are NPN emitter followers with no current limiting devices.
- The digit output buffers; these are short-circuit protected CMOS devices.

A typical application circuit is shown in Figure 6.

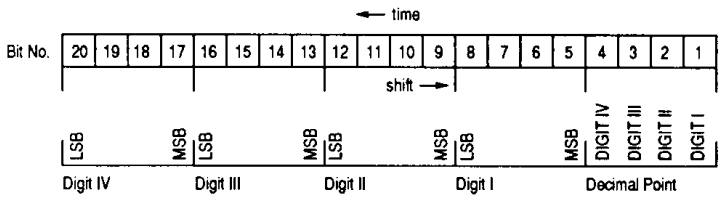


Figure 1. Input Sequence

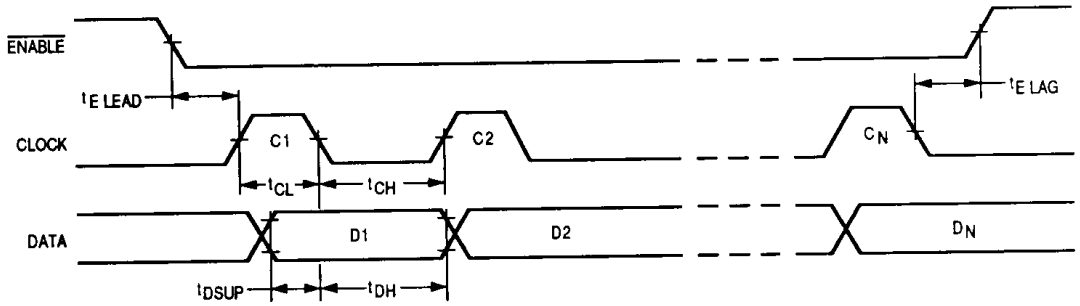


Figure 2a. Serial Input, Positive Clock

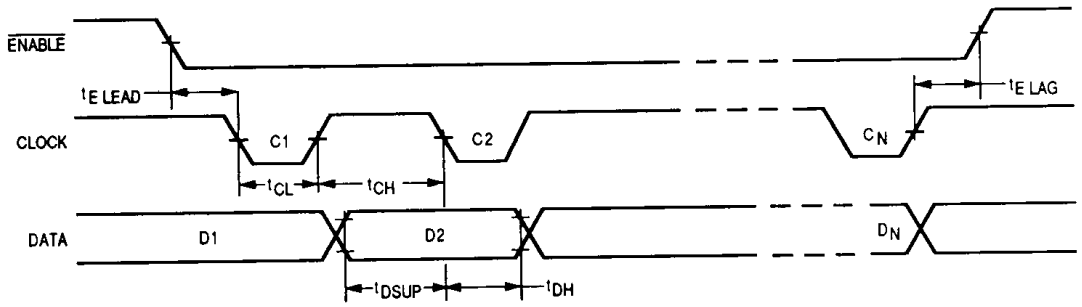


Figure 2b. Serial Input, Negative Clock

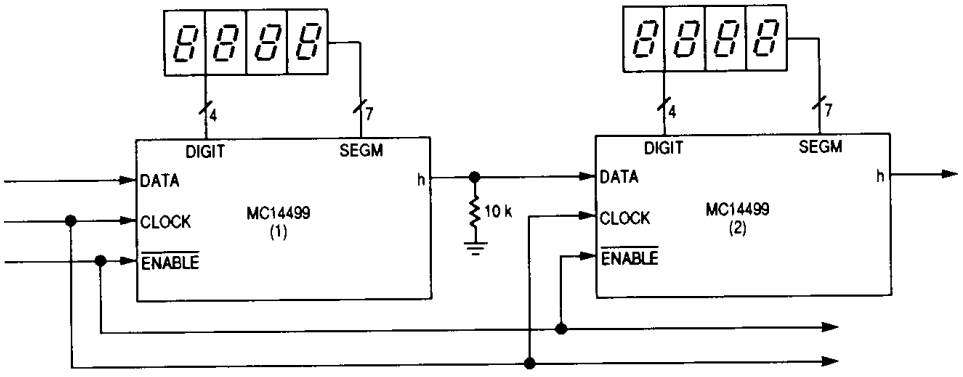


Figure 3. Cascading MC14499s

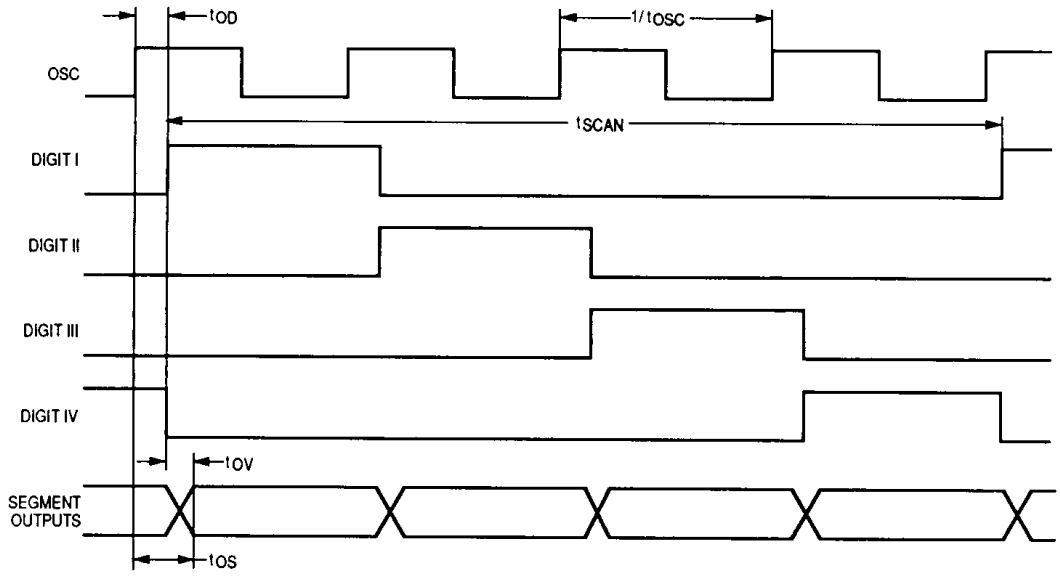


Figure 4. Scanner Waveforms

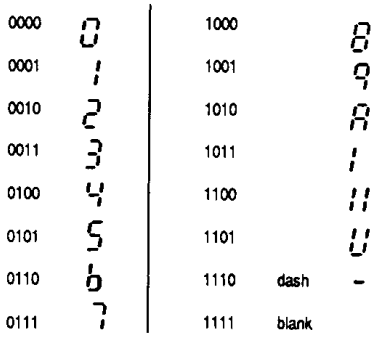


Figure 5. Segment Code

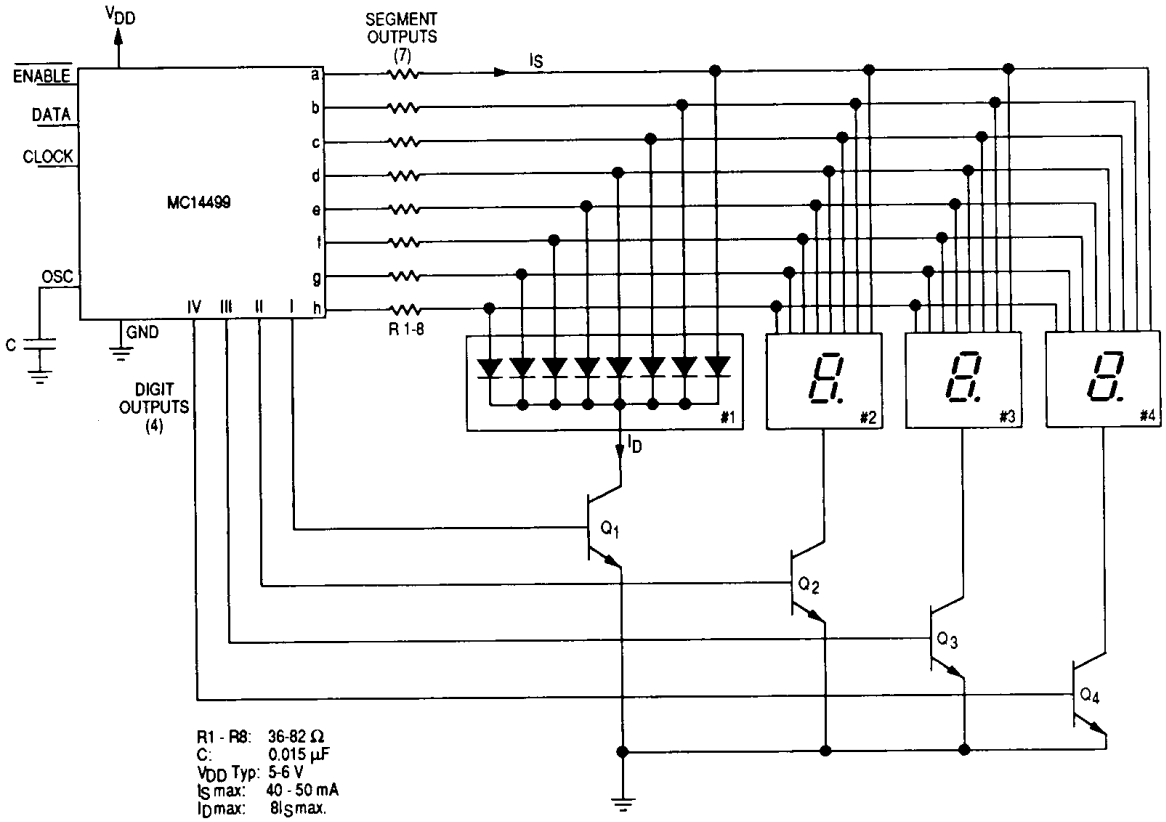


Figure 6. Application Example