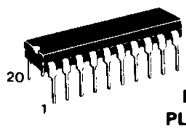
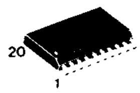
MC14489

Advance Information

Multi-Character LED Display/Lamp Driver
CMOS



P SUFFIX
PLASTIC DIP
CASE 738

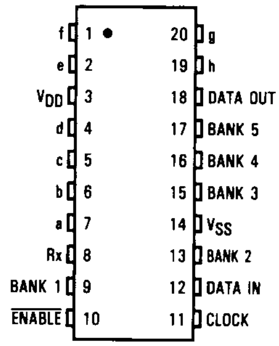


DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

MC14489P	Plastic DIP
MC14489DW	SOG Package

PIN ASSIGNMENT

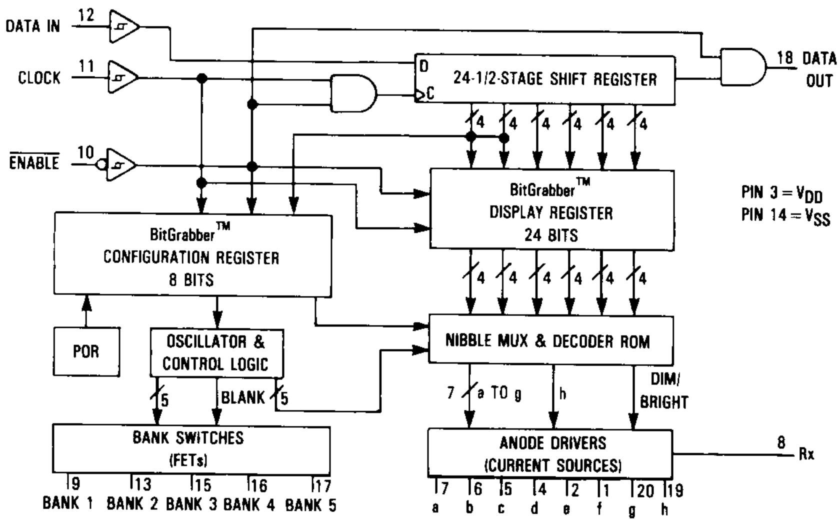


The MC14489 is a flexible light-emitting-diode driver which directly interfaces to individual lamps, 7-segment displays, or various combinations of both. LEDs wired with common cathodes are driven in a muliplexed-by-5 fashion. Communication with an MCU/MPU is established through a synchronous serial port. The MC14489 features data retention plus decode and scan circuitry, thus relieving processor overhead. A single, current-setting resistor is the only ancillary component required.

A single device can drive any one of the following: a 5-digit display plus decimals, a 4 1/2-digit display plus decimals and sign, or 25 lamps. A special technique allows driving 5 1/2 digits; see Figure 16. A configuration register allows the drive capability to be partitioned off to suit many additional applications. The on-chip decoder outputs 7-segment-format numerals 0 to 9, hexadecimal characters A to F, plus 15 letters and symbols.

The MC14489 is compatible with the Motorola/RCA SPI and National MICROWIRE serial data ports. The chip's new BitGrabber registers augment the serial interface by allowing random access without steering or address bits. A 24-bit transfer updates the display register. Changing the configuration register requires an 8-bit transfer.

- Operating Voltage Range of Drive Circuitry: 4.5 to 6 V
- Operating Junction Temperature Range: − 40° to 130°C
- Current Sources Controlled by Single Resistor Provide Anode Drive
- Low-Resistance FET Switches Provide Direct Common Cathode Interface
- Low-Power Mode (Extinguishes the LEDs) and Brightness Controlled Via Serial Port
- Special Circuitry Minimizes EMI when Display is Driven and Eliminates EMI in Low-Power Mode
- Power-On Reset (POR) Blanks the Display on Power Up
- May Be Used with the New Double-Heterojunction LEDs for Optimum Efficiency
- Chip Complexity: 4300 Elements (FETs, Resistors, Capacitors, etc.)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS* (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current—per Pin (includes Pin 8)	±15	mA
I_{out}	DC Output Current—Pins 1, 2, 4-7, 19, 20 Sourcing Sinking	−40 10	mA
	Pins 9, 13, 15, 16, 17 Sinking	320	
	Pin 18	±15	
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	±350	mA
T_J	Chip Junction Temperature	−40 to +130	°C
$R_{\theta JA}$	Device Thermal Resistance, Junction-to-Ambient (see Thermal Considerations section) Plastic DIP SOG	90 100	°C/W
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_J = −40° to 130°C* unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range of LED Drive Circuitry		—	4.5 to 6.0	V
V_{DD} (stby)	Minimum Standby Voltage	Bits Retained in Display and Configuration Registers, Data Port Fully Functional	—	3.0	V
V_{IL}	Maximum Low-Level Input Voltage (Data In, Clock, $\overline{Enable}$)		3.0 6.0	0.9 1.8	V
V_{IH}	Minimum High-Level Input Voltage (Data In, Clock, $\overline{Enable}$)		3.0 6.0	2.1 4.2	V
V_{Hys}	Minimum Hysteresis Voltage (Data In, Clock, $\overline{Enable}$)		3.0 6.0	0.2 0.4	V
V_{OL}	Maximum Low-Level Output Voltage (Data Out)	I_{out} = 20 µA	3.0 6.0	0.1 0.1	V
		I_{out} = 1.3 mA	4.5	0.4	
V_{OH}	Minimum High-Level Output Voltage (Data Out)	I_{out} = −20 µA	3.0 6.0	2.9 5.9	V
		I_{out} = −800 µA	4.5	4.1	
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{Enable}$)	V_{in} = V_{DD} or V_{SS}	6.0	±2.0	µA
		V_{in} = V_{DD} or V_{SS}, T_J = 25°C only	6.0	±0.1	
I_{OL}	Minimum Sinking Current (a, b, c, d, e, f, g, h)	V_{out} = 1.0 V	4.5	0.2	mA
I_{OH}	Peak Sourcing Current (See Fig. 9 for currents up to 35 mA) (a, b, c, d, e, f, g, h)	Rx = 2.0 kΩ, V_{out} = 3.0 V, Dimmer Bit = High	5.0	13 to 17.5	mA
		Rx = 2.0 kΩ, V_{out} = 3.0 V, Dimmer Bit = Low	5.0	6 to 9	
I_{OZ}	Maximum Output Leakage Current (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5)	V_{out} = V_{DD} (FET Leakage)	6.0	50	µA
		V_{out} = V_{DD} (FET Leakage), T_J = 25°C only	6.0	1	
		V_{out} = V_{SS} (Protection Diode Leakage)	6.0	1	
R_{on}	Maximum ON Resistance (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5)	I_{out} = 0 to 200 mA	5.0	10	Ω
I_{DD}, I_{SS}	Maximum Quiescent Supply Current	Device in Low-Power Mode, V_{in} = V_{SS} or V_{DD}, Rx in Place, Outputs Open	6.0	100	µA
		Same as Above, T_J = 25°C	6.0	20	
I_{ss}	Maximum RMS Operating Supply Current (The V_{SS} leg does not contain the Rx current component. See Pin Descriptions.)	Device NOT in Low-Power Mode, V_{in} = V_{SS} or V_{DD}, Outputs Open	6.0	1.5	mA

*See Thermal Considerations section.

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AC ELECTRICAL CHARACTERISTICS ($T_J = -40°$ to 130°C★, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency, Single Device or Cascaded Devices NOTE: Refer to Clock t_w below (Figure 1)	3.0 4.5 6.0	dc to 3.0 dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Data Out (Figures 1 and 5)	3.0 4.5 6.0	140 80 80	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Data Out (Figures 1 and 5)	3.0 4.5 6.0	70 50 50	ns
f_R	Refresh Rate—Bank 1 through Bank 5 (Figures 2 and 6)	3.0 4.5 6.0	NA 700 to 1900 700 to 1900	Hz
C_{in}	Maximum Input Capacitance—Data In, Clock, $\overline{\text{Enable}}$	—	10	pF

★See Thermal Considerations section.

TIMING REQUIREMENTS ($T_J = -40°$ to 130°C★, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	3.0 4.5 6.0	50 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold,* and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	3.0 4.5 6.0	150 100 100	ns
$t_{w(L)}$	Minimum Active-Low Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	3.0 4.5 6.0	4.5 3.4 3.4	μs
$t_{w(H)}$	Minimum Inactive-High Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	3.0 4.5 6.0	300 150 150	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	3.0 4.5 6.0	167 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times—Data In, Clock, $\overline{\text{Enable}}$ (Figure 1)	3.0 4.5 6.0	1 1 1	ms

★See Thermal Considerations section.

*For a high-speed 8-Clock access, t_h for $\overline{\text{Enable}}$ is determined as follows.
$V_{DD} = 3$ to 4.5 V, $f_{clk} > 1.78$ MHz: $t_h = 4350 - (7500/f_{clk})$
$V_{DD} = 4.5$ to 6 V, $f_{clk} > 2.34$ MHz: $t_h = 3300 - (7500/f_{clk})$
where t_h is in ns and f_{clk} is in MHz.

NOTES:
1. This restriction does NOT apply for f_{clk} rates less than those listed above. For "slow" f_{clk} rates, use the t_h limits in the above table.
2. This restriction does NOT apply for an access involving more than 8 Clocks. For >8 Clocks, use the t_h limits in the above table.

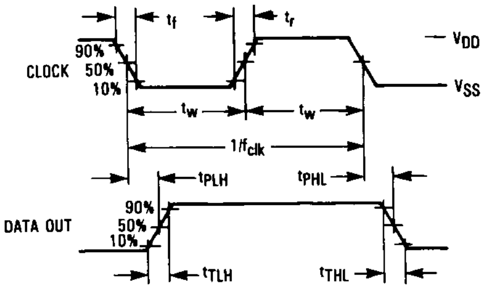


Figure 1

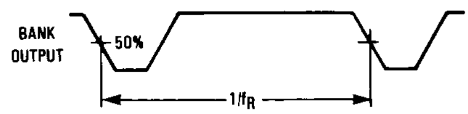


Figure 2

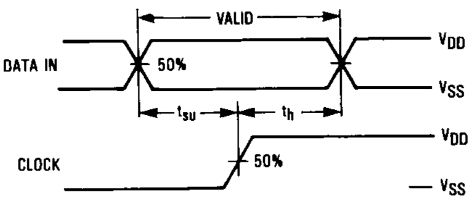


Figure 3

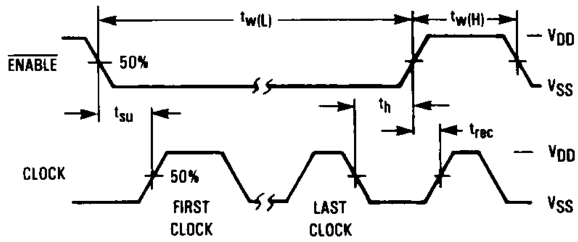
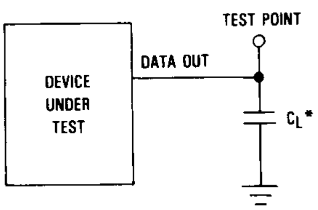
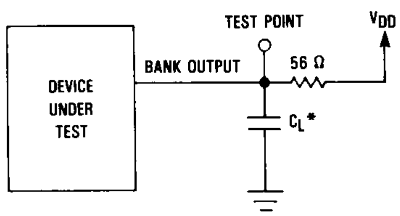


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE

Data In (Pin 12)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low-to-high transition of Clock. When the device is not cascaded, the bit pattern is either 1 byte (8 bits) long to change the configuration register or 3 bytes (24 bits) long to update the display register. For two chips cascaded, the pattern is either 4 or 6 bytes, respectively. The display does not flicker during shifting which allows slow serial data rates, if desired.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the two registers. Random access of either register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 3 to 6 V. The format is shown in Figures 7 and 8. Information on the segment decoder is given in Table 1.

Data In typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. These features combine to maximize noise immunity for use in harsh environments and bus applications. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC14504B, MC74HCT04A) or pullup resistor of 1 kΩ to 10 kΩ must be used. Parameters to be considered when sizing the resistor are the worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Clock (Pin 11)

Serial Data Clock Input. Low-to-high transitions on Clock shift bits available at Data In, while high-to-low transitions shift bits from Data Out. The chip's 24-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode. The Clock input does not need to be synchronous with the on-chip clock oscillator which drives the multiplexing circuit.

Eight clock cycles are required to access the configuration register, while 24 are needed for the display register when the MC14489 is not cascaded. See Figures 7 and 10.

As shown in Figure 11, two devices may be cascaded. In this case, 32 clock cycles access the configuration register and 48 access the display register, as depicted in Figure 8.

Cascading of 3, 4, and 5 devices is shown in Figures 12, 13, and 14, respectively.

Clock typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow Clock rise and fall times are tolerated. See the last paragraph of **Data In** for more information.

$\overline{\text{Enable}}$ (Pin 10)

Active-Low Enable Input. This pin allows the MC14489 to be used on a serial bus, sharing Data In and Clock with other peripherals. When $\overline{\text{Enable}}$ is in an inactive high state, Data Out is forced to a known (low) state, shifting is inhibited, and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which initially must be inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken high. The low-to-high transition on $\overline{\text{Enable}}$ transfers data to either the configuration or display register, depending on the data stream length.

CAUTION

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data in the registers. See the last paragraph of **Data In** for more information.

Data Out (Pin 18)

Serial Data Output. Data is transferred out of the shift register through Data Out on the high-to-low transition of Clock. This output is a no connect, unless used in one of the manners discussed below.

When cascading MC14489s, Data Out feeds Data In of the next device per Figures 11, 12, 13, and 14.

Data Out could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, pc board traces, solder joints, etc.

The pin could be monitored at an in-line Q.A. test during board manufacturing.

Finally, Data Out facilitates troubleshooting a system.

DISPLAY INTERFACE

Rx (Pin 8)

External Current-Setting Resistor. A resistor tied between this pin and ground (V_{SS}) determines the peak segment drive current delivered at pins a through h. Pin 8's resistor ties into a current mirror with an approximate current gain of 10 when bit D23 = high (brighten). With D23 = low, the peak current is reduced about 50%. Values for Rx range from 700 Ω to infinity. When Rx = ∞ (open circuit), the display is extinguished. For proper current control, resistors having ± 1% tolerance should be used. See Figure 9.

CAUTION

Small Rx values may cause the chip to overheat if precautions are not observed. See **THERMAL CONSIDERATIONS.**

a through h (Pins 1, 2, 4-7, 19, 20)

Anode-Driver Current Sources. These outputs are closely-matched current sources which directly tie to the anodes of external discrete LEDs (lamps) or display segment LEDs.

When used with lamps, outputs a, b, c, and d are used to independently control up to 20 lamps. Output h is used to control up to 5 lamps dependently. (See Figure 17.) For lamps, the *No Decode* mode is selected via the configuration register, forcing e, f, and g inactive (low).

When used with segmented displays, outputs a through g drive segments a through g, respectively. Output h is used to drive the decimals. If unused, h must be left open. Refer to Figure 10.

Bank 1 through Bank 5 (Pins 9, 13, 15, 16, 17)

Diode-Bank FET Switches. These outputs are low-resistance switches to ground (V_{SS}) capable of handling currents of up to 320 mA. These pins directly tie to the common cathodes of segmented displays or the cathodes of lamps (wired with cathodes common).

The display is refreshed at a nominal 1 kHz rate to achieve optimum brightness from the LEDs. A 20% duty cycle is utilized.

Special design techniques are used on-chip to accommodate the high currents with low EMI (electromagnetic interference) and minimal spiking on the power lines.

POWER SUPPLY

V_{SS} (Pin 14)

Most-negative supply potential. This pin is usually ground. Resistor Rx is externally tied to ground (V_{SS}). Therefore, the chip's V_{SS} pin does not contain the Rx current component.

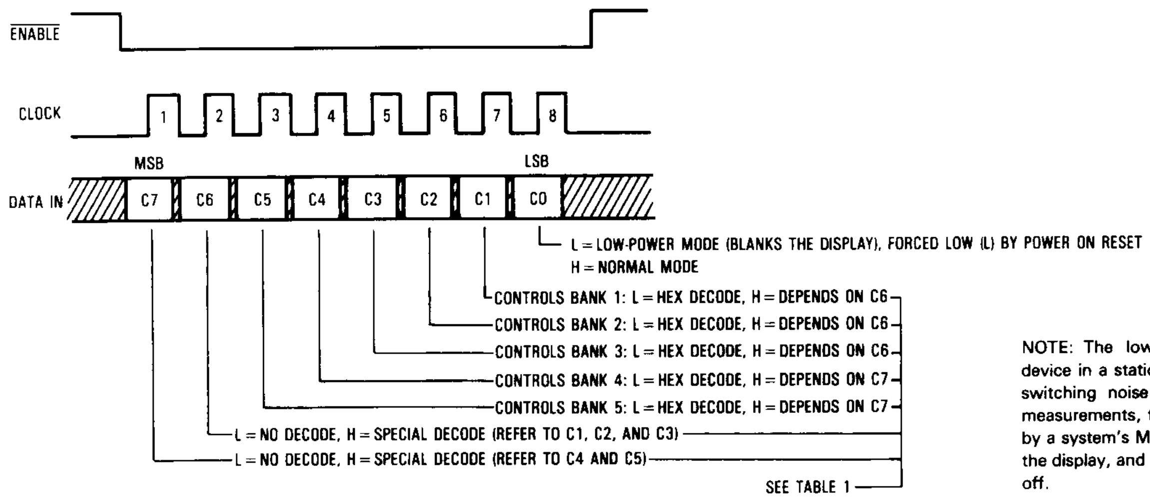
V_{DD} (Pin 3)

Most-positive supply potential.

To guarantee data integrity in the registers and to ensure the serial interface is functional, this voltage may range from 3 to 6 volts with respect to V_{SS}. For example, within this voltage range, the chip could be placed in and out of the low-power mode.

To adequately drive the LEDs, this voltage must be 4.5 to 6 volts with respect to V_{SS}.

The V_{DD} pin contains the Rx current component plus the chip's current drain. In the low-power mode, the current mirror and clock oscillator are turned off, thus significantly reducing the V_{DD} current, I_{DD}.



NOTE: The low-power (standby) mode places the device in a static state, thus eliminating EMI and mux switching noise. Therefore, during precision analog measurements, the low-power mode could be invoked by a system's MCU. Also, the low-power mode blanks the display, and could be used to flash the LEDs on and off.

Figure 7a. Configuration Register Format (1 Byte)

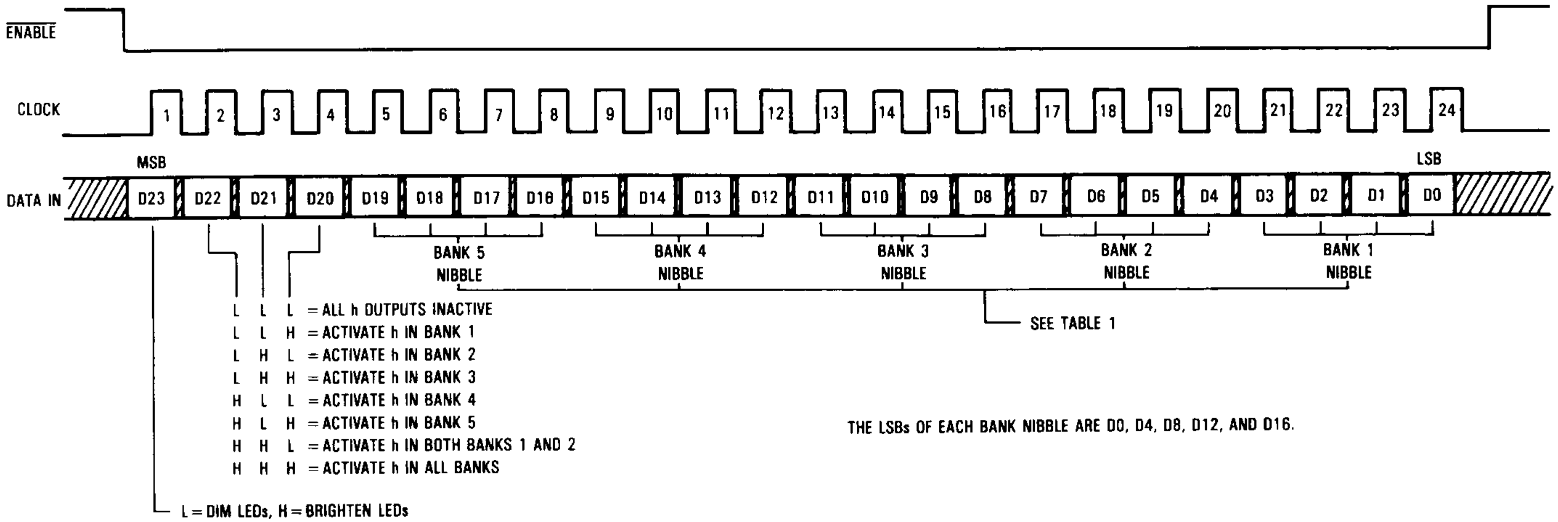


Figure 7b. Display Register Format (3 Bytes)

NOTE: L = Low Voltage Level (Logic 0), H = High Voltage Level (Logic 1)

Figure 7. Timing Diagrams for Non-Cascaded Devices

Table 1. Triple-Mode Segment Decoder Function Table

Bank Nibble Value		7-Segment Display Characters		Lamp Conditions: No Decode (1) (Invoked via Bits C1 to C7)			
Hexadecimal	Binary MSB LSB	Hex Decode (Invoked via Bits C1 to C5)	Special Decode (Invoked via Bits C1 to C7)	d	c	b	a
$0	L L L L	0					
$1	L L L H	1	c				on
$2	L L H L	2	H			on	
$3	L L H H	3	h			on	on
$4	L H L L	4	J		on		
$5	L H L H	5 (2)	L		on		on
$6	L H H L	6	n		on	on	
$7	L H H H	7	o		on	on	on
$8	H L L L	8 (3)	P	on			
$9	H L L H	9 (4)	r	on			on
$A	H L H L	A	U	on		on	
$B	H L H H	b	u	on		on	on
$C	H H L L	C	y	on	on		
$D	H H L H	d	-	on	on		on
$E	H H H L	E	=	on	on	on	
$F	H H H H	F	°	on	on	on	on

(1) In the *No Decode* mode, outputs e, f, and g are unused and are all forced inactive (low). Output h's decoding is unaffected, i.e., unchanged from the other modes. The *No Decode* mode is used for three purposes:

1. Individually controlling lamps.
2. Controlling a half digit with sign.
3. Controlling annunciators—examples: AM, PM, UHF, kV, mm Hg.

(2) Can be used as "cap S".

(3) Can be used as "cap B".

(4) Can be used as "small g".

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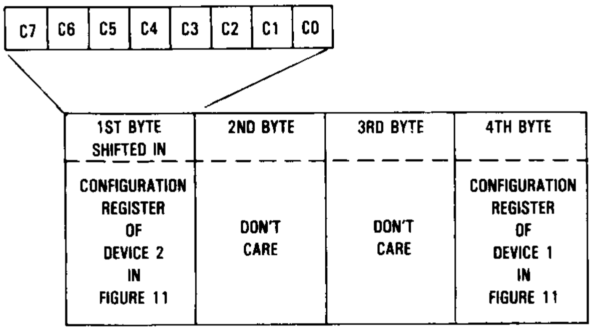

Figure 8a. Configuration Registers

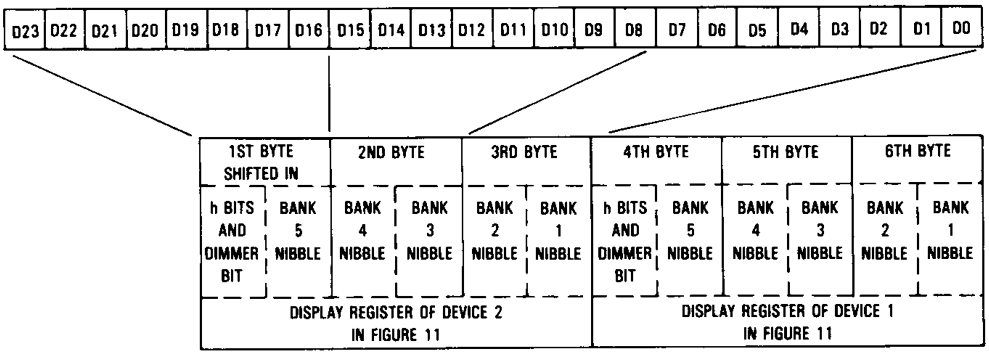

Figure 8b. Display Registers

NOTE: $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active-low during the entire 4-byte configuration transfer or 6-byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either a 4- or 6-byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

Figure 8. Bit Stream Formats for Two Devices Cascaded

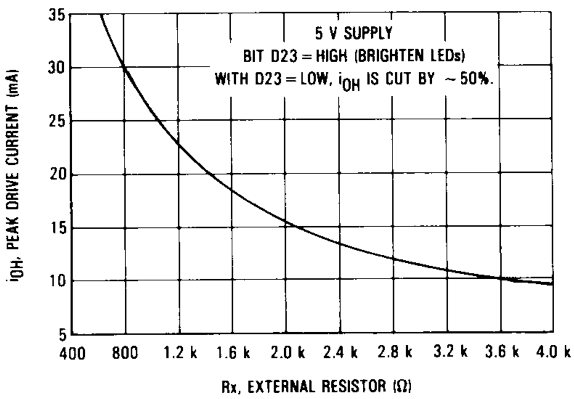

Figure 9. a through h Nominal Current versus Rx

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APPLICATIONS INFORMATION

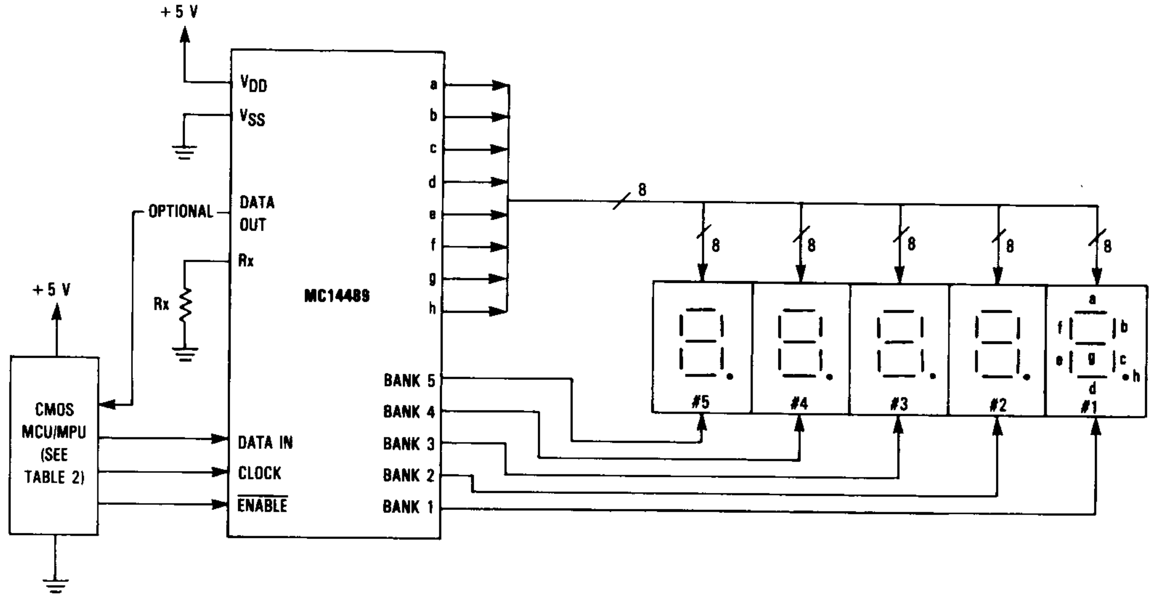


Figure 10. Non-Cascaded Application Example: 5 Character Common Cathode LED Display with Two Intensities as Controlled via Serial Port

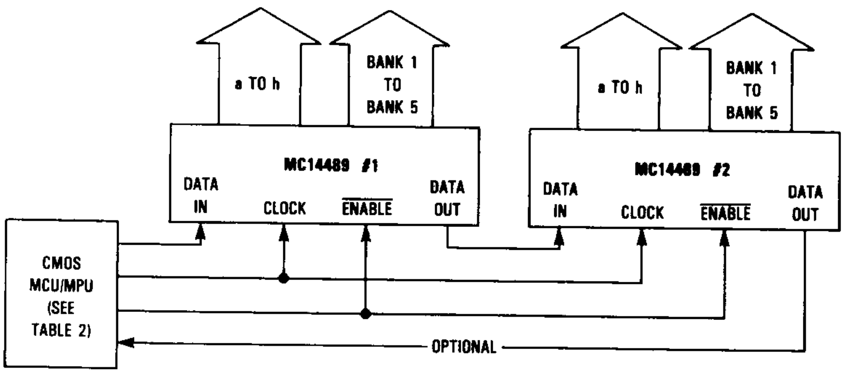


Figure 11. Cascading Two Devices

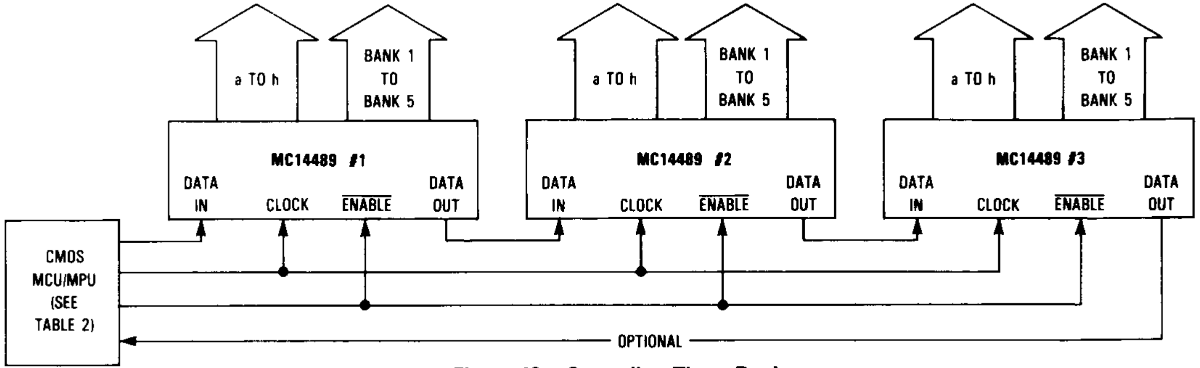


Figure 12a. Cascading Three Devices

C7	C6	C5	C4	C3	C2	C1	C0

1ST BYTE SHIFTED IN	2ND BYTE	3RD BYTE	4TH BYTE	5TH BYTE	6TH BYTE	7TH BYTE	8TH (LAST) BYTE
DON'T CARE	CONFIGURATION REGISTER OF DEVICE #3	DON'T CARE	DON'T CARE	CONFIGURATION REGISTER OF DEVICE #2	DON'T CARE	DON'T CARE	CONFIGURATION REGISTER OF DEVICE #1

Figure 12b. Configuration Registers

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

1ST BYTE SHIFTED IN	2ND BYTE		3RD BYTE		4TH BYTE		5TH BYTE		6TH BYTE		7TH BYTE		8TH BYTE		9TH BYTE		10TH (LAST) BYTE	
DON'T CARE (OPTIONAL, SEE NOTE.)	h BITS AND DIMMER BIT	BANK 5 NIBBLE	BANK 4 NIBBLE	BANK 3 NIBBLE	BANK 2 NIBBLE	BANK 1 NIBBLE	h BITS AND DIMMER BIT	BANK 5 NIBBLE	BANK 4 NIBBLE	BANK 3 NIBBLE	BANK 2 NIBBLE	BANK 1 NIBBLE	h BITS AND DIMMER BIT	BANK 5 NIBBLE	BANK 4 NIBBLE	BANK 3 NIBBLE	BANK 2 NIBBLE	BANK 1 NIBBLE
	DISPLAY REGISTER OF DEVICE #3						DISPLAY REGISTER OF DEVICE #2						DISPLAY REGISTER OF DEVICE #1					

Figure 12c. Display Registers

NOTE: When the "don't care" bytes are included, $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active-low during the entire 8-byte configuration transfer or 10-byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either an 8- or 10-byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the one "don't care" byte can be eliminated as follows: (1) take $\overline{\text{ENABLE}}$ active low, (2) transfer 6 bytes, (3) pulse $\overline{\text{ENABLE}}$ inactive high, see $t_{w(H)}$ spec, (4) transfer last 3 bytes, and (5) take $\overline{\text{ENABLE}}$ inactive high.

Figure 12. Bit Stream Formats for Three Devices Cascaded

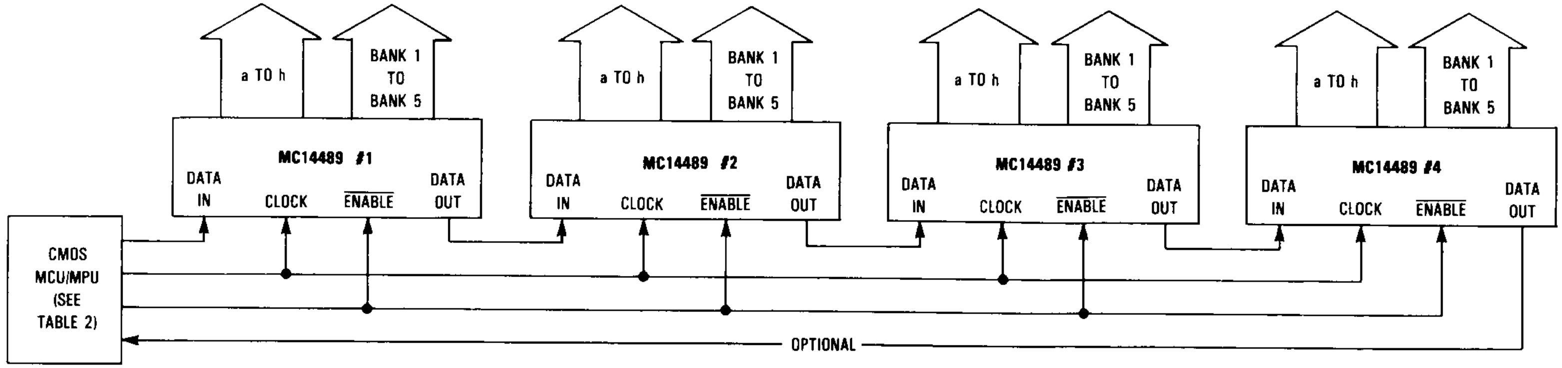


Figure 13a. Cascading Four Devices

C7	C6	C5	C4	C3	C2	C1	C0

1ST BYTE SHIFTED IN	2ND BYTE SHIFTED IN	3RD BYTE	4TH BYTE	5TH BYTE	6TH BYTE	7TH BYTE	8TH BYTE	9TH BYTE	10TH BYTE	11TH BYTE	12TH (LAST) BYTE
DON'T CARE	DON'T CARE	CONFIGURATION REGISTER OF DEVICE #4	DON'T CARE	DON'T CARE	CONFIGURATION REGISTER OF DEVICE #3	DON'T CARE	DON'T CARE	CONFIGURATION REGISTER OF DEVICE #2	DON'T CARE	DON'T CARE	CONFIGURATION REGISTER OF DEVICE #1

Figure 13b. Configuration Registers

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

1ST BYTE SHIFTED IN	2ND BYTE SHIFTED IN	3RD BYTE		4TH BYTE		5TH BYTE		6TH BYTE		7TH BYTE		8TH BYTE		. . .	12TH BYTE		13TH BYTE		14TH (LAST) BYTE	
DON'T CARE (OPTIONAL, SEE NOTE.)	DON'T CARE (OPTIONAL, SEE NOTE.)	h BITS AND DIMMER BIT	BANK 5 NIBBLE	BANK 4 NIBBLE	BANK 3 NIBBLE	BANK 2 NIBBLE	BANK 1 NIBBLE	h BITS AND DIMMER BIT	BANK 5 NIBBLE	BANK 4 NIBBLE	BANK 3 NIBBLE	BANK 2 NIBBLE	BANK 1 NIBBLE	. . .	h BITS AND DIMMER BIT	BANK 5 NIBBLE	BANK 4 NIBBLE	BANK 3 NIBBLE	BANK 2 NIBBLE	BANK 1 NIBBLE
		DISPLAY REGISTER OF DEVICE #4						DISPLAY REGISTER OF DEVICE #3						. . .	DISPLAY REGISTER OF DEVICE #1					

Figure 13c. Display Registers

NOTE: When the "don't care" bytes are included, $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active-low during the entire 12-byte configuration transfer or 14-byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either a 12- or 14-byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the two "don't care" bytes can be eliminated as follows: (1) take $\overline{\text{ENABLE}}$ active low, (2) transfer 6 bytes, (3) pulse $\overline{\text{ENABLE}}$ inactive high, see $t_{w(H)}$ spec, (4) transfer last 6 bytes, and (5) take $\overline{\text{ENABLE}}$ inactive high.

Figure 13. Bit Stream Formats for Four Devices Cascaded

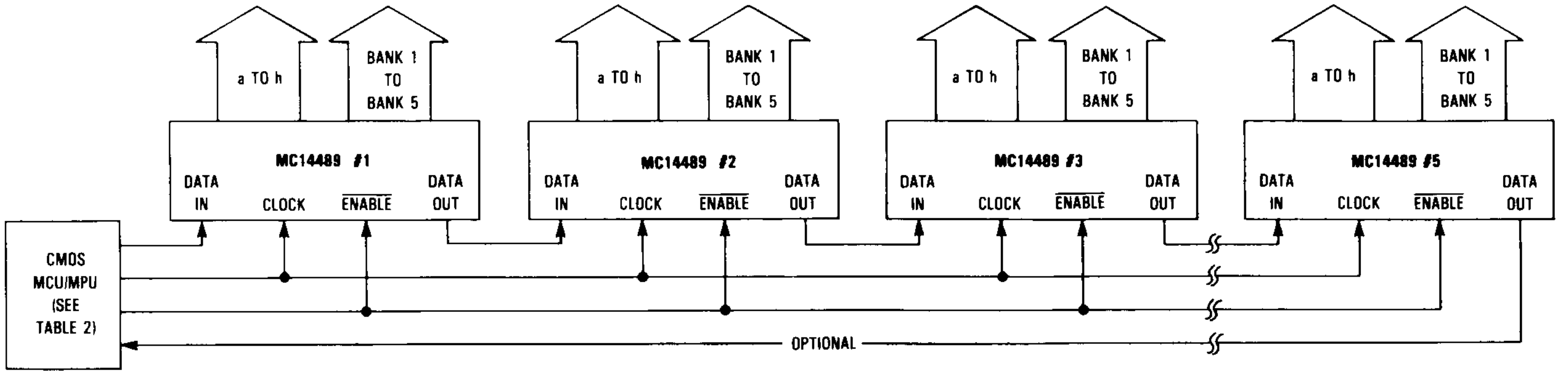


Figure 14a. Cascading Five Devices

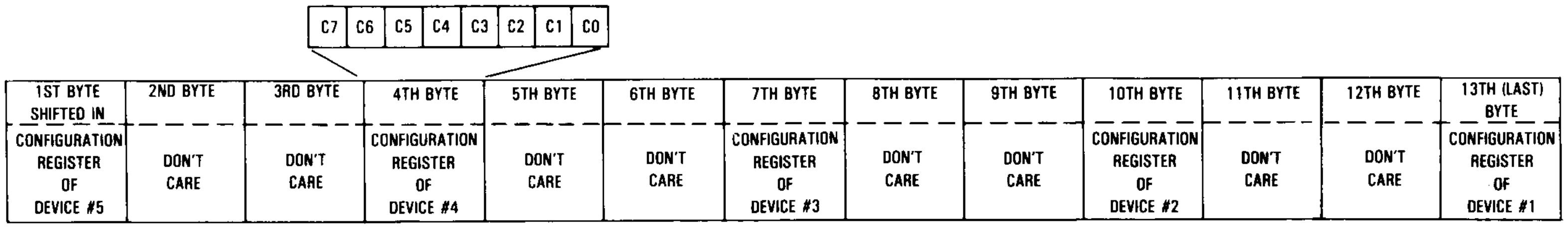


Figure 14b. Configuration Registers

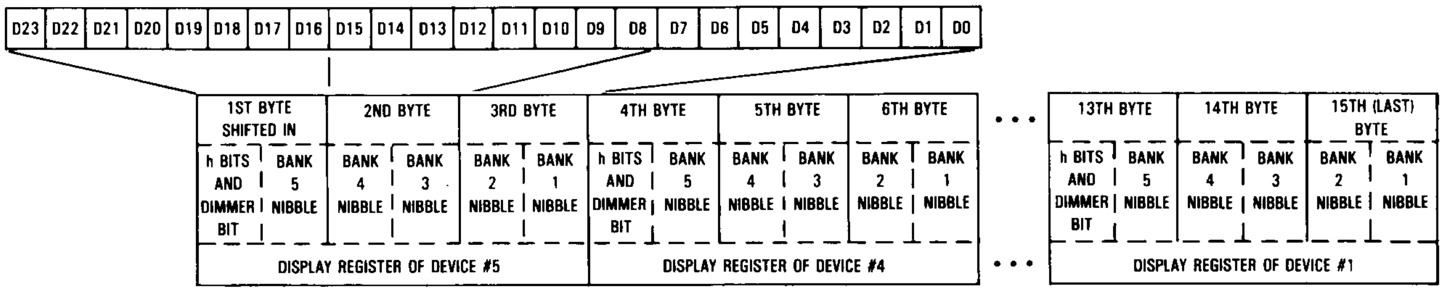
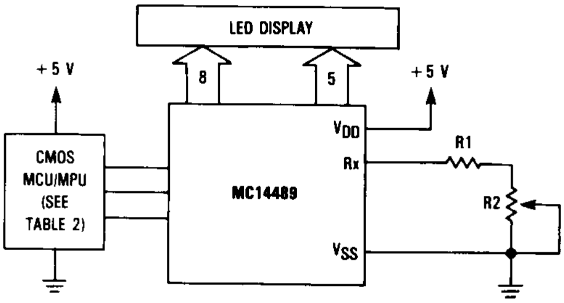


Figure 14c. Display Registers

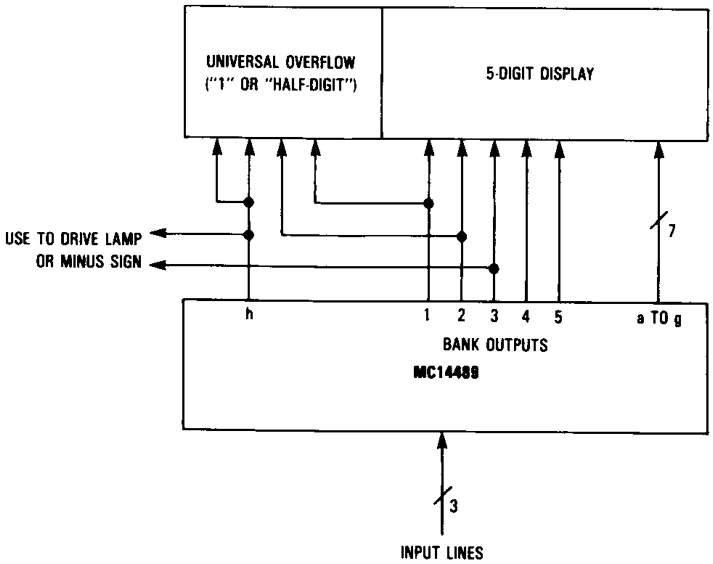
NOTE: ENABLE (which initially must be inactive high) is kept active-low during the entire 13-byte configuration transfer or 15-byte display transfer. When ENABLE is brought back high, either a 13- or 15-byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

Figure 14. Bit Stream Formats for Five Devices Cascaded



NOTES: R1 limits the maximum current to avoid damaging the display and/or the MC14489 due to overheating. See the Thermal Considerations section. An 1/8 watt resistor may be used for R1. R2 is a 1 kΩ or 5 kΩ potentiometer (≥ 1/8 watt).

Figure 15. Common-Cathode LED Display with Dial-Adjusted Brightness



NOTE: A Universal Overflow pins out all anodes and cathodes.

Figure 16. Driving 5 1/2 Digits

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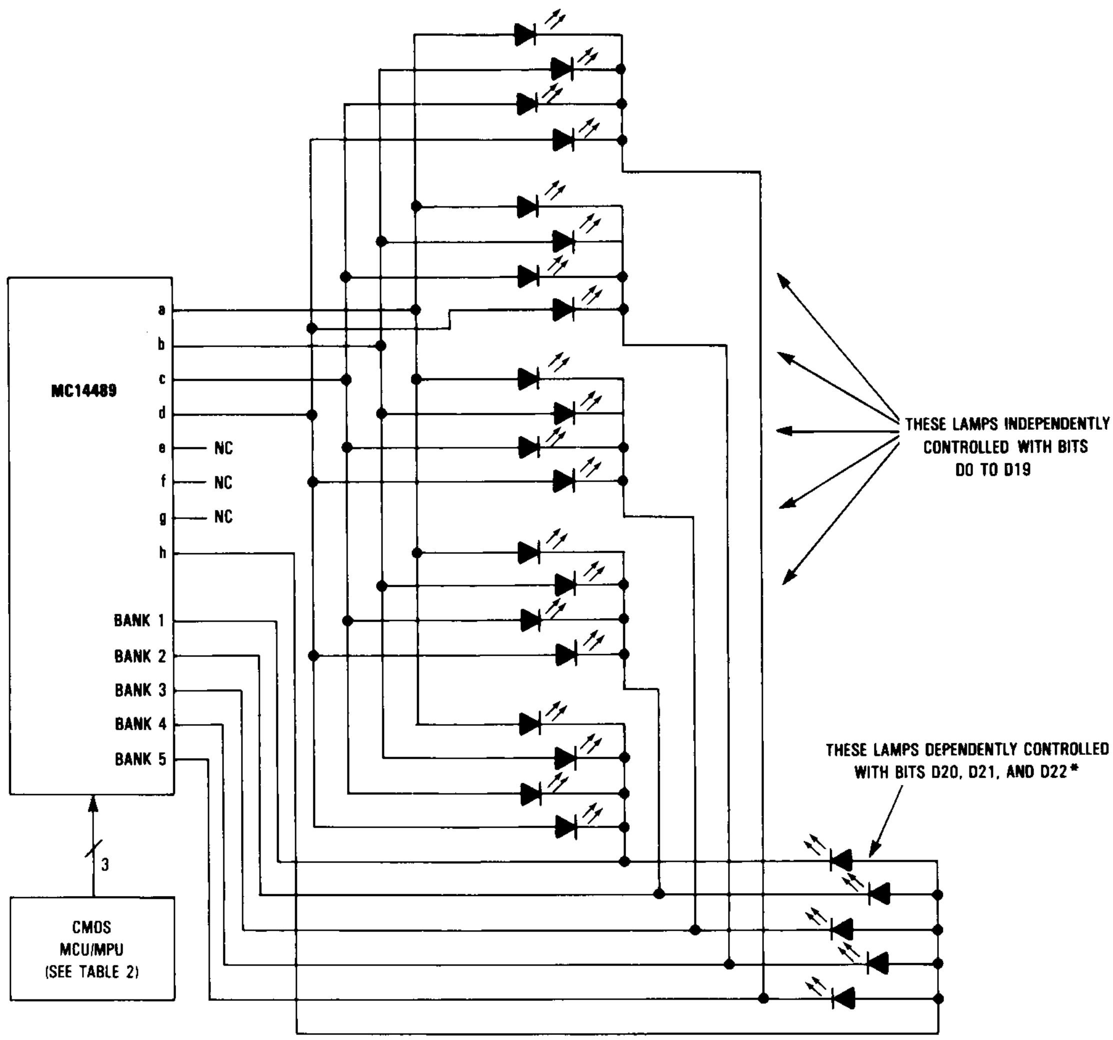


*If required, this group of lamps can be independently controlled. To accomplish independent control, only connect lamps to BANK 1 and BANK 2 for output h (2 lamps). Then, use bits D20, D21, and D22 for control of these 2 lamps.

Figure 17. 25 Lamp Application

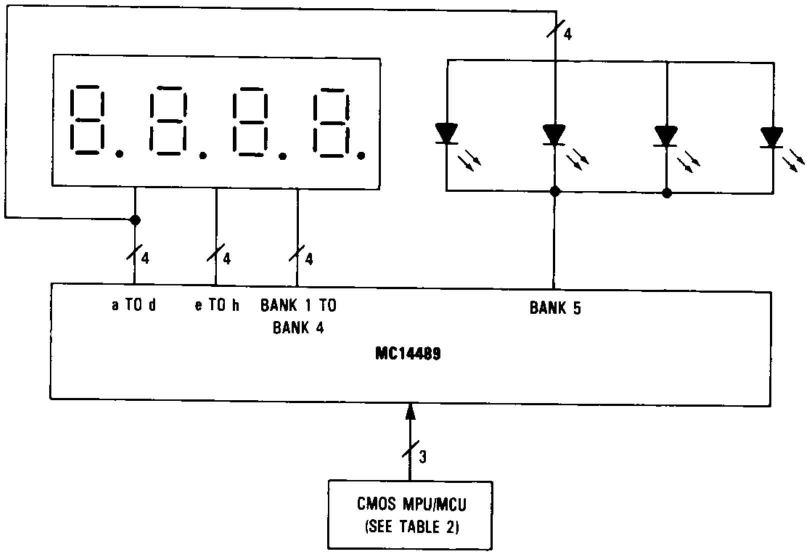


Figure 18. 4-Digit Display Plus Decimals with Four Annunciators or 4 1/2-Digit Display Plus Sign

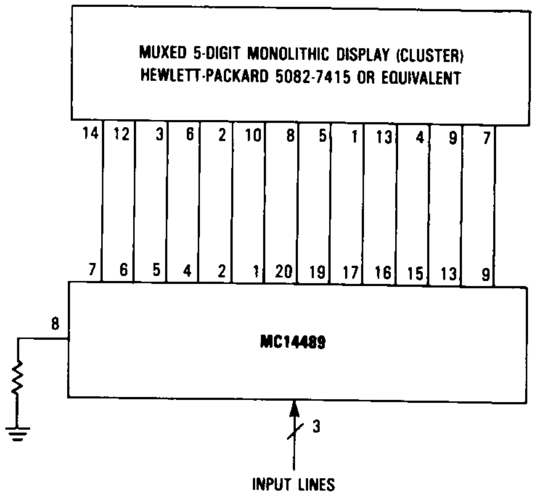


Figure 19. Compact Display System with Three Components

THERMAL CONSIDERATIONS

The MC14489 is designed to operate with a *chip-junction* temperature (T_J) ranging from -40 to 130°C, as indicated in the electrical characteristics tables. The *ambient* operating temperature range (T_A) is dependent on $R_{\theta JA}$, the internal chip current, how many anode drivers are used, the number of bank drivers used, the drive current, and how the package is cooled. The maximum ratings table gives the thermal resistance, junction-to-ambient, of the MC14489 mounted on a pc board using natural convection to be 90°C per watt for the plastic DIP. The SOG thermal resistance is 100°C per watt.

The following general equation (1) is used to determine the power dissipated by the MC14489.

$$P_T = P_D + P_I \qquad (1)$$

where

P_T = Total power dissipation of the MC14489
P_D = Power dissipated in the driver circuitry (mW)
P_I = Power dissipated by the internal chip circuitry (mW)

The equations for the two terms of the general equation are:

$$P_D = (i_{OH})(N)(V_{DD} - V_{LED})(B/5) \qquad (2)$$

$$P_I = (1.5\ \text{mA})(V_{DD}) + I_{Rx}(V_{DD} - I_{Rx}R_x) \qquad (3)$$

where

i_{OH} = Peak anode driver current (mA)
$I_{Rx} \approx i_{OH}/10$, with i_{OH} = the peak anode driver current (mA) when the dimmer bit is high
N = Number of anode drivers used
B = Number of bank drivers used
R_x = External resistor value (kΩ)
V_{DD} = Maximum supply voltage, referenced to V_{SS} (volts)
V_{LED} = Minimum anticipated voltage drop across the LED
1.5 mA = Operating supply current of the MC14489

The following two examples show how to calculate the maximum allowable ambient temperature.

Worst-Case Analysis Example 1:

5-digit display with decimals (5 banks and 8 anode drivers)
DIP without heat sink on PC board
i_{OH} = 20 mA max
V_{LED} = 1.8 V min
V_{DD} = 5.25 V max

$P_D = (20)(8)(5.25 - 1.8)(5/5) = 552$ mW — Ref. (2)

$P_I = (1.5)(5.25) + 2[5.25 - 2(2)] = 10$ mW — Ref. (3)

Therefore, $P_T = 552 + 10 = 562$ mW — Ref. (1)

and $\Delta T_{chip} = R_{\theta JA} P_T = (90°C/W)(0.562) = 51°C$

Finally, the maximum allowable $T_A = T_J max - \Delta T_{chip} = 130 - 51 = 79°C$

That is, if $T_A = 79°C$, the maximum junction temperature is 130°C. The chip's average temperature for this example is lower than 130°C because all segments are usually not illuminated simultaneously for an indefinite period.

Worst-Case Analysis Example 2:

16 lamps (4 banks and 4 anode drivers)
SOG without heat sink on PC board
i_{OH} = 30 mA max
V_{LED} = 1.8 V min
V_{DD} = 5.5 V max

$P_D = (30)(4)(5.5 - 1.8)(4/5) = 355$ mW — Ref. (2)

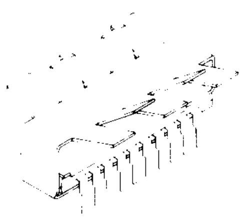
$P_I = (1.5)(5.5) + 3[5.5 - 3(1.0)] = 16$ mW — Ref. (3)

Therefore, $P_T = 355 + 16 = 371$ mW — Ref. (1)

and $\Delta T_{chip} = R_{\theta JA} P_T = (100°C/W)(0.371) = 37°C$

Finally, the maximum allowable $T_A = T_J max - \Delta T_{chip} = 130 - 37 = 93°C$

To extend the allowable ambient temperature range or to reduce T_J, which extends chip life, a heat sink such as shown in Figure 20 can be used in high-current applications. Alternatively, heat-spreader techniques can be used on the PC board, such as running a wide trace under the MC14489 and using thermal paste. Wide, radial traces from the MC14489 leads also act as heat spreaders.



AAVID #5804 or equivalent
(Tel. 603/524-4443, TWX 510/298-1127)
Motorola cannot recommend one supplier over another and in no way suggests that this is the only heat sink supplier.

Figure 20. Heat Sink

Table 2. Compatible Motorola MCUs/MPUs
This is not a complete listing of Motorola's MCUs/MPUs. Contact your Motorola representative if you need additional information.

Instruction Set	Memory (Bytes) ROM	Memory (Bytes) EEPROM	SPI ① SCI ②	A/D ③	Device Number
M68HC11	–	–	Yes	Yes	MC68HC11A0
	–	512	Yes	Yes	MC68HC11A1
	–	2048	Yes	Yes	MC68HC811A2
	8192	512	Yes	Yes	MC68HC11A8
	12 K	512	Yes	Yes	MC68HC11E9
M6805	2096	–	–	–	MC68HC05C2
	2096	–	Yes	–	MC68HC05C3
	4160	–	Yes	–	MC68HC05C4
	4160④	–	Yes	–	MC68HSC05C4
	8K④	–	Yes	–	MC68HSC05C8
	4160⑤	–	Yes	–	MC68HCL05C4
	8K⑤	–	Yes	–	MC68HCL05C8
	7700	–	Yes	–	MC68HC05C8
	–	4160	–	–	MC68HC805C4
M68000	–	–	–	–	MC68HC000

① SPI = Serial Peripheral Interface.

② SCI = Serial Communications Interface.

③ A/D = Analog-to-Digital Converter.

④ High speed.

⑤ Low power.

Table 3. LED Lamp and Common-Cathode Display Manufacturers

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of LED suppliers.

Supplier	Contact Information
General Instruments (GI), Optoelectronics Division	Phone: (415) 493-0400 TWX/TLX: 470208 FAX: (415) 493-7055
Hewlett-Packard (HP), Components Group	Contact your local H-P Components Sales Office
Industrial Electronic Engineers (IEE), Component Products Div.	Phone: (818) 787-0311 TLX: 4720556 FAX: (818) 902-3723
William J. Purdy Co., AND Division	Phone: (415) 347-9916 MCI/TLX: 677-1439 FAX: (415) 340-1670

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