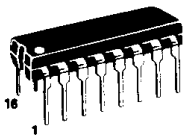
MC145170

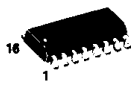
Product Preview

PLL Frequency Synthesizer with Serial Interface

CMOS



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOG
CASE 751B

ORDERING INFORMATION

MC145170P	Plastic DIP
MC145170D	SOG Package

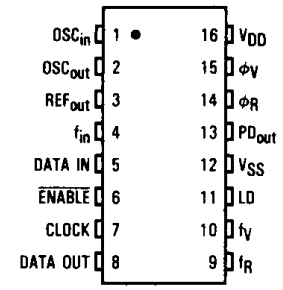
The MC145170 is a single-chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL the easiest to program in the industry. Either a bit- or byte-oriented format may be used. Due to the BitGrabber registers,* no address/steering bits are required for random access of the three registers. Thus, tuning can be accomplished via a 2-byte serial transfer to the 16-bit N register.

The device features fully-programmable R and N counters, an amplifier at the f_{in} pin, on-chip support of an external crystal, a programmable reference output, and both single- and double-ended phase detectors with linear transfer functions. A new feature on the MC145170 is the C register (configuration register). The C register allows the part to be configured to meet various applications. Also, the C register allows unused outputs to be shut off,* thereby minimizing system noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam-load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.5 to 6 V
- Maximum f_{in} Operating Frequency: 160 MHz @ $V_{in} = 500\ mV_{p-p}$, 4.5 to 6 V Supply
- Operating Temperature Range: −40° to 85°C
- R Counter Division Range: 5 to 32,767 Plus Direct Access to Phase Detector Input
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola/RCA SPI and National MICROWIRE Serial Data Ports
- 180 MHz Version Available (Part Number SC370566), Consult Factory
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates

PIN ASSIGNMENT



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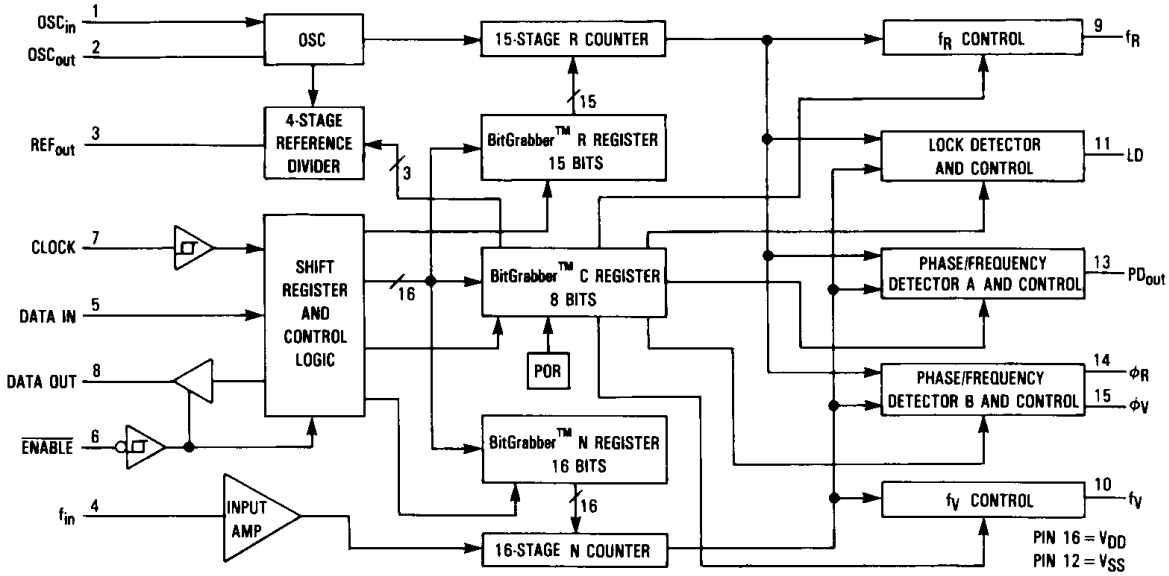

*Patent pending.

BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

MAXIMUM RATINGS* (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, $T_A = -40°$ to 85°C unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		–	2.5 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage (Data In, Clock, $\overline{Enable}$)		2.5 4.5 6.0	0.5 1.35 1.8	V
V_{IH}	Minimum High-Level Input Voltage (Data In, Clock, $\overline{Enable}$)		2.5 4.5 6.0	2.0 3.15 4.2	V
V_{Hys}	Minimum Hysteresis Voltage (Clock, $\overline{Enable}$)		2.5 6.0	0.15 0.2	V
V_{OL}	Maximum Low-Level Output Voltage (Any Output)	$I_{out} = 20\ \mu A$	2.5 6.0	0.1 0.1	V
V_{OH}	Minimum High-Level Output Voltage (Any Output)	$I_{out} = -20\ \mu A$	2.5 6.0	2.4 5.9	V
I_{OL}	Minimum Low-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	2.5 4.5 6.0	0.12 0.36 0.5	mA
I_{OH}	Minimum High-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	$V_{out} = 2.2$ V $V_{out} = 4.1$ V $V_{out} = 5.5$ V	2.5 4.5 6.0	−0.12 −0.36 −0.5	mA
I_{OL}	Minimum Low-Level Output Current (Data Out)	$V_{out} = 0.4$ V	4.5	1.6	mA
I_{OH}	Minimum High-Level Output Current (Data Out)	$V_{out} = 4.1$ V	4.5	−1.6	mA
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{Enable}$, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	6.0	±1.0	μA
		$V_{in} = V_{DD}$ or V_{SS}, $T_A = 25°C$ only	6.0	±0.1	
I_{in}	Maximum Input Current (f_{in})	$V_{in} = V_{DD}$ or V_{SS}	6.0	±120	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	$V_{in} = V_{DD}$ or V_{SS}, Output in High-Impedance State	6.0	±100	nA
	(Data Out)		6.0	±5	μA
I_{DD}	Maximum Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS}, Outputs Open, Excluding f_{in} Amp Input Current Component	6.0	100	μA
		Same as Above, $T_A = 25°C$ only	6.0	TBD	
I_{dd}	Maximum Operating Supply Current	f_{in} = 160 MHz @ 500 mV_{p-p}; OSC_{in} = 10 MHz @ 1 V_{p-p}; f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; Data In, $\overline{Enable}$, Clock = V_{DD} or V_{SS}	4.5 6.0	TBD TBD	mA

AC INTERFACE CHARACTERISTICS ($T_A = -40°$ to 85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency NOTE: Refer to Clock t_w below (Figure 1)	2.5 4.5 6.0	dc to TBD dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Data Out (Figures 1 and 5)	2.5 4.5 6.0	TBD 85 85	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, Data Out Active to High Impedance (Figures 2 and 6)	2.5 4.5 6.0	TBD 200 200	ns
t_{PZL}, t_{PZH}	Access Time, Data Out High Impedance to Active (Figures 2 and 6)	2.5 4.5 6.0	TBD 0 to 100 0 to 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Data Out (Figures 1 and 5), $C_L = 50$ pF	2.5 4.5 6.0	TBD 50 50	ns
	$C_L = 200$ pF	2.5 4.5 6.0	TBD 150 150	
C_{in}	Maximum Input Capacitance—Data In, Clock, $\overline{\text{Enable}}$	—	10	pF
C_{out}	Maximum Output Capacitance—Data Out	—	15	pF

TIMING REQUIREMENTS ($T_A = -40°$ to 85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	2.5 4.5 6.0	TBD 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	2.5 4.5 6.0	TBD 100 100	ns
$t_{w(H)}$	Minimum Inactive-High Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	2.5 4.5 6.0	TBD 300 300	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.5 4.5 6.0	TBD 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times—Clock, $\overline{\text{Enable}}$ (Figure 1)	2.5 4.5 6.0	100 100 100	μs

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SWITCHING WAVEFORMS

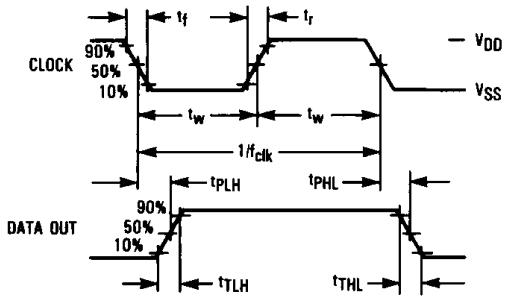


Figure 1

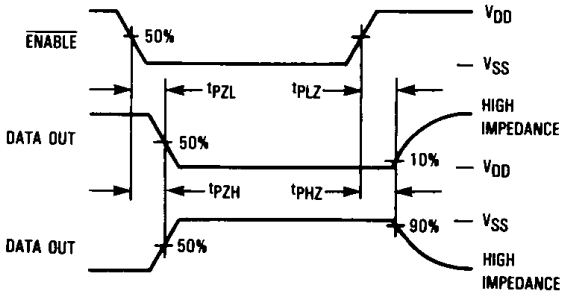


Figure 2

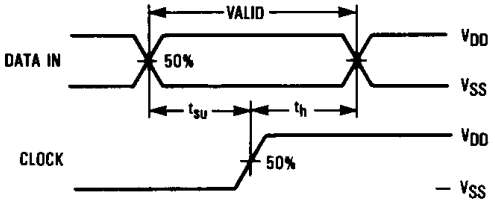


Figure 3

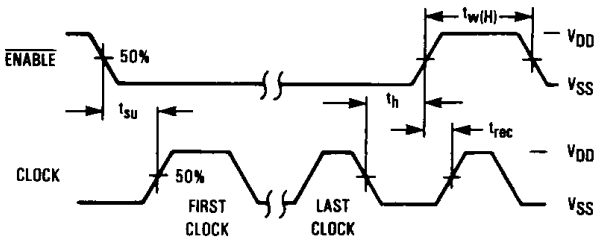
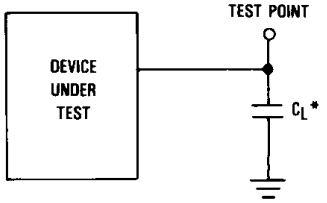
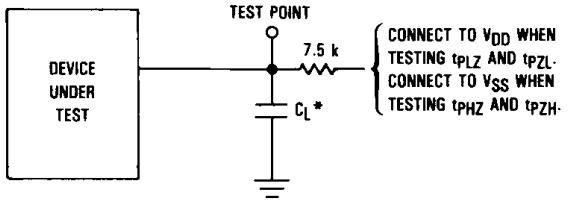


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (T_A = −40° to 85°C)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit		Unit
				Min	Max	
f_{in}	Input Frequency, f_{in} (Figure 7)	V_{in} = 500 mV_{p-p} Sine Wave, N Counter set to divide ratio such that $f_V \leq 2$ MHz	2.5 3.0 4.5 6.0	TBD TBD TBD TBD	TBD 100 160 160	MHz
f_{in}	Input Frequency, OSC_{in} Externally Driven (Figure 8)	V_{in} = 1 V_{p-p}, OSC_{out} = No Connect, R Counter set to divide ratio such that $f_R \leq 2$ MHz	2.5 3.0 4.5 6.0	1 1 1 1	12 14 20 20	MHz
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out} (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	2.5 3.0 4.5 6.0	2 2 2 2	12 12 15 15	MHz
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 30 pF	2.5 3.0 4.5 6.0	dc dc dc dc	TBD TBD 10 10	MHz
f	Operating Frequency of the Phase Detectors		2.5 3.0 4.5 6.0	dc dc dc dc	TBD TBD 2 2	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD (Figures 11 and 12)	f_R in Phase with f_V, C_L = 50 pF	2.5 3.0 4.5 6.0	TBD TBD 20 16	TBD TBD 100 90	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, f_V, f_R, ϕ_V, and ϕ_R (Figures 11 and 12)	C_L = 50 pF	2.5 3.0 4.5 6.0	– – – –	TBD TBD 65 60	ns
C_{in}	Input Capacitance, f_{in} OSC_{in}		– –	– –	5 5	pF

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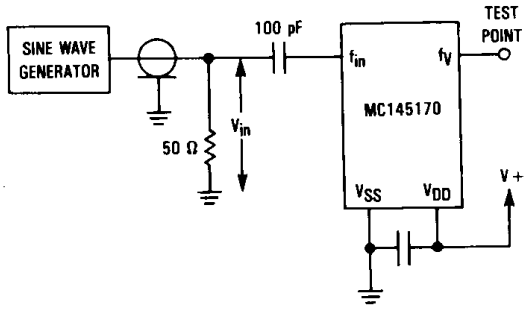

Figure 7. Test Circuit

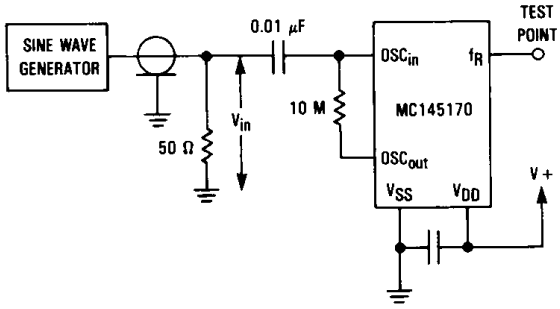

Figure 8. Test Circuit

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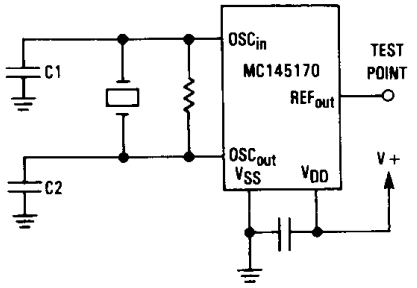


Figure 9. Test Circuit

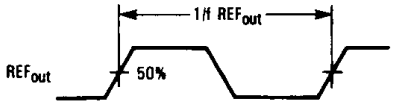


Figure 10. Switching Waveform

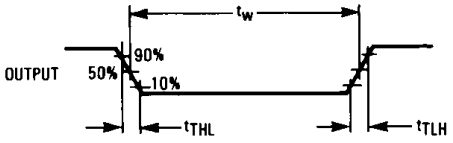
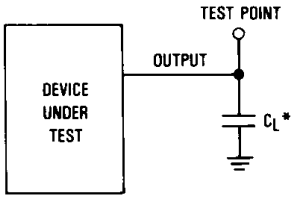


Figure 11. Switching Waveform



*Includes all probe and jig capacitance.

Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE

Data In (Pin 5)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low-to-high transition of Clock. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R or reference register. Optionally, the R register can be accessed with a 15-bit transfer. See Table 1. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{\text{Enable}}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 2.5 to 6 V. The formats are shown in Figures 13, 14, and 15.

Data In typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pullup resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first. C0, N0, and R0 are the LSBs)

No. of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤32	None	
Values >32	Not Allowed	

Clock (Pin 7)

Serial Data Clock Input. Low-to-high transitions on Clock shift bits available at Data In, while high-to-low transitions shift bits from Data Out. The chip's 16-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 can be used to access the R register. See Table 1 and Figures 13, 14, and 15.

Clock typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow Clock rise and fall times are allowed. See the last paragraph of **Data In** for more information.

$\overline{\text{Enable}}$ (Pin 6)

Active-Low Enable Input. This pin is used to activate the serial interface to allow the transfer of data to/from the MC145170. When $\overline{\text{Enable}}$ is in an inactive high state, Data Out is forced to the high-impedance state, shifting is inhibited, and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which must start inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken back high. The low-to-high transition on $\overline{\text{Enable}}$ transfers data to the C, N, or R register, depending on the data stream length per Table 1.

CAUTION

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **Data In** for more information.

Data Out (Pin 8)

Three-State Serial Data Output. Data is transferred out of the 16-1/2-stage shift register through Data Out on the high-to-low transition of Clock. This output is a no connect, unless used in one of the manners discussed below.

Data Out could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in-line QA test during board manufacturing.

Finally, Data Out facilitates troubleshooting a system.

REFERENCE PINS

OSC_{in} and OSC_{out} (Pins 1 and 2)

Oscillator Input and Output. These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The MC145170 is designed to operate with crystals up to 15 MHz with a 4.5 to 6 V supply. With supplies less than 4.5 V, up to 12 MHz crystals may be used. See Figure 9.

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 μF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 10 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac-coupled case. (See Figure 8.) *OSC_{out} is an internal node on the device and should not be used to drive any loads.* That is, OSC_{out} is unbuffered. However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V_{p-p}; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, then dc coupling can be used. In the dc-coupled case, no external feedback resistor is needed. OSC_{out} must be a no connect to avoid loading an internal node on the MC145170, as above.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

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REF_{out} (Pin 3)

Reference Frequency Output. This output is the buffered output of the crystal-generated reference frequency or externally-provided reference source. This output may be enabled, disabled, or scaled via bits in the C register. See Figure 13.

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces REF_{out} to the OSC_{in} divided-by-8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUTS

f_R (Pin 9)

Reference Counter Output. This signal is the buffered output of the 15-stage R counter. f_R can be enabled or disabled via the C register. (Patent pending.) The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of one. See Figure 14. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the f_R signal appears as normally low. f_R pulses high whenever the R counter is loading the value from the R register.

f_V (Pin 10)

N Counter Output. This signal is the buffered output of the 16-stage N counter. f_V can be enabled or disabled via the C register. (Patent pending.) The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the f_V signal appears as normally low. f_V pulses high whenever the N counter is loading the value from the N register.

LOOP PINS

f_{in} (Pin 4)

Frequency Input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac-coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. (See Figure 7.) The frequency capability of this input is dependent on the input signal level for the divide ratios listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used.

Each rising edge on the f_{in} pin causes the N counter to decrement by one.

PD_{out} (Pin 13)

Single-Ended Phase/Frequency Detector Output. This is a 3-state output for use as a loop error signal when combined with an external low-pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register. (Patent pending.)

ϕ_R and ϕ_V (Pins 14 and 15)

Doubled-Ended Phase/Frequency Detector Outputs. These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register. (Patent pending.)

LD (Pin 11)

Lock Detector Output. This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. See Figure 16.

This output can be enabled and disabled via the C register. (Patent pending.) Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

V_{DD} (Pin 16)

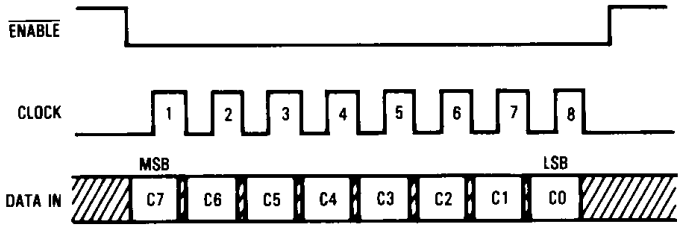
Most-Positive Supply Potential. This pin may range from +2.5 to +6 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using (a) low-inductance capacitor(s) mounted very close to the MC145170. Lead lengths on the capacitor(s) should be minimized. (The very-fast switching speed of the device causes current spikes on the power leads.)

V_{SS} (Pin 12)

Most-Negative Supply Potential. This pin is usually ground.

For measurement purposes, the V_{SS} pin is tied to a ground plane.



NOTE:

C7-POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges ϕ_R function with ϕ_V as depicted in Figure 16. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6-PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5-LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4, C3, C2-OSC2, OSC1, OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1-f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

C0-f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 13. C Register Access and Format (8 Clock Cycles Are Used)

5

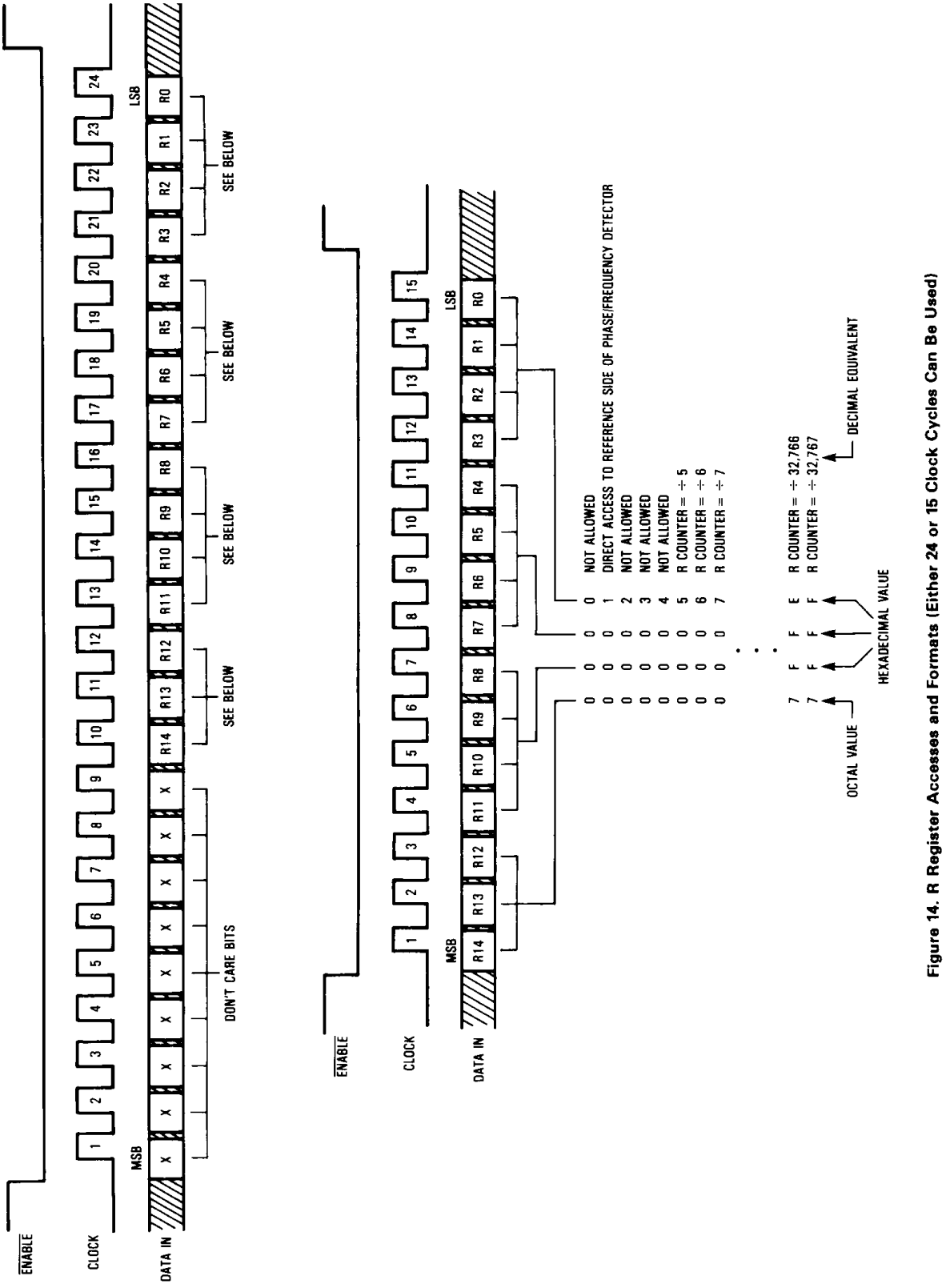


Figure 14. R Register Accesses and Formats (Either 24 or 15 Clock Cycles Can Be Used)

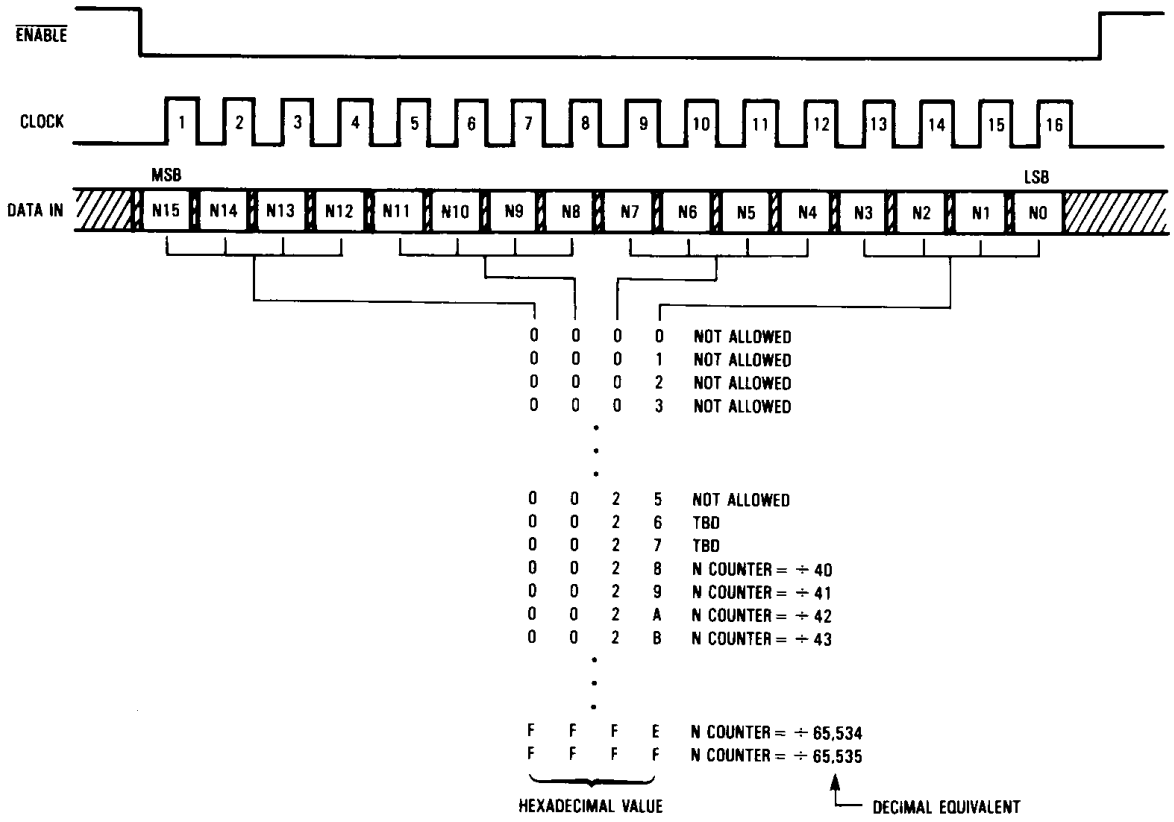
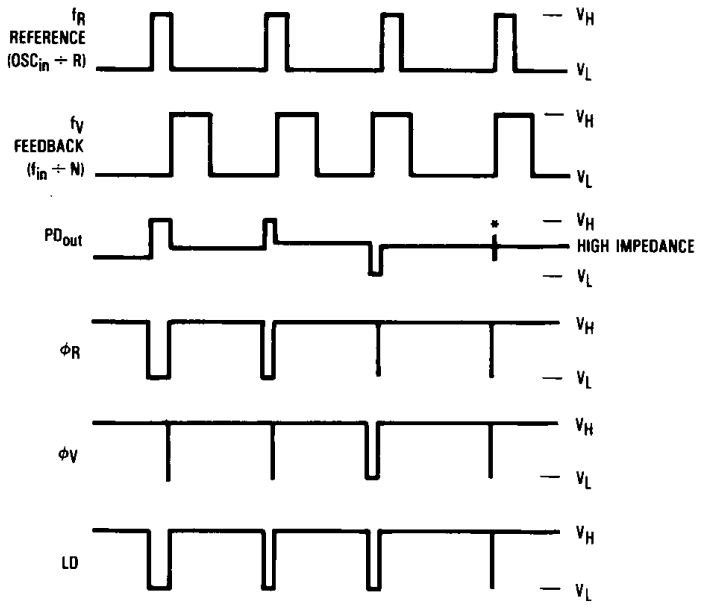


Figure 15. N Register Access and Format (16 Clock Cycles Are Used)

5



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
NOTE: The PD_{out} output generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 13 for POL.

Figure 16. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. See Figure 8.

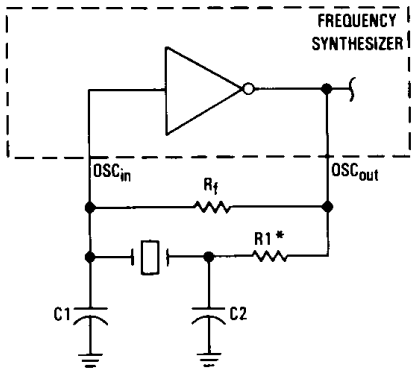
For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling is used.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 17.



*May be needed in certain cases. See text.

Figure 17. Pierce Crystal Oscillator Circuit

For $V_{DD} = 5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 12 pF when used at the highest operating frequency of 15 MHz. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

$C_{in} = 5$ pF (see Figure 18)
$C_{out} = 6$ pF (see Figure 18)
$C_a = 1$ pF (see Figure 18)
C1 and C2 = external capacitors (see Figure 17)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

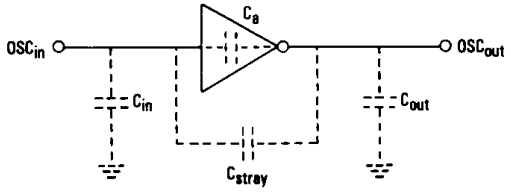
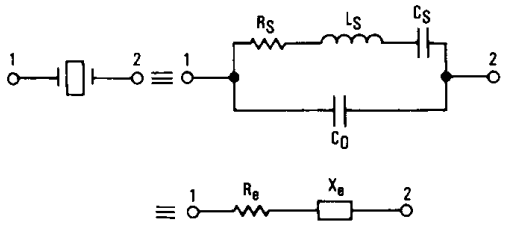


Figure 18. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 19. Equivalent Crystal Networks

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

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Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 19. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 17 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of supply voltage at REF_{out}. (OSC_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 2.

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit—Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, February 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

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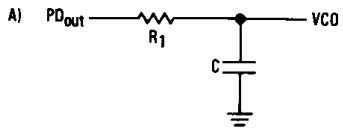
Table 2. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

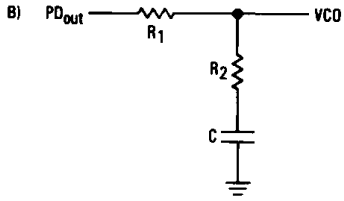
PHASE-LOCKED LOOP—LOW PASS FILTER DESIGN

A) 

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

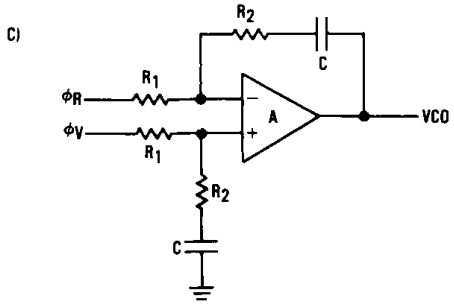
$$F(s) = \frac{1}{R_1sC + 1}$$

B) 

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\ \omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

C) 

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE:

For C), R_1 is frequently split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly effect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ volts/radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ volts/radian for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\dfrac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R-related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*, New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538-586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator" *EDN*. March 5, 1980.
AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.
BR504/D, Electronic Tuning Address Systems, Motorola Semiconductor Products, Inc., 1986.

PLL Frequency Synthesizers (PLL FS)

5

SELECTOR GUIDE

Divider Programming Format	External Prescaler Modulus	Single-Ended 3-State Phase Detector Output	Double-Ended Phase Detector Output	Number of Divider Stages +R	+A	+N	f_{max} MHz	Device Number
Serial	Single	√	√	14*	—	14	20	**MC145155-2**
		√	√	14	—	14	20	**MC145157-2**
	Dual	√√♦	—	14	7	10	15	**MC145149**
		√	√	12*	7	10	20	**MC145156-2**
		√	√	14	7	10	20	**MC145158-2**
	Dual	Frequency Detector	Analog Detector	14	7	10	15	**MC145159-1**
	None	√√♦	—	11*	—	14	60	**MC145167**
		√√♦	—	11*	—	14	60	**MC145169**
		√	√	15	—	16	160#	**MC145170**
Parallel	Single	√	—	11*	—	9	4	**MC145106**
		√	√	14*	—	14	20	**MC145151-2**
	Dual	—	√	12*	6	10	20	**MC145152-2**
	None	√√♦	—	12*	—	14	60	**MC145160**
		√√♦	—	11*	—	14	60	**MC145166**
		√√♦	—	11*	—	14	60	**MC145168**
4-Bit Bus	Single	√	√	12	—	14	20	**MC145145-2**
	Dual	√	√	12	7	10	20	**MC145146-2**

*Limited number of selectable values.

♦Accommodates two loops per package.

#180 MHz version available. See data sheet.