MC145155-2

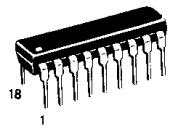
Serial-Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers

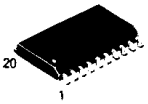
The MC145155-2 is programmed by a clocked, serial input, 16-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 14-bit programmable divide-by-N counter, and the necessary shift register and latch circuitry for accepting serial input data.

The MC145155-2 is an improved-performance drop-in replacement for the MC145155-1. Power consumption has decreased and ESD and latch-up performance have improved.

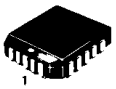
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- 8 User-Selectable ÷ R Values: 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Single Modulus/Serial Programming
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State) or Double Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 707



DW SUFFIX
SOG
CASE 751D



FN SUFFIX
PLCC
CASE 775

ORDERING INFORMATION

MC145155P2	Plastic DIP
MC145155DW2	SOG Package
MC145155FN2	PLCC Package

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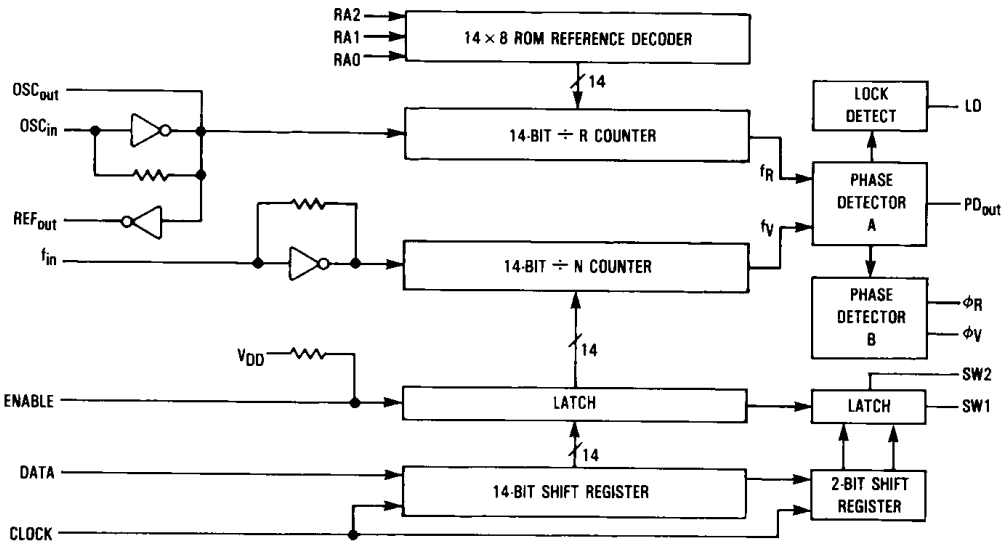
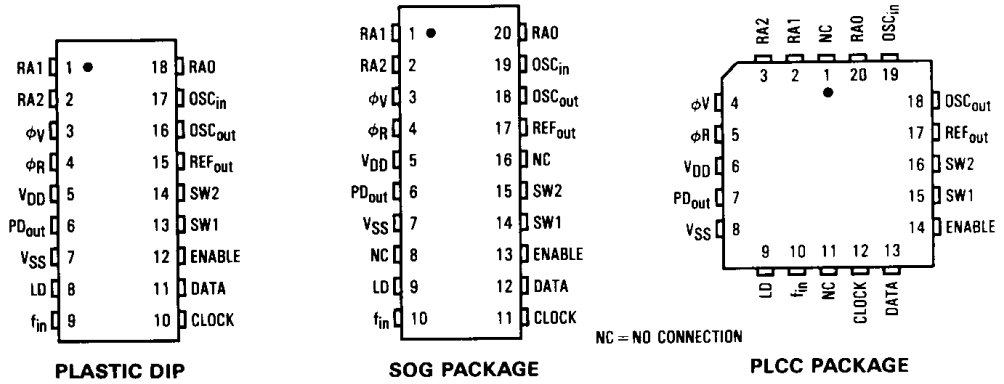
BLOCK DIAGRAM



PIN ASSIGNMENTS



PLASTIC DIP | SOG PACKAGE | PLCC PACKAGE

PIN DESCRIPTIONS

INPUTS

f_{in}—Frequency Input

Input to the ÷ N portion of synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

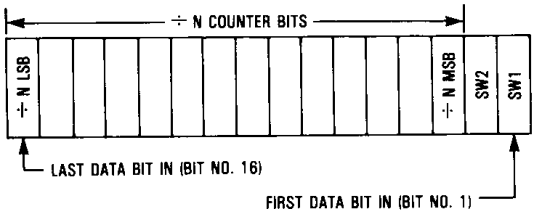
RA0, RA1, RA2—Reference Address Inputs

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	16
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	3668
1	0	1	4096
1	1	0	6144
1	1	1	8192

CLOCK, DATA—Shift Clock, Serial Data Inputs

Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 16-bit shift register. The Data input provides programming information for the 14-bit ÷ N counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE—Latch Enable Input

When high ("1") transfers contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low ("0") inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip pullup establishes a continuously high level for Enable when no external signal is applied. Enable is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUTS

PD_{out}—Phase Detector A Output

Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses.
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses.
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State.

ϕV, ϕR—Phase Detector B Outputs

These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

LD—Lock Detector Output

Lock detector signal. Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

SW1, SW2—Band Switch Outputs

SW1 and SW2 provide latched open-drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V dc, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic one causes the output to assume a high-impendance state, while a logic zero causes the output to be low.

REF_{out}—Buffered Oscillator Output

Buffered output of on-chip reference oscillator or externally provided reference-input signal.

POWER SUPPLY

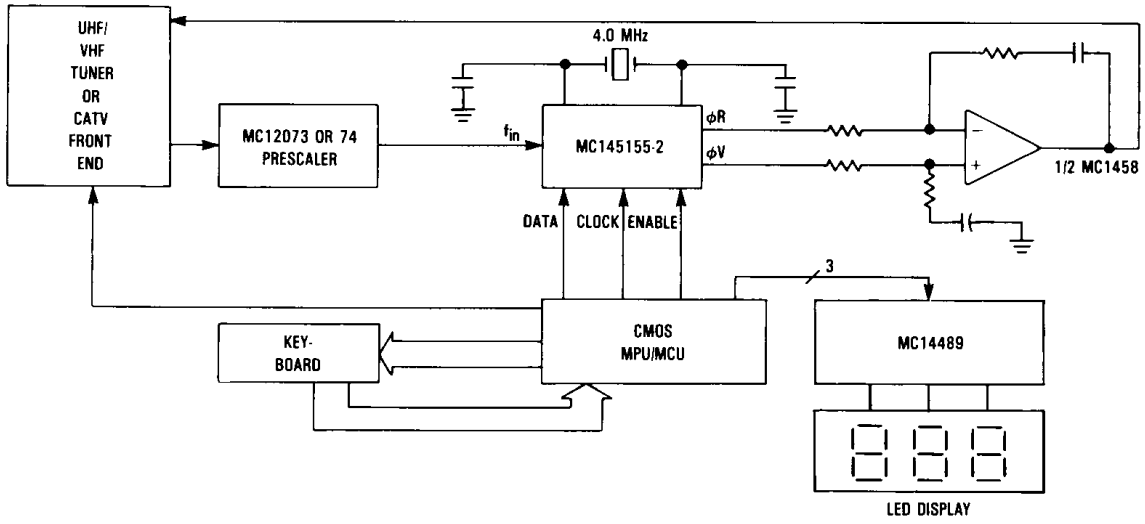
V_{DD}

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

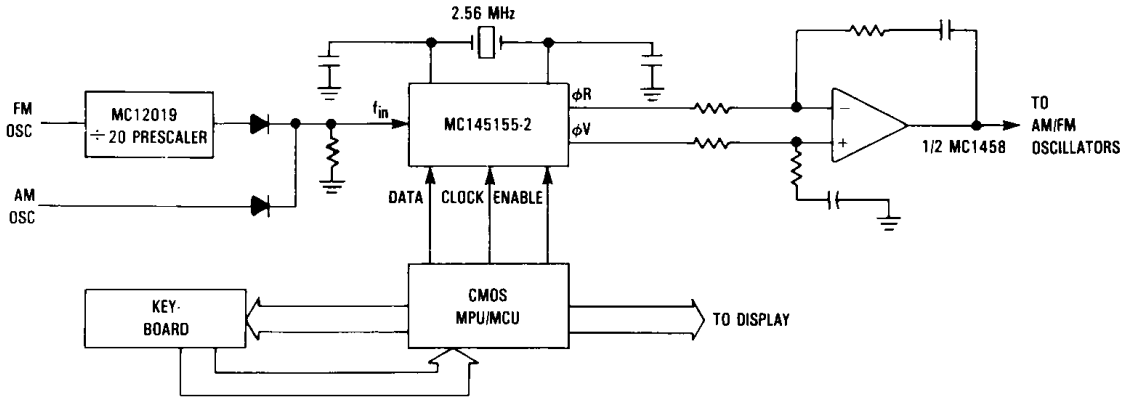
V_{SS}

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



Microprocessor-Controlled TV/CATV Tuning System with Serial Interface



AM/FM Radio Synthesizer