**MC145157-2**

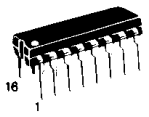
# Serial-Input PLL Frequency Synthesizer

## Interfaces with Single-Modulus Prescalers

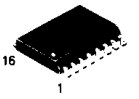
The MC145157-2 has a fully programmable 14-bit reference counter, as well as a fully programmable ÷ N counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145157-2 is an improved-performance drop-in replacement for the MC145157-1. Power consumption has decreased and ESD and latch-up performance have improved.

- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383
- $f_V$ and $f_R$ Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOG
CASE 751G

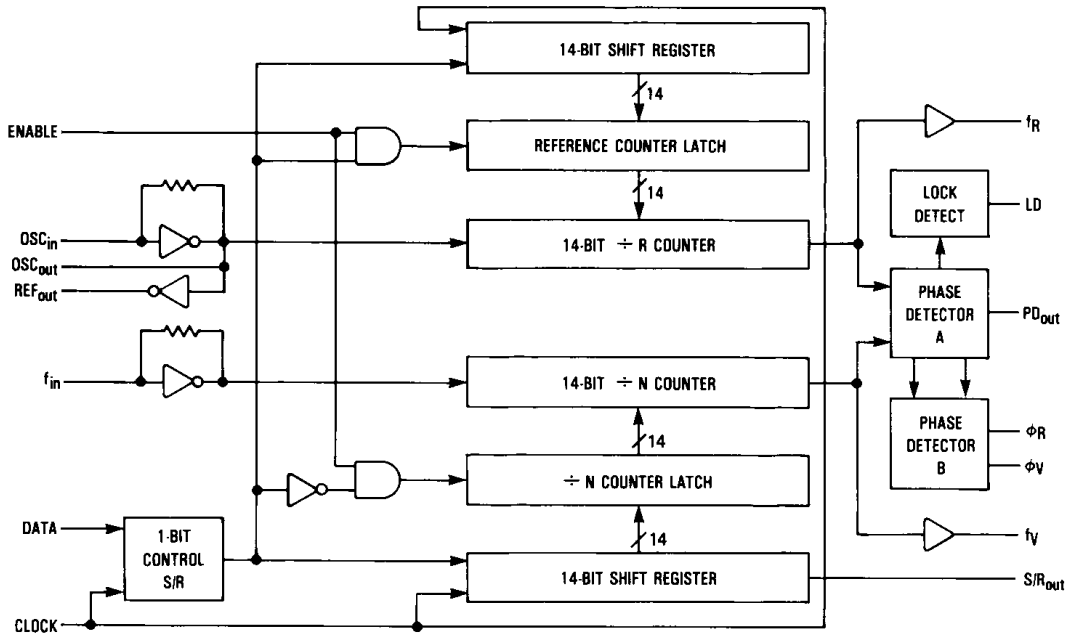
FN SUFFIX
PLCC
CASE 775

**ORDERING INFORMATION**

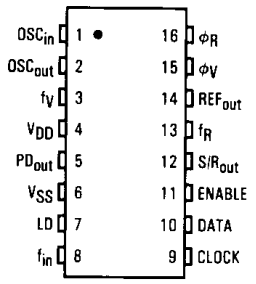
| | |
|---|---|
| MC145157P2 | Plastic DIP |
| MC145157DW2 | SOG Package |
| MC145157FN2 | PLCC Package |

5

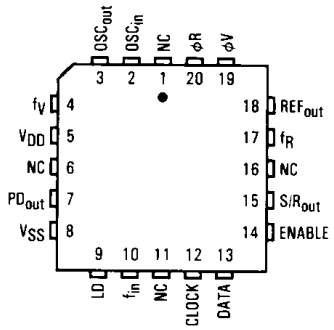
**BLOCK DIAGRAM**



## PIN ASSIGNMENTS




PLASTIC DIP
SOG PACKAGE




PLCC PACKAGE

## PIN DESCRIPTIONS

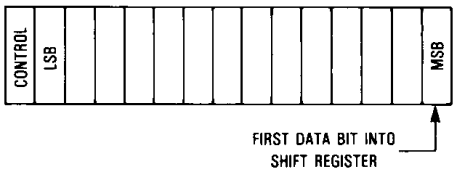
### INPUTS

#### $f_{in}$—Frequency Input

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p-p. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

#### CLOCK, DATA—Shift Clock, Serial Data Inputs

Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic one selects the reference counter latch and a logic zero selects the ÷ N counter latch. The data entry format is as follows:




#### ENABLE—Latch Enable Input

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. Enable is normally low and is pulsed high to transfer data to the latches.

#### $OSC_{in}$, $OSC_{out}$—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from $OSC_{in}$ to ground and $OSC_{out}$ to ground. $OSC_{in}$ may also serve as input for an externally-generated reference signal. This signal is typically ac coupled to $OSC_{in}$, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to $OSC_{out}$.

### OUTPUTS

#### $PD_{out}$—Phase Detector A Output

This single ended (three-state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or $f_V$ Leading: Negative Pulses
Frequency $f_V < f_R$ or $f_V$ Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

#### $\phi V$, $\phi R$—Phase Detector B Outputs

Double-ended phase detector outputs. These outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see $PD_{out}$).

If frequency $f_V$ is greater than $f_R$ or if the phase of $f_V$ is leading, then error information is provided by $\phi V$ pulsing low. $\phi R$ remains essentially high.

If the frequency $f_V$ is less than $f_R$ or if the phase of $f_V$ is lagging, then error information is provided by $\phi R$ pulsing low. $\phi V$ remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both $\phi V$ and $\phi R$ remain high except for a small minimum time period when both pulse low in phase.

#### $f_R$, $f_V$—R Counter Output, N Counter Output

Buffered, divided reference and $f_{in}$ frequency outputs. The $f_R$ and $f_V$ outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

#### LD—Lock Detector Output

This output is essentially at a high level when the loop is locked ($f_R$, $f_V$ of same phase and frequency), and pulses low when loop is out of lock.

**$REF_{out}$ – Buffered Oscillator Output**

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

**$S/R_{out}$ – Shift Register Output**

This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

**POWER SUPPLY**

**$V_{DD}$**

The positive power supply potential. This pin may range from +3 to +9 V with respect to $V_{SS}$.

**$V_{SS}$**

The most negative supply potential. This pin is usually ground.