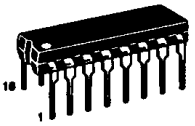
MC145168
MC145169

Advance Information

Dual PLLs for 46/49 MHz Cordless Telephones

CMOS



P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG
CASE 751G

These devices are dual phase-locked loop frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 15 channels. These parts contain two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Other features include a lock detect circuit for the transmit loop, illegal code default, a buffered oscillator output for mixing purposes in the system, and a 5.0 kHz tone output.

- Maximum Operating Frequency: 60 MHz @ V_{in}=200 mV p-p
- Operating Temperature Range: –40°C to 75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On-Chip Oscillator Circuit Supports External Crystal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Lock Detect Signal
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V
- Two Versions:
  - MC145168—Up to 15-Channel ROM with 4-Bit Binary Code Input for Channel Pair Selection
  - MC145169—Up to 15-Channel ROM with Serial Interface for Channel Pair Selection
- Custom 20-Channel ROM Versions of the MC145169 are Possible; Consult Factory

ORDERING INFORMATION

MC145168P	Plastic DIP
MC145168DW	SOG Package
MC145169P	Plastic DIP
MC145169DW	SOG Package

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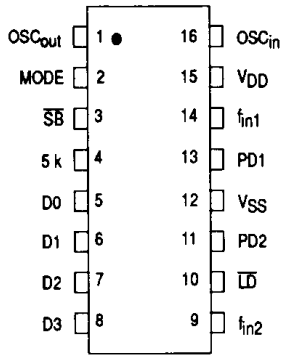
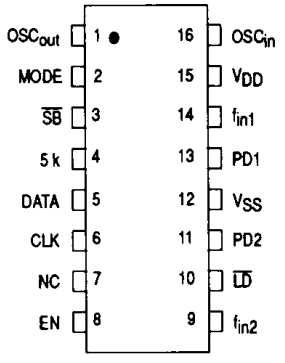
MC145168



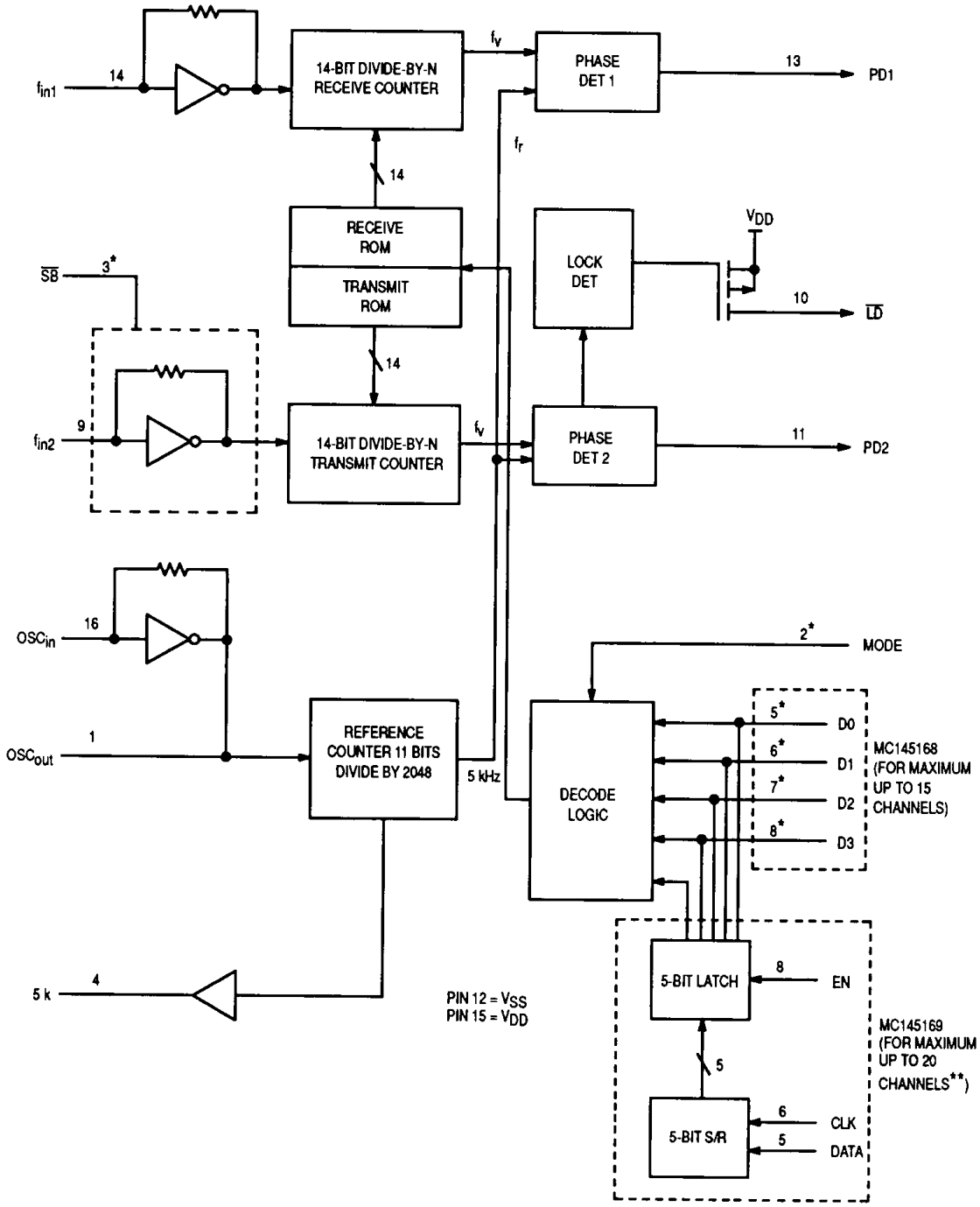
MC145169



NC=NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



*On chip pull down.

**The standard MC145169 is 15 channels; see Tables 1 and 2. Custom versions up to 20 channels are possible.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	Input Voltage, All Inputs	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	−65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=25°C)

Symbol	Characteristic		V_{DD}	Guaranteed Limit		Unit
				Min	Max	
V_{DD}	Power Supply Voltage Range		—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out}=0)	0 Level	2.5 5.5	— —	0.05 0.05	V
V_{OH}	(V_{in}=V_{DD} or 0)	1 Level	2.5 5.5	2.45 5.45	— —	V
V_{IL}	Input Voltage (V_{out}=0.5 V or V_{DD}−0.5 V)	0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}		1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out}=2.2 V) (V_{out}=5.0 V)	Source	2.5 5.5	−0.18 −0.55	— —	mA
I_{OL}	(V_{out}=0.3 V) (V_{out}=0.5 V)	Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in}=0)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	−30 −66	µA
		Data, $\overline{SB}$, Mode	2.5 5.5	— —	−0.05 −0.11	
I_{IH}	(V_{in}=V_{DD}−0.5)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	30 66	µA
		Data, $\overline{SB}$, Mode	2.5 5.5	— —	50 121	
C_{in}	Input Capacitance		—	—	8.0	pF
C_{out}	Output Capacitance		—	—	8.0	pF
I_{DD}	Standby Current, $\overline{SB}$=V_{SS} or Open		2.5 5.5	— —	1.4 3.6	mA
I_{dd}	Operating Current (200 mV p-p input at f_{in1}, f_{in2}, $\overline{SB}$=V_{DD})		2.5 5.5	— —	2.8 6.2	mA
I_{OZ}	Three-State Leakage Current (V_{out}=0 V or 5.5 V)		5.5	—	±1.0	µA

SWITCHING CHARACTERISTICS (T_A=25°C, C_L=50 pF)

Symbol	Characteristic		V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time (Figures 1 and 5)		3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time (Figures 1 and 5)		3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in} (Figure 2)		3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency Input=Sine Wave 200 mV p-p	OSC_{in} f_{in1} f_{in2}	3.0-5.0 3.0-5.0 3.0-5.0	— — —	12 60 60	MHz
t_{su}	Setup Time (MC145169) (Figure 3)	Data to Clock	3.0 5.0	100 50	— —	ns
		Enable to Clock	3.0 5.0	200 100	— —	
t_h	Hold Time (MC145169), Clock to Data (Figure 3)		3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time (MC145169), Enable to Clock (Figure 3)		3.0 5.0	80 40	— —	ns
t_w	Input Pulse Width (MC145169), Clock and Enable (Figure 4)		3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

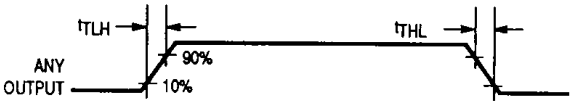


Figure 1.

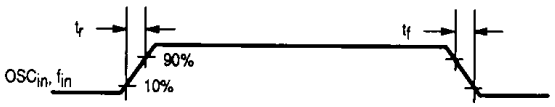


Figure 2.

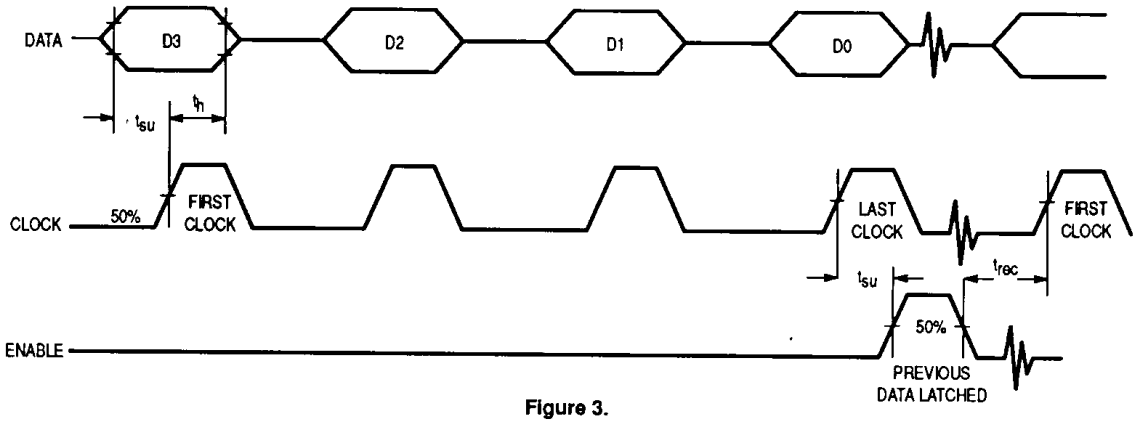


Figure 3.

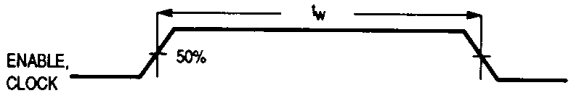


Figure 4.

PIN DESCRIPTIONS

INPUTS

OSC_{in}, OSC_{out} (Pins 16, 1)

These pins form a reference oscillator when connected to an external parallel-resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac-coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

Mode (Pin 2)

Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull down device.

$\overline{SB}$ (Pin 3)

The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull down device.

D0 through D3 (Pins 5, 6, 7, 8) — MC145168 only

These inputs provide the 4-bit binary code for selecting the one of 15 channels for the transmit and receive loops. When address data other than 1–15 are input, the decoding logic defaults to channel 1. The frequency assignments, with reference to Mode and D0–D3, are shown in Tables 1 and 2. These inputs have internal pull down devices.

f_{in1}, f_{in2} (Pins 14, 9)

f_{in1} and f_{in2} are inputs to the divide-by-N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. The mininum input level is 200 mV p-p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

Data, Clk (Pins 5, 6) — MC145169 only

These pins provide the binary input by using serial channel programming. A logic high represents a "1." Each low-to-high transition of the clock shifts one bit of data into the on-chip shift register. Data is entered MSB first, see Figure 3.

EN (Pin 8) — MC145169 only

The enable pin controls the data transfer from the shift register to the latch. A positive pulse transfers the data. This pin should normally be held low to avoid loading erroneous data into the latch.

OUTPUTS

5 k (Pin 4)

This is a 5 kHz tone signal derived from the reference oscillator. This pin is a push pull output.

$\overline{LD}$ (Pin 10)

Lock detect signal associated with the transmit loop. The lock output goes high to indicate an out-of-lock condition. This is a P-channel open-drain output.

PD1, PD2 (Pins 13, 11)

These are 3-state outputs of the transmit and receive phase detectors for use as loop error signals.

Frequency $f_V > f_r$ or f_V leading: Negative pulses

Frequency $f_V < f_r$ or f_V lagging: Positive pulses

Frequency $f_V = f_r$ and phase coincidence: High impedance state

NOTE: f_V is the output of the N counter. f_r is the output of the reference counter.

POWER

V_{SS} (Pin 12)

This pin is the negative supply potential and is usually ground.

V_{DD} (Pin 15)

This pin is the positive supply potential and may range from +2.5 to +5.5 volts with respect to V_{SS}.

Table 1. Handset Frequencies of Each Corresponding Channel in a 46/49 MHz Cordless Phone for the Korean Market

Channels					RX Freq. (MHz)	Receive (Note 3)		TX Freq. (MHz)	Transmit		Mode
D3	D2	D1	D0	CH#		f_{in1} (MHz)	+N		f_{in2} (MHz)	+N	
0	0	0	1	1	46.610	35.915	7183	49.670	49.670	9934	0
0	0	1	0	2	46.630	35.935	7187	49.845	49.845	9969	0
0	0	1	1	3	46.670	35.975	7195	49.860	49.860	9972	0
0	1	0	0	4	46.710	36.015	7203	49.770	49.770	9954	0
0	1	0	1	5	46.730	36.035	7207	49.875	49.875	9975	0
0	1	1	0	6	46.770	36.075	7215	49.830	49.830	9966	0
0	1	1	1	7	46.830	36.135	7227	49.890	49.890	9978	0
1	0	0	0	8	46.870	36.175	7235	49.930	49.930	9986	0
1	0	0	1	9	46.930	36.235	7247	49.990	49.990	9998	0
1	0	1	0	10	46.970	36.275	7255	49.970	49.970	9994	0
1	0	1	1	11	46.510	35.815	7163	49.695	49.695	9939	0
1	1	0	0	12	46.530	35.835	7167	49.710	49.710	9942	0
1	1	0	1	13	46.550	35.855	7171	49.725	49.725	9945	0
1	1	1	0	14	46.570	35.875	7175	49.740	49.740	9948	0
1	1	1	1	15	46.590	35.895	7179	49.755	49.755	9951	0

NOTES:
1. 0=logic low, 1=logic high.
2. Power up and illegal inputs are defaulted to channel 1 in the MC145169. Illegal inputs are defaulted to channel 1 in MC145168.
3. 1st IF frequency of receive is 10.695 MHz, 2nd IF is 455 kHz.
4. $+N=\frac{f_{in}}{f_{ref}}$ where f_{in} is the VCO frequency and f_{ref} is the reference frequency (5.0 kHz).

Table 2. Base Frequencies of Each Corresponding Channel in a 46/49 MHz Cordless Phone for the Korean Market

Channels					RX Freq. (MHz)	Receive (Note 3)		TX Freq. (MHz)	Transmit		Mode
D3	D2	D1	D0	CH#		f_{in1} (MHz)	+N		f_{in2} (MHz)	+N	
0	0	0	1	1	49.670	38.975	7795	46.610	46.610	9322	1
0	0	1	0	2	49.845	39.150	7830	46.630	46.630	9326	1
0	0	1	1	3	49.860	39.165	7833	46.670	46.670	9334	1
0	1	0	0	4	49.770	39.075	7815	46.710	46.710	9342	1
0	1	0	1	5	49.875	39.180	7836	46.730	46.730	9346	1
0	1	1	0	6	49.830	39.135	7827	46.770	46.770	9354	1
0	1	1	1	7	49.890	39.195	7839	46.830	46.830	9366	1
1	0	0	0	8	49.930	39.235	7847	46.870	46.870	9374	1
1	0	0	1	9	49.990	39.295	7859	46.930	46.930	9386	1
1	0	1	0	10	49.970	39.275	7855	46.970	46.970	9394	1
1	0	1	1	11	49.695	39.000	7800	46.510	46.510	9302	1
1	1	0	0	12	49.710	39.015	7803	46.530	46.530	9306	1
1	1	0	1	13	49.725	39.030	7806	46.550	46.550	9310	1
1	1	1	0	14	49.740	39.045	7809	46.570	46.570	9314	1
1	1	1	1	15	49.755	39.060	7812	46.590	46.590	9318	1

NOTES:
1. 0=logic low, 1=logic high.
2. Power up and illegal inputs are defaulted to channel 1 in the MC145169. Illegal inputs are defaulted to channel 1 in MC145168.
3. 1st IF frequency of receive is 10.695 MHz, 2nd IF is 455 kHz.
4. $+N=\frac{f_{in}}{f_{ref}}$ where f_{in} is the VCO frequency and f_{ref} is the reference frequency (5.0 kHz).

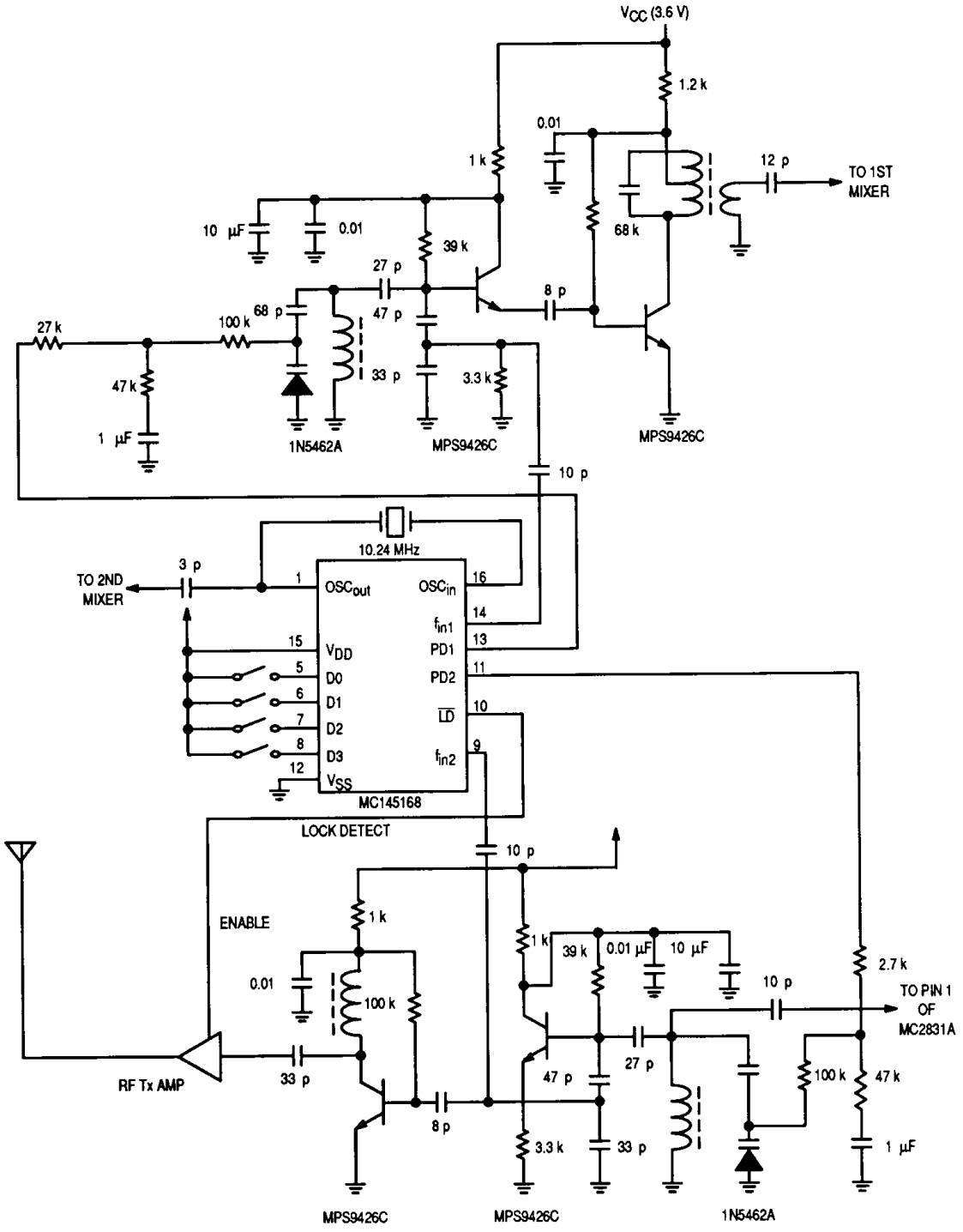


Figure 5. MC145168 Circuit Example

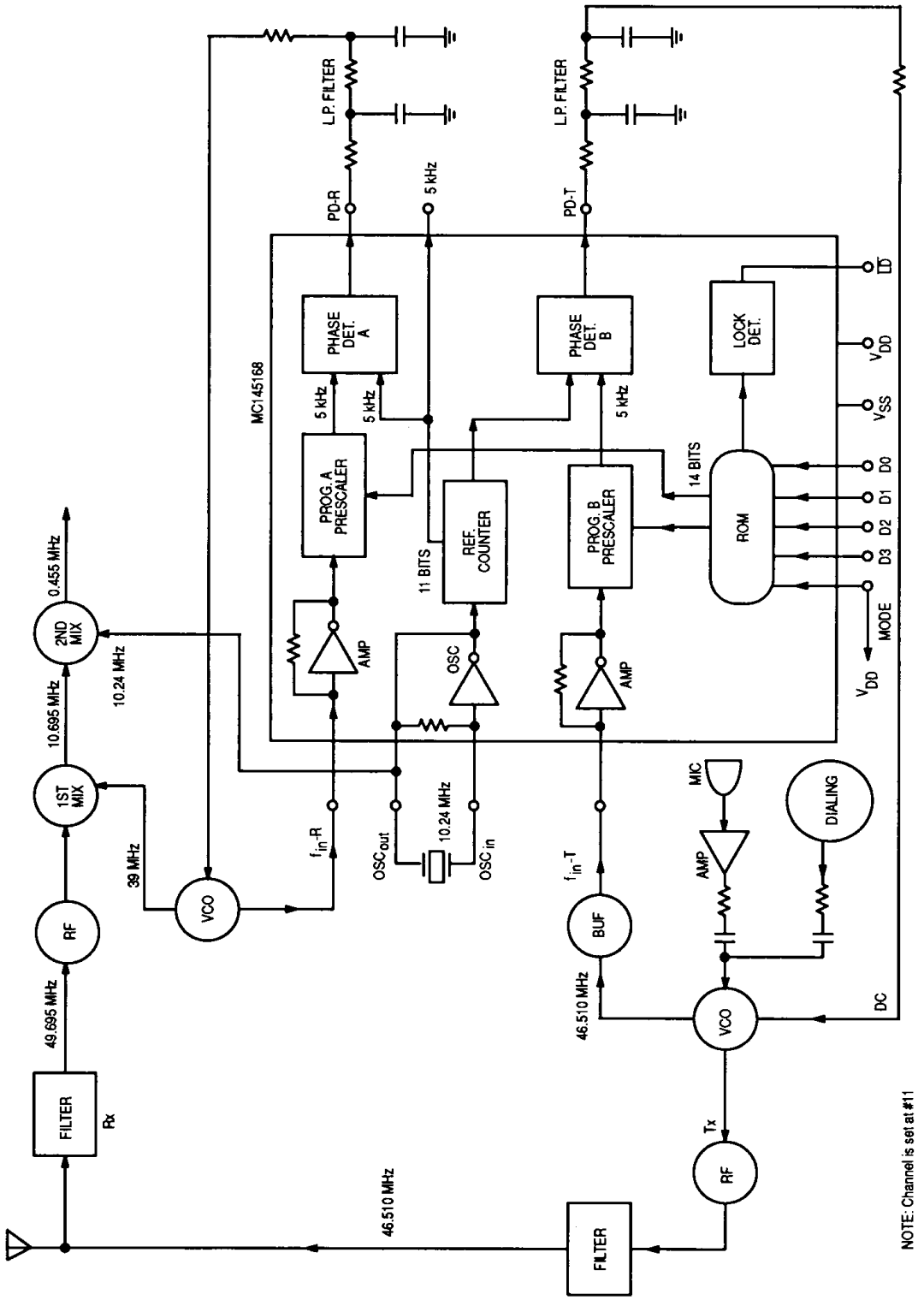


Figure 6a. DPLL Application in 46/49 MHz Cordless Phone 15-Channel Base

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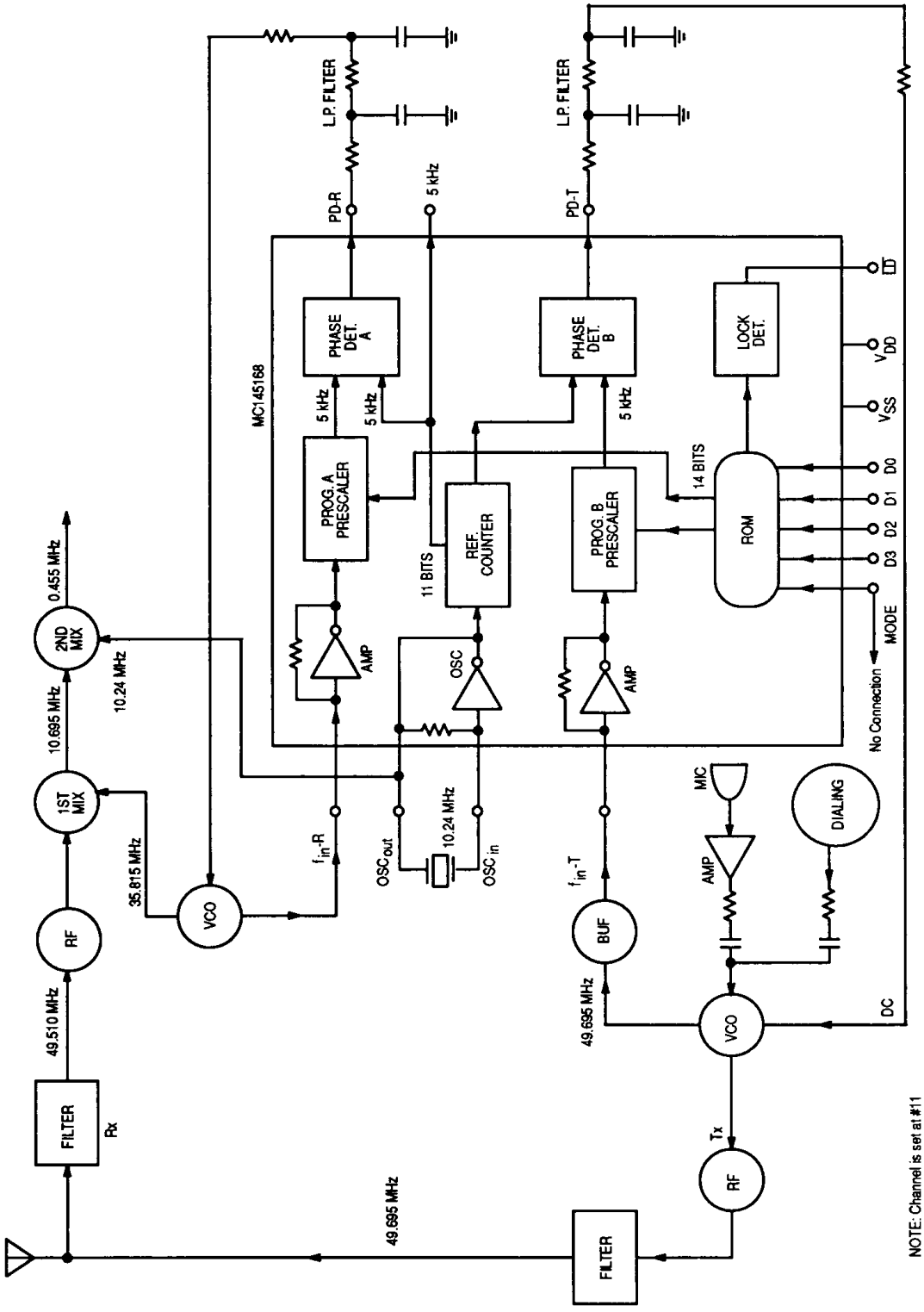

Figure 6b. DPLL Application In 46/49 MHz Cordless Phone 15-Channel Handset