Technical Summary
Token Bus Controller

The MC68824 token bus controller (TBC) is a silicon integrated circuit, which implements the media access control (MAC) function for an IEEE 802.4 local area network (LAN) station and the receiver portion for IEEE 802.2 logical link control (LLC) type 3 as well as providing support for LLC type 1 and type 2 (see Figure 1). IEEE 802.4 defines the physical and MAC portion of the data link layer of the GM Manufacturing Automation Protocol (MAP) specification. The LLC functions implemented on chip are those associated with real-time applications, namely Acknowledged Connectionless Service (type 3) as required in the enhanced performance architecture (EPA) specified in MAP 3.0.
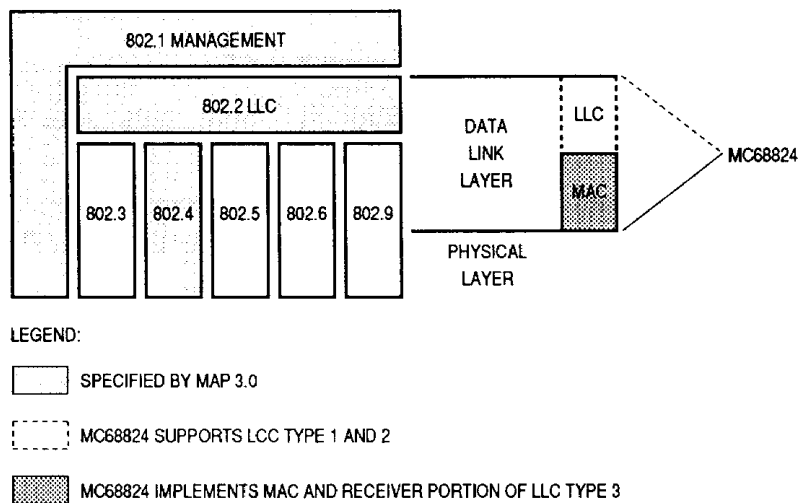
The major features of the TBC are as follows:

- Implementation of the MAC Portion of the IEEE 802.4 Standard

- Implementation of the Receiver Portion of IEEE 802.2 LLC Acknowledged Connectionless Service (Type 3)

- Support of IEEE 802.2 LLC Type 1 and Type 2

- Support of ANSI/ISA-72.01 PROWAY PLC Send Data with Acknowledge (SDA) and Request Data with Reply (RDR)

- MAC Options Suitable for Real-Time Environments
  — Four Receive and Four Transmit Queues Supporting Four Priority Levels
  — Immediate Response Mechanism

- On-Chip Network Monitoring and Diagnostics

- Simple Interface to Higher Level Software using Powerful, Fully Linked Data Structure

- Options For Bridging Include Hierarchical and IBM® Defined Source Routing As Well As Support for Flat Bridges

- Powerful Addressing: Group Address Recognition and Multidrop Capability

8

IBM is a trademark of International Business Machines.

Features (Continued)

- System Clock Rate up to 16.67 MHz
- Serial Data Rates from 10 Kbps to 12.5 Mbps
- IEEE 802.4 Recommended Serial Interface Supporting Various Physical Layers
- Highly Integrated M68000 Family Bus Master/Slave Interface
  — Four-Channel DMA for Transfer of Data Frames to and from Memory
    - 40-Byte FIFO To Efficiently Support High Data Rate
    - 32-Bit Address Bus with Virtual Address Capabilities
- Simplified Interface to Other Processor Environments
  — Byte-Swapping Capability for Alternate Memory Structures
  — 8- or 16-Bit Data Bus
- Low Power Consumption through 1.5-μm HCMOS Fabrication
- Contains Several Modes To Increase Reliability and Flexibility:
  — Reduced Data Structure Mode for Increased Performance
  — Control Frame Preference for Increased Reliability
  — Address Comparison Options for Increased Performance
  — Bus Analyzer Mode To Enable Running the TBC as a Powerful Protocol Analyzer

LEGEND:

SPECIFIED BY MAP 3.0

MC68824 SUPPORTS LCC TYPE 1 AND 2

MC68824 IMPLEMENTS MAC AND RECEIVER PORTION OF LLC TYPE 3

Figure 1. IEEE Standard Model

GENERAL DESCRIPTION

The TBC functions as an intelligent peripheral device to a microprocessor. An on-chip DMA transfers data frames to and from a buffer memory with minimal microprocessor interference required. A microcoded, fully linked buffer management scheme queues frames during transmission and reception and optimizes memory use. The TBC simplifies interfacing a microcomputer to a token bus network by providing the following link layer services: managing ordered access to the token bus medium, providing a means for admission and deletion of stations, and handling fault recovery. This provision allows the host to operate almost totally isolated from the task of ensuring error-free transmission and reception of data.

The TBC can be used in a variety of machines in the factory from programmable controllers to large computers. Although the token bus is especially well suited to the factory because of its deterministic characteristics, the TBC can be used in other networking applications such as office automation. The TBC provides the capability to swap the byte ordering of data to support alternate memory organizations. Additionally, the TBC is a full M68000 bus master, providing on-chip direct memory access (DMA) capability for management of memory tables and frame buffers. Since the TBC bus interface is configurable, the TBC can handle both 8- and 16-bit data transfers. Figure 2 shows the TBC in a typical intelligent I/O processor system environment.
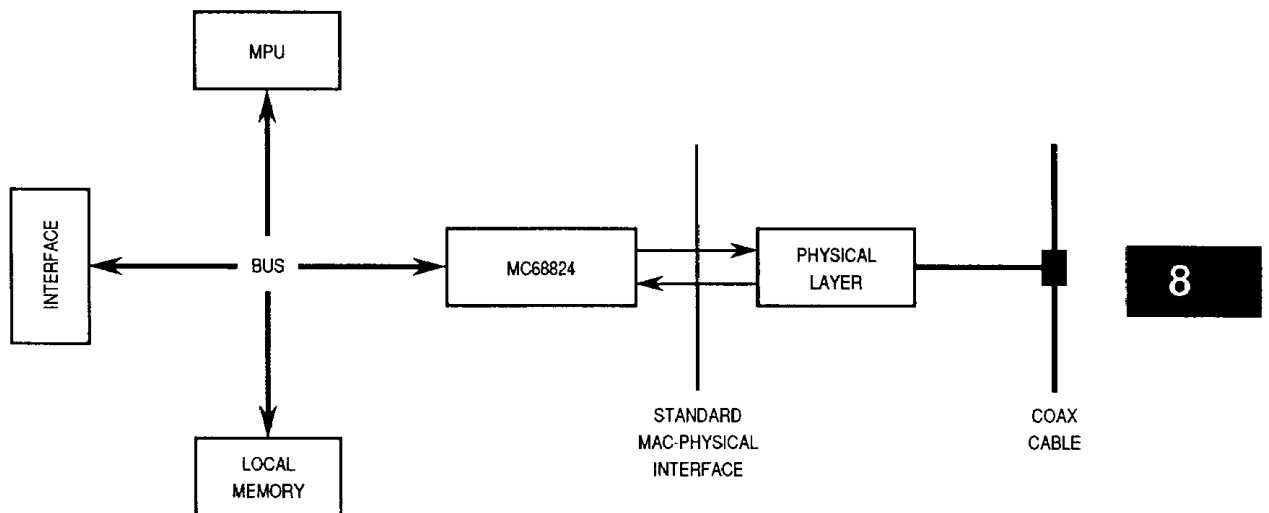

Figure 2. Token Bus LAN Node

The following sections summarize the TBC operational modes, data structures, and commands. Refer to Table 1 for an explanation of the acronyms used throughout this document.

Table 1. Acronyms

Acronym	Definition	Acronym	Definition
ACM	Access Control Machine	LLC	Logical Link Control
BD	Buffer Descriptor	LSAP	Link Service Access Point
CRC	Cyclic Redundancy Check	LSDU	Link Service Data Unit
DA	Destination Address	MAC	Media Access Control
DB	Data Buffer	RDS	Reduced Data Structure
DMA	Direct Memory Access	RWR	Request with Response
DSAP	Destination Service Access Point	RX	Receive
EOQ	End of Queue	SA	Source Address
EPA	Enhanced Performance Architecture	SSAP	Source Service Access Point
		TBC	Token Bus Controller
FC	Frame Control	TS	This Station Address
FD	Frame Descriptor	TX	Transmit
HOQ	Head of Queue		
IA	Individual Address		

INTERNAL ARCHITECTURE

The TBC has four functional blocks: serial, DMA, microcoded controller, and register file/ALU. Each section contains user-visible and nonvisible registers that define control and operation of the TBC. A block diagram of the TBC is shown in Figure 3.

Because the TBC communicates with the host primarily through shared memory, minimal host processor accessible registers are required. These directly accessible registers include the command register, semaphore register, interrupt vector register, and data register. Internal registers not directly accessible to the host processor can be accessed through the initialization table in shared memory.

OPERATIONAL MODES

The MC68824 has three main operational modes: TBC mode, EPA mode, and bus analyzer mode. In the TBC mode, which is the default mode, the MC68824 provides a full MAC implementation; it only supports and does not implement LLC type 3. Running in the default mode allows the user to perform the LLC functions or equivalent in software. In the EPA mode, the MC68824 performs the receiver portion of the acknowledged connectionless service of the LLC type 3 sublayer, as well as operating normally when a nonrequest with response frame is received. In the bus analyzer mode, the MC68824 is not part of the logical ring. In this mode, the MC68824 receives all frames, making the TBC an ideal chip to be used in a protocol analyzer application. The MC68824 also offers several additional modes and options to tailor the TBC to a specific application. The TBC/EPA mode is selected via the mode selector word located in the initialization table. Several other options are available to the user by using the SET MODE commands. Table 2 summarizes all modes available on the MC68824 while running in either the TBC or EPA mode except where noted. Refer to Table 1 for definitions of acronyms.
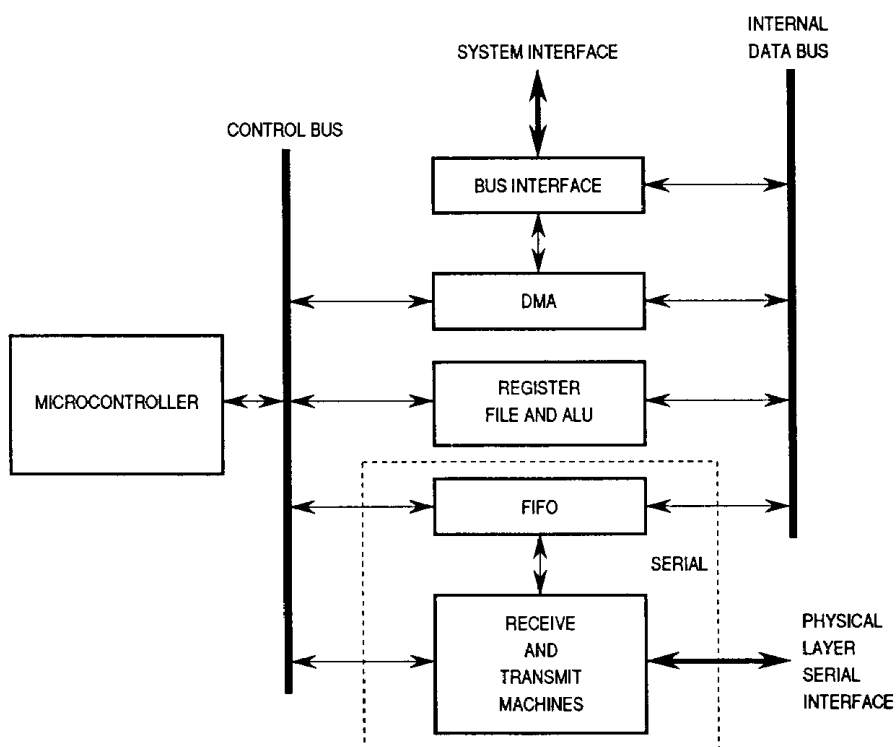

Figure 3. TBC Block Diagram

Table 2. Modes and Options

Mode	Description	Selected By
EPA	Enables the TBC to implement LLC type 3 functions. The TBC mode is the default	Mode Selector Word
Reduced Data Structure	Optimizes the number of back-to-back frames the TBC can receive by modifying the frame structures in memory	Mode Selector Word
Copy All Data Frames	Determines whether the TBC copies to memory all non-RWR data frames that are heard. Station may still be part of logical ring. Useful mode for bridge implementations. Valid only in reduced data structure mode.	Mode Selector Word
Control Frames Preference	Ensures that the TBC will not lose control frames if adequate system performance is provided	Mode Selector Word
No Mask Mode	Indicates to the TBC that only individually addressed frames with DA = TS exactly or all group addressed frames, regardless of the mask, will be received	Mode Selector Word
Receive Erroneous Frames in RDS	Allows the TBC to store erroneous frames while in the reduced data structure mode	Mode Selector Word
MAC Address Length	Allows the user to select 16- or 48-bit MAC addresses	Mode Selector Word
Bus Analyzer	Enables the bus analyzer mode	SET MODE 1
Copy Frames with Undefined FC	Allows user to store frames with undefined frame control	SET MODE 1
Copy All Control Frames	May be used to set the TBC in promiscuous mode to monitor network traffic	SET MODE 1
Limited Statistics Tracking	TBC can keep track of all statistics or of a subset (see Initialization Table).	SET MODE 1
Response SA Filtering	Allows the TBC to selectively store response frames according to a mask on the SA while running in the EPA mode only	SET MODE 1
Lower Bridge Mode	Puts the TBC in lower bridge mode used in hierarchical bridging	SET MODE 2
In_Ring Desired	Determines whether or not the TBC is a member of the logical ring while in the steady-state condition	SET MODE 2
Source Routing Limited Broadcast	If source routing is enabled, then broadcast frames can be recognized.	SET MODE 2
Bridge Delay Mode	To be used in bridges when SA can be unequal to TS for long-distance broadband networks	SET MODE 2
Recognize Source Routing	Allows the TBC to act as part of a source routing bridge between interconnected networks	SET MODE 2
Copy CRC to Memory	Causes the TBC to copy the 4-byte CRC of data frames to memory as part of the data unit	SET MODE 3
Suppress CRC Generation (All Frames)	Disables CRC generation for all data frames transmitted by the TBC	SET MODE 3

8

Table 2. Modes and Options (Continued)

Mode	Description	Selected By
Halt Generator Enable	Controls the maximum number of DMA transfers that the TBC performs in one DMA burst	SET MODE 3
Data Byte Swap Mode	Allows the user to select either the Motorola/IBM or the Intel(™)/DEC(™) data organization for data buffers	SET MODE 3
Prescaler	Determines whether a prescaler of 3 or 6 should be used for octet timers	SET MODE3
Flow Control	Enables the flow control algorithm to allow the user to selectively copy RWR frames to memory while in the EPA mode only	LSAP Only
Suppress CRC Generation (Per Frame)	Disables transmission of CRC on a frame-by-frame basis	Frame Only

Intel is a trademark of Intel Corporation.
DEC is a trademark of Digital Equipment Corporation.

SHARED MEMORY STRUCTURES

The TBC and host processor communicate through a memory structure consisting of two tables and a fully linked buffer structure. The initialization table allows the host processor to set and update the TBC operating parameters and table pointers and to receive status and error information. The TBC is given a pointer to the initialization table during initialization. The private area is the other table used by the TBC to store MAC parameters. The fully linked buffer structure consists of frame descriptors, buffer descriptors, and data buffers. There is one frame descriptor for each frame. Each frame descriptor contains pointers to a buffer descriptor which in turn points to a data buffer where the message data is stored. If more than one data buffer is needed, the buffer descriptor will point to another buffer descriptor which, in turn, points to another data buffer.

8

INITIALIZATION TABLE

The initialization table format is listed in Table 3. The first 124 bytes (0-7C hex) initialize the TBC and the TBC private area in memory. The command parameter area (CPA) is most frequently used by the host to set and read internal TBC parameters. The CPA is divided into the command area and the command return area. The commands dedicated to reading and setting internal TBC parameters are SET ONE WORD, SET TWO WORDS, and READ VALUE.

Table 3. Initialization Table Format

Displacement In Hex Bytes	Description of Field
00	Private Area Function Code
02	Private Area Pointer High
03	Private Area Pointer Low
05	Zero
08	Initial Hi_Priority_Token_Hold_Time
0A	Zero
0C	Zero
0E	Initial Target_Rotation_Time for Access Class 4
10	Zero
12	Initial Target_Rotation_Time for Access Class 2
14	Zero
16	Initial Target_Rotation_Time for Access Class 0
18	Zero
1A	Initial Target_Rotation_Time for Ring Maintenance Initial Ring Maintenance Time Initial Value
1C	Initial Source Segment/Bridge ID (SID)
1E	
20	Initial Target Segment/Bridge ID (TID)
22	Initial Segment Number Mask for Source Routing
24	Initial Max_Inter_Solicit_Count
26	Initial RX Frame Status Error Mask
28	Initial TX Queue Access Class 6 Status
2A	Initial TX Queue Access Class 6 HOQ Pointer
2E	Zero
30	Initial TX Queue Access Class 4 Status
32	Initial TX Queue Access Class 4 HOQ Pointer
36	Zero
38	Initial TX Queue Access Class 2 Status
3A	Initial TX Queue Access Class 2 HOQ Pointer
3E	Zero
40	Initial TX Queue Access Class 0 Status
42	Initial TX Queue Access Class 0 HOQ Pointer
46	Zero
48	Initial RX Queue Access Class 6 EOQ Pointer
4C	Initial RX Queue Access Class 4 EOQ Pointer
50	Initial RX Queue Access Class 2 EOQ Pointer
54	Initial RX Queue Access Class 0 EOQ Pointer
58	Initial Free Frame Descriptor Pool Pointer to First FD Initial Free Buffer Descriptor Pool Pointer to First BD
5C	
60	Initial Group Address Mask — Low
62	Initial Group Address Mask — Medium
64	Initial Group Address Mask — High
66	Initial Individual Address Mask — Low
68	Initial Individual Address Mask — Medium
6A	Initial Individual Address Mask — High
6C	Initial Non-RWR Maximum Retry Limit
6E	Initial RWR Maximum Retries Limit

Table 3. Initialization Table Format (Continued)

Displacement In Hex Bytes	Description of Field
70	Initial Slot Time
72	Initial This Station Address — Low
74	Initial This Station Address — Medium
76	Initial This Station Address — High
78	Initial Pad Timer Preset (PTP)
7A	Mode Selector Word
7C*	Response SA Mask — Low
7E*	Response SA Mask — Medium
80*	Response SA Mask — High
82	Zero
84**	Response Destination Address Pointer
88**	Response Pointer
8C**	RWR Pointer
Command Parameter Area	
90	Command Parameter Area VAL0
92	Command Parameter Area VAL1
94	Command Parameter Area VAL2
96	Command Return Area RET0
98	Command Return Area RET1
9A	Command Return Area RET2
9C	Command Status and Done Bit
9E	Zero
A0	Zero
A2	Zero
A4	Zero
A6	Zero
Interrupt Status Area	
A8	Interrupt Status Word 0
AA	Interrupt Mask 0
AC	Interrupt Status Word 1
AE	Interrupt Mask 1
Statistics	
B0	Number of Tokens Passed (Threshold)
B2	Number of Tokens Passed
B4	Number of Tokens Heard (Threshold)
B6	Number of Tokens Heard
B8	Number of Tokens Passed Through No_Successor_8 Arcs (Threshold)
BA	Number of Tokens Passed Through No_Successor_8 Arcs
BC	Number of Who_Follows Transmitted (Threshold)
BE	Number of Who_Follows Transmitted
C0	Number of Token Passes That Failed (Threshold)
C2	Number of Token Passes That Failed
C4	Number of Non-Silence (Threshold)
C6	Number of Non-Silence
C8	Number of FCS Errors (Threshold)
CA	Number of FCS Errors
CC	Number of E-Bit Errors (Threshold)
CE	Number of E-Bit Errors

8

Table 3. Initialization Table Format (Concluded)

Displacement In Hex Bytes	Description of Field
D0	Number of Tokens Passed (Threshold)
D2	Number of Tokens Passed
D4	Number of Tokens Heard (Threshold)
D6	Number of Tokens Heard
D8	Number of Tokens Passed Through No_Successor_8 Arcs (Threshold)
DA	Number of Tokens Passed Through No_Successor_8 Arcs
DC	Number of Who_Follows Transmitted (Threshold)
DE	Number of Who_Follows Transmitted
DMA Dump Area	
E0	FC1
E2	DPTR1
E6	FC2
E8	DPTR2
EC	FC3
EE	DPTR3
F2	FC4
F4	DPTR4
F8-FE	Zero

*In Response SA Filtering Mode Only
**See Table 4.

The TBC continuously updates the two interrupt status words as status changes. The interrupt status word, combined with the interrupt status mask, determines whether an interrupt will be generated. If an interrupt condition occurs and the corresponding bit in the interrupt status mask is set, the MC68824 will assert IRQ. The host must, after determining the interrupting event, issue a CLEAR INTERRUPT STATUS command to negate IRQ and clear the interrupt bit. The following list specifies the events updated in the interrupt status words by the TBC.
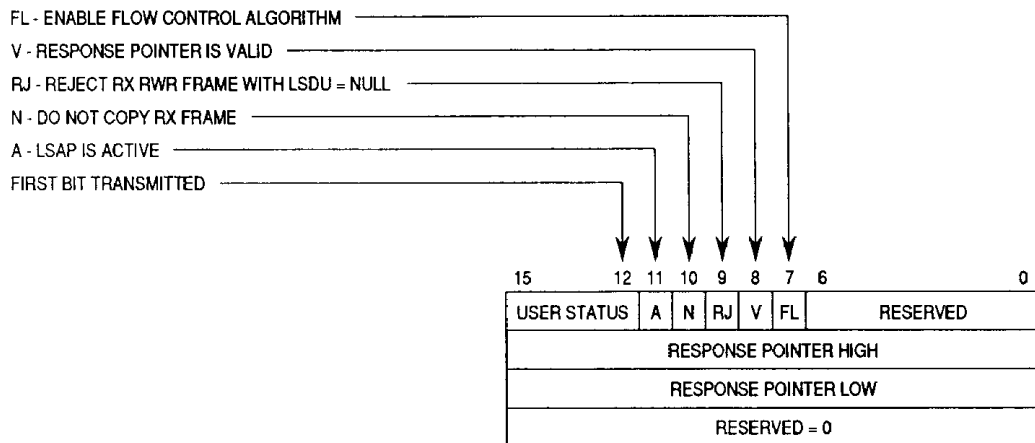
Interrupt Status Words Definitions

Interrupt Status Word 1	Interrupt Status Word 2
TBC Command Complete	Duplicate MAC Address Detected
Frame Descriptor Pool Empty	Faulty Transmitter
Buffer Descriptor Pool Empty	Successor Changed
Transmit Queue Empty	No Successor/No Successor 1
Token Skipped	Unexpected Frame 6
Token Passed	Solicit Any Arc of the ACM Performed
Bus/Address Error	Unexpected Frame 10
Frame Descriptor Pool Low	Receive Claim Token
Buffer Descriptor Pool Low	No Response Received (ACM in the Await Response State)
Overrun	Win Address Sort
Underrun	Bus Idle Timer Expired
Transmitted RWR Frame	Threshold Counter Exceeded
Transmitted Response Frame	Lose Address Sort
Transmitted Data Frame	Modem Error
Received RWR Frame	
Received Data Frame	

The initialization table also contains statistics about network operation. The statistics are 16-bit wraparound counters. Every counter has a threshold variable which the TBC checks against. If the threshold is reached, the host may be notified through the interrupt status bit. The host may select to collect all statistics or may disable the collection of the two most frequent statistics: number of tokens passed and number of tokens heard.

When the MC68824 is the EPA mode, the initialization table must be extended by 1024 words to accommodate the LSAP table. The LSAP table consists of 2 × 128 entries, one for each possible LSAP address, individual and group. Each of the first 128 entries represents an individual LSAP; each of the following 128 entries represents group LSAPs. Figure 4 shows the format of each entry in the LSAP table; Table 4 shows the entries in the initialization table which are different when the MC68824 is in the EPA mode.

8

Table 4. Initialization Table Entries in EPA Mode

Displacement in Hex Bytes	Description of Field
84	Not Used
86	Not Used
88	RX Retry RWR Frame – Threshold
8A	RX Retry RWR Frame – Counter
8C	RX RWR with LSDU = Null – Threshold
8E	RX RWR with LSDU = Null – Counter

```
FL - ENABLE FLOW CONTROL ALGORITHM ─────────────────────────┐
V - RESPONSE POINTER IS VALID ─────────────────────────┐    │
RJ - REJECT RX RWR FRAME WITH LSDU = NULL ─────────┐   │    │
N - DO NOT COPY RX FRAME ──────────────────────┐   │   │    │
A - LSAP IS ACTIVE ────────────────────────┐   │   │   │    │
FIRST BIT TRANSMITTED ─────────────────┐   │   │   │   │    │
                                       ▼   ▼   ▼   ▼   ▼   ▼
   15              12  11  10   9   8   7   6                    0
```

USER STATUS	A	N	RJ	V	FL	RESERVED
RESPONSE POINTER HIGH							
RESPONSE POINTER LOW							
RESERVED = 0							

Figure 4. LSAP Table Entry

Note that if the MC68824 is running in the EPA mode and the user wishes to enable the flow control mode, the initialization table must be extended beyond the LSAP table by 512 words to accommodate the message counter table.

PRIVATE AREA

The MC68824 private area is a 128-byte area of RAM reserved for use by the TBC to store internal variables and statistical information associated with the MAC operation. During initialization, the host specifies the appropriate initial values of the private area parameters in the initialization table (see displacement 08 hex through 76 hex in Table 3). The private area should never be directly accessed by the host as this would not guarantee IEEE 802.4 operation. The parameters in the private area must only be set and read by the SET/READ VALUE commands. When the MC68824 is operating in the EPA mode, the private area must be doubled to 256 bytes to provide extra storage to save protocol variables.

LINKED BUFFER STRUCTURES

The fully linked buffer structures include frame descriptors (FD), buffer descriptors (BD), and data buffers (DB). One FD is required per received or transmitted frame. Each FD contains information pertaining to the frame sent or received, a pointer to the next FD, and a pointer to its first BD. BDs contain the pointer to a DB as well as that buffer's attributes, and a pointer to the next BD in the frame if used. The DBs are used to store message data; one DB is associated with each BD. Figure 5 illustrates the linked buffer structure.
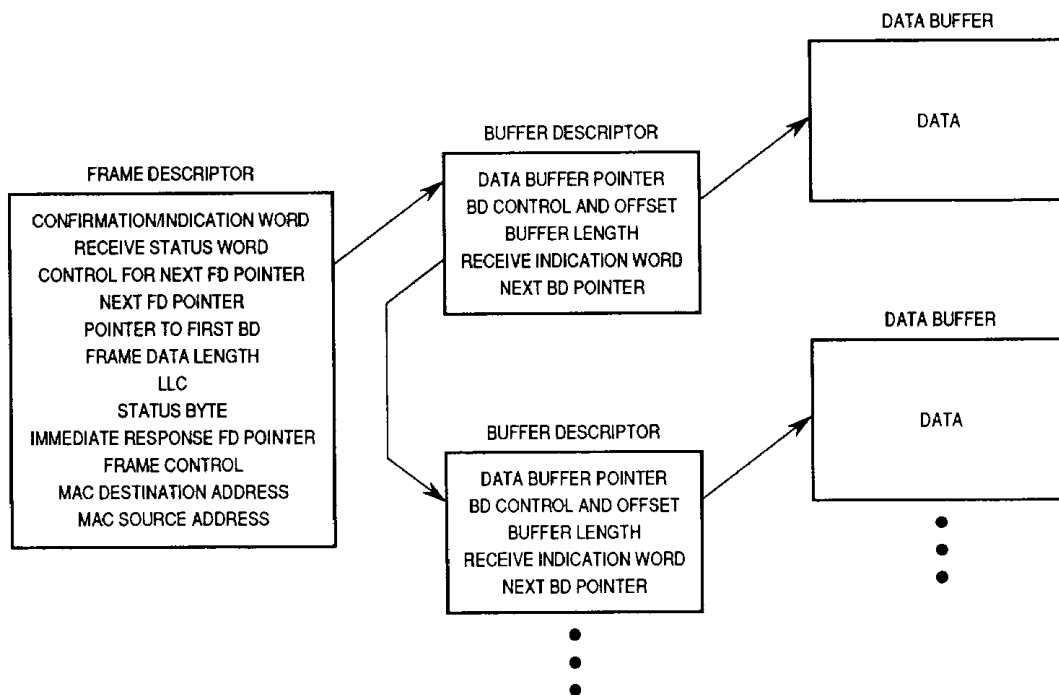
Figure 5. Linked Buffer Structure

To fully support the IEEE 802.4 message priorities, the TBC provides four transmit queues and four receive queues. Before transmission of a message, the host processor creates FDs, BDs, and DBs for that message and then links the FD to the appropriate transmit queue. Transmission queues may be enabled or disabled using the SET ONE WORD command. The TBC confirms transmission of the frames in each FD as they are sent out. During reception, the TBC reverses the process to use FDs and BDs from the prelinked free frame descriptors pool and free buffer descriptors pool as frames are received, assigning these frames to the proper reception queue. Receive queues may not be disabled. The free frame descriptor and free buffer descriptor pool pointers, which are located in the private area, must be valid at initialization time and may be changed thereafter using the SET TWO WORDS command while the TBC is OFFLINE. Finally, the host processor removes the frame data from these reception queues as programmed. Figure 6 illustrates the linking between the queues, FDs, BDs, and DBs.
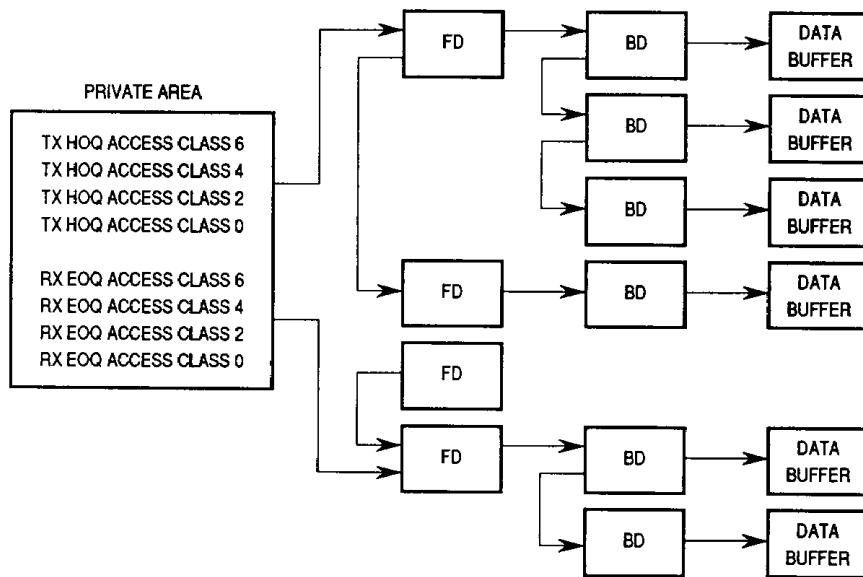
Figure 6. MC68824 Queues

If the MC68824 is programmed to run in the reduced data structure mode, a separate data structure is used for storing received frames while the TX frame queues structure remains the same as previously explained. In the reduced data structure mode, there is only one receive queue; frames of all priority classes are copied to the same receive queue.

COMMAND SET

The host processor issues commands to the TBC to perform various functions by writing to the TBC command register. The commands fall into seven categories listed in Table 5.

INITIALIZATION

Initialization commands configure the TBC for operation after a hardware or software reset. The five initialization commands specify various system attributes and the location of the initialization table in memory.

RESET Command

Both the RESET command and hardware reset cause the TBC to perform a reset operation.

Table 5. Commands by Categories

INITIALIZATION	TEST
LOAD INITIAL TABLE FUNCTION CODE INITIALIZE OFFLINE IDLE RESET	INTERNAL-EXTERNAL LOOPBACK MODE RECEIVER TEST TRANSMITTER TEST HOST INTERFACE TEST FULL-DUPLEX LOOPBACK TEST SELF-TEST MEASURE SLOT TIME
SET OPERATION MODE	**NOTIFY TBC**
SET MODE 0 SET MODE 1 SET MODE 2 SET MODE 3 SET/CLEAR IN_RING_DESIRED	CLEAR INTERRUPT STATUS RESPONSE READY SET RESPONSE
TRANSMIT DATA FRAMES	**MODEM CONTROL**
STOP RESTART START	PHYSICAL END PHYSICAL
SET/READ VALUE	
READ VALUE SET FUNCTION CODE OF BUFFER DESCRIPTORS SET FUNCTION CODE OF FRAME DESCRIPTORS SET FUNCTION CODE OF RX AND TX DATA BUFFERS SET PAD TIMER PRESET (PTP) REGISTER SET ONE WORD SET TWO WORDS UPDATE LSAP STATUS UPDATE LSAP COUNTERS RESET TRT	

OFFLINE Command

The OFFLINE command causes the TBC to transition to the offline state. The OFFLINE command is typically used to end an internal diagnostic test on the TBC.

8

IDLE Command

The IDLE command causes the TBC to transition from the offline state to the idle state. The IDLE command is used after initialization is complete.

LOAD INITIALIZATION TABLE FUNCTION CODE Command

The LOAD INITIALIZATION TABLE FUNCTION CODE command writes the initialization table function code value in the data register into the TBC and sets the bus width to 8 or 16 bits.

INITIALIZE Command

The INITIALIZE command loads the initialization table pointer from the data register and loads initial values from the initialization table into the TBC and the TBC private area. This command should only be given while in the offline state after reset.

SET OPERATION MODE

These five commands are used to set various operation modes and options in the TBC. Defaults are off except for the halt generator enable bit, which comes up set after a reset.

SET MODE 0 Command

The SET MODE 0 command allows the user to dynamically change the no mask mode, the control frames preference mode, and the ability to receive erroneous frames while in the reduced data structure mode. See Table 2 for a description of these modes.

SET MODE 1, 2, AND 3 Commands

The SET MODE 1, 2, and 3 commands are used at initialization to set up various options of the MC68824. See Table 2 for a description of these modes.

SET/CLEAR IN_RING_DESIRED Command

The SET/CLEAR IN_RING DESIRED command is used to change the value of the IEEE 802.4 boolean in_ring_ desired during normal operation.

TRANSMIT DATA FRAMES

Transmit data frames commands are used to stop/restart transmission of data frames or to start an empty transmission queue.

STOP Command

The STOP command suspends transmission of data frames by the TBC.

RESTART Command

The RESTART command restarts transmission of data frames by the TBC after transmission has been stopped via the STOP command.

START Command

The START command is used by the host processor whenever new frame(s) is (are) added to an empty transmit queue. Before issuing this command, the command parameter area must contain the code of the appropriate transmit queue status and the next two words must contain the pointer to the new frame(s).

SET/READ VALUE

These commands are used by the host processor to set and read TBC parameters. The parameters that may be modified include function codes, pad timer preset register, and some of the parameters residing in the private area or initialization table.

READ VALUE Command

The READ VALUE command reads internal TBC parameters and statistical information. The opcode of the parameter to be read is placed into the first word of the command parameter area, the read value command is issued, and the TBC returns the value of the parameter in the command return area in the initialization table.

SET ONE WORD/TWO WORDS Commands

The SET ONE WORD/TWO WORDS commands allow the user to set a number of MAC parameters and TBC pointers. The opcode of the parameter to be set must be placed in the first word of the command parameter area with the value in the next three words.

SET PTP Command

This command allows the user to set the pad timer preset register, which is used by the MC68824 to set the length and pattern of the preamble and the minimum number of preamble octets transmitted between frames.

SET FUNCTION CODES Commands

There are three commands available to the user to set the function codes. The MC68824 utilizes function codes to access the buffer descriptors, frame descriptors, and RX and TX data buffers. If function codes are not used, these commands may be ignored.

UPDATE LSAP STATUS Command

The UPDATE LSAP STATUS command can be used to activate, deactivate, or update user status when the TBC is on-line. This command can only be issued when the MC68824 is in the EPA mode.

UPDATE LSAP COUNTERS Command

The UPDATE LSAP COUNTERS command allows the user to set the flow control counters to new values without disabling the specific LSAP. This command can only be issued when the MC68824 is in the EPA mode and with the Flow control mode enabled.

RESET TRT Command

The RESET TRT command causes the MC68824 to reset the internal token rotation timer to zero. Since the last value of the token rotation timer is also returned to the host, this command may be used to make time calculations. This command must only be issued when the MC68824 is in the bus analyzer mode.

TEST

Test commands are used to test the interface from the host to the TBC, the transmitter, the receiver, and the serial section as well as the internal sections of the TBC.

SET INTERNAL/EXTERNAL LOOPBACK MODE Command

This command determines whether the TBC is in internal or external loopback mode while running the receiver, transmitter, and full-duplex loopback tests.

TEST Commands

Five tests can be run on the TBC while in the offline state: HOST INTERFACE TEST, RECEIVER TEST, TRANSMITTER TEST, FULL-DUPLEX LOOPBACK TEST, and SELF-TEST.

MEASURE SLOT TIME Command

The MEASURE SLOT TIME command is used when the MC68824 is offline to enable the user to monitor the length of a response window opened by a station already in the ring. Upon issuance of this command, the MC68824 waits until the first solicit_successor_1 frame is heard. Then, the time is measured until a successive token is heard.

NOTIFY TBC

The seven commands in this category are used to notify the TBC to dynamically perform an action.

CLEAR INTERRUPT STATUS Command

The CLEAR INTERRUPT STATUS command resets the interrupt request signal and clears specific status bits in the status words.

RESPONSE READY Command

The RESPONSE READY command notifies the TBC that the host has completed preparing a response frame for the TBC in answer to a request with response frame. This command is only valid when not in predefined response mode.

SET RESPONSE Command

The SET RESPONSE command is used to notify the MC68824 that an updated response frame is to be sent out at a later time when requested by another station. The SET RESPONSE command performs a function equivalent to L_REPLY_UPDATE defined in IEEE 802.2. This command can only be issued when the MC68824 is in the EPA mode.

MODEM CONTROL

Two commands allow the TBC to provide management services to the physical layer of the node.

PHYSICAL Command

The PHYSICAL command is used by the host processor to control the physical layer. This command allows the TBC to either pass commands or send serial data to the physical layer while in station management. Status or data is returned in the last word in the command return area.

END PHYSICAL Command

The END PHYSICAL command removes the TBC from the station management mode. The TBC negates $\overline{\text{SMREQ}}$ and waits for the modem to negate $\overline{\text{SMIND}}$ before setting the command confirmation bit.

TRANSMISSION OF A FRAME

Data frames are transmitted from one of four transmission priority queues. The host processor passes the pointer from the start of the queue to be transmitted to the TBC using the START command. Upon reception of the token by the station, the TBC checks the transmission queues for frames to be sent. If frames are present in one or more of the queues, the TBC will send frames based on their priorities until its allotted transmission time expires. At the end of the frame transmission, the TBC writes into the frame descriptor the status of the frame. The TBC may then generate an interrupt request according to the frame type (non-RWR, RWR, response), interrupt status, and the interrupt mask. The host processor services the interrupt and checks for the status of the frame, (i.e., if transmission was successful). The TBC can transmit frames with lengths of up to 64K bytes. The TBC does not check if the frame is longer than 8K bytes. (The IEEE standard specifies frame lengths of up to 8K bytes.) The TBC does not check if the frame control, destination address, and source address are correct but takes them from the frame descriptor as they are. This means that the host must be sure to write them correctly.

8

RECEPTION OF A FRAME

If the incoming frame's destination address matches the individual station's address, the individual station's group address, or the broadcast address, then the TBC will accept the frame. The TBC can accept frames with undefined frame control field and data frames, can treat control frames as data frames, and can write the CRC of a received frame into the data buffer as defined by the SET MODE commands. The CRC is always calculated and compared with the CRC of the frame. When a frame is accepted, the frame is placed into the appropriate RX priority queue in memory, and its frame descriptor is linked to the last frame descriptor in the queue. If an error occurred on frame reception, the RX status error mask (set by the user initialization) in the TBC private area determines whether to accept or reject the frame. The TBC may generate interrupts upon detecting error conditions. A normal interrupt may also be generated according to the frame's type (RWR or request with no response), the interrupt status, and the interrupt mask.

# LLC TYPE 3 PROTOCOL IMPLEMENTATION

While running in the EPA mode, the MC68824 provides the user with the IEEE 802.2 acknowledged connectionless service primitives described in Table 6. These services provide the means at the data link level to exchange link service data units point to point, which have been acknowledged at the LLC sublayer without establishing a data link connection. Upon receiving an RWR frame, the MC68824, if in the EPA mode, will first check if data is requested in the response. If data is not requested, the MC68824 sends an ACK as a response to acknowledge the RWR frame's reception. If data is requested in the response, then the MC68824 checks for a response associated with the specific DSAP of the request. If the LSAP is active and the response is ready, the response is sent back to the requester with the appropriate status; otherwise, an NACK is sent.

8

Table 6. LLC Type 3 Primitives Provided by the MC68824

Acknowledged Connectionless Data Unit Transmission Service	
Primitive	**Description**
L_DATA_ACK.request	Used to send a data unit with acknowledgement to another node
L_DATA_ACK.indication	Used to indicate the reception of a non-null, non-duplicate LSDU from a remote data link node
L_DATA_ACK_STATUS.indication	Used to indicate whether the previous LSDU transmission request was successful

Acknowledged Connectionless Data Unit Exchange Service	
Primitive	**Description**
L_REPLY.request	Used to request an acknowledged connectionless data unit exchange
L_REPLY.indication	Used to indicate reception of an acknowledged connectionless data frame
L_REPLY_STATUS.indication	Used to confirm acknowledged connectionless data frames

Reply Data Unit Preparation	
Primitive	**Description**
L_REPLY_UPDATE.request	Used to indicate the need to update a response
L_REPLY_UPDATE_STATUS.indication	Used to confirm that a response was updated

8

SIGNAL SUMMARY

For a detailed description of the MC68824 signals, refer to MC68824 UM/AD, *MC68824 Token Bus Controller User's Manual*. Figure 7 illustrates the signals by their functional groups, and Table 7 gives a signal summary.
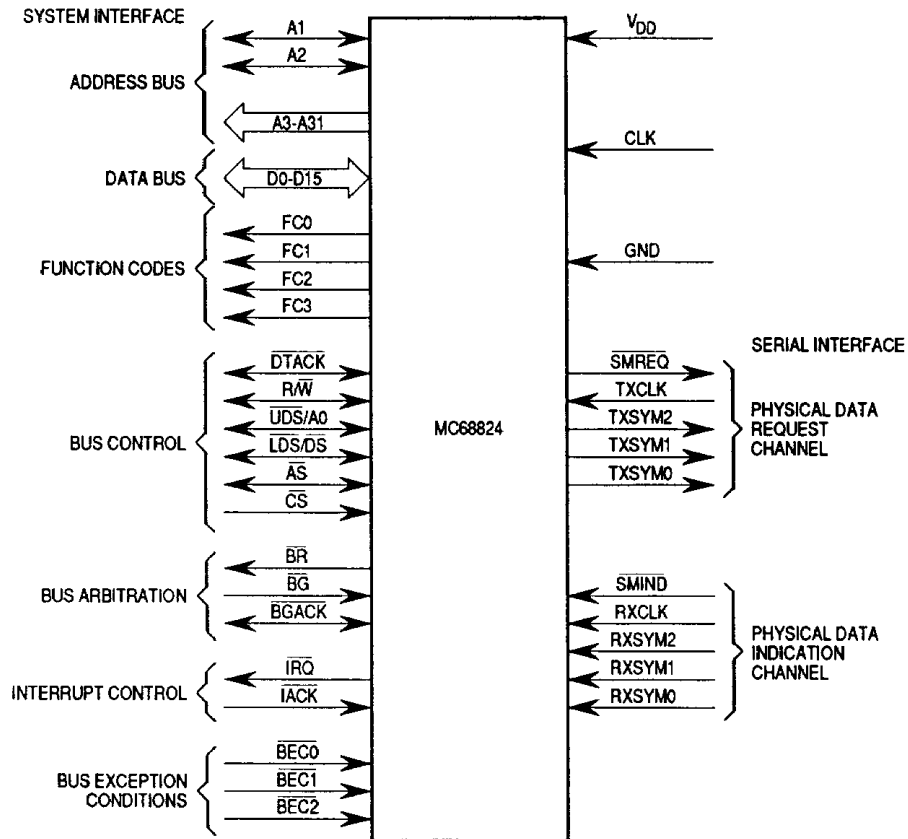
Figure 7. Functional Signal Groups

8

Table 7. Signal Summary

Signal Name	Menemonic	Input/Output	Active State	Driver Type
Address Bus	A1–A2	Input/Output		Three State
Address Bus	A3–A31	Output		Three State
Data Bus	D0–D15	Input/Output		Three State
Function Codes	FC0–FC3	Output		Three State
Bus Exception Codes	$\overline{BEC0}$–$\overline{BEC2}$	Input	Low	
Upper Data Strobe	$\overline{UDS}$/A0	Input/Output	Low/High	Three State[1]
Lower Data Strobe	$\overline{LDS}$/$\overline{DS}$	Input/Output	Low/Low	Three State[1]
Address Strobe	$\overline{AS}$	Input/Output	Low	Three State[1]
Read/Write	R/$\overline{W}$	Input/Output	High/Low	Three State[1]
Chip Select	$\overline{CS}$	Input	Low	
Data Transfer Acknowledge	$\overline{DTACK}$	Input/Output	Low	Three State[1]
Bus Request	$\overline{BR}$	Output	Low	Open Drain[2]
Bus Grant	$\overline{BG}$	Input	Low	
Bus Grant Acknowledge	$\overline{BGACK}$	Input/Output	Low	Three State[1]
Receive Clock	RXCLK	Input		
Indication Channel	$\overline{SMIND}$	Input	Low	
Indication Channel	RXSYM0	Input		
Indication Channel	RXSYM1	Input		
Indication Channel	RXSYM2	Input		
Transmit Clock	TXCLK	Input		
Request Channel	$\overline{SMREQ}$	Input	Low	
Request Channel	TXSYM0	Output		
Request Channel	TXSYM1	Output		
Request Channel	TXSYM2	Output		
Interrupt Request	$\overline{IRQ}$	Output	Low	Open Drain[2]
Interrupt Acknowledge	$\overline{IACK}$	Input	Low	
Clock	CLK	Input		

NOTES:
1. These signals require a pullup resistor to maintain a high voltage when in the high-impedance or negated state. However, when these signals go to the high-impedance or negated state they will first drive the pin high momentarily to reduce the signal rise time.
2. These signals are wire-ORed and require a pullup resistor to maintain a high voltage when not driven.

8

ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications and associated timing information for the MC68824. See Figure 7 for a diagram of the MC68824 signals.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to $+7.0$	V
Input Voltage	V_{in}	-0.3 to $+7.0$	V
Operating Temperature MC68824 MC68824I	T_A	0 to 70 0 to 85	°C
Storage Temperature	T_{stg}	-55 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance for PGA	θ_{JA}		°C/W
Thermal Resistance PGA PLCC		33 TBD	

$T_J = T_A + (P_D \cdot \theta_{JA})$
$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$
where:

      $P_{I/O}$ is the lower dissipation on pins (user determined) which can be neglected in most cases.

For $T_A = 70°C$ and $P_D = 0.55$ W @ 12.5 MHz $T_J = 88°C$

8

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \tag{1}$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins, Watts — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

The following is an approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected):

$$P_D = K \div (T_J + 273°C) \tag{2}$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D{}^2 \tag{3}$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

8

DC ELECTRICAL CHARACTERISTICS

(All specifications are valid under the following conditions: $V_{DD} = 4.75$ V to 5.25 V, $V_{SS} = 0$ V, $T_A = T_L$ to T_H, and output load = 130 pF.)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage (Except System Clock)	V_{IH}	2.0	V_{DD}	V
Input Low Voltge (Except System Clock)	V_{IL}	$V_{SS} - 0.3$	0.8	V
Input High Voltage (System Clock)	V_{CIH}	2.4	V_{DD}	V
Input Low Voltage (System Clock)	V_{CIL}	$V_{SS} - 0.3$	0.5	V
Input Leakage Current @ 5.25 V	I_{in}	—	20	μA
Input Capacitance ($V_{in} = 0$ V, $T_A = 25°C$, F = 1 MHz)	C_{in}	—	13	pF
Three-State Leakage Current @ 2.4/0.5 V	I_{TSI}	—	20	μA
Open-Drain Leakage Current @ 2.4 V	I_{OD}	—	20	μA
Output High Voltage ($I_{OH} = 1$ mA) SMREQ, TXSYM2, TXSYM1, TXSYM0 ($I_{OH} = 400$ μA) All Others	V_{OH}	2.5 2.4	— —	V
Output Low Voltage ($I_{OL} = 8.0$ mA) SMREQ, TXSYM2, TXSYM1, TXSYM0 ($I_{OL} = 3.2$ mA) A1–A31, FC0–FC3, and UDS/A0 as A0 ($I_{OL} = 5.3$ mA) D0–D15, AS, LDS/DS, UDS/A0 as UDS, DTACK, BGACK, R/W ($I_{OL} = 8.9$ mA) IRQ, BR	V_{OL}	— — — —	0.5 0.5 0.5 0.5	V
Power Dissipation @ 10 MHz, 0°C @ 12.5 MHz, 0°C @ 16.67 MHz, 0°C	P_D	—	0.50 0.55 0.70	W

8

AC ELECTRICAL CHARACTERISTICS

(All specifications are valid under the following conditions: $V_{DD} = 4.75$ V to 5.25 V, $V_{SS} = 0$ V, $T_A = T_L$ to T_H, output load = 130 pF, and output current as specified in **DC ELECTRICAL CHARACTERISTICS**.)

Num.	Characteristic	10 MHz		12.5 MHz		16.67 MHz		Unit
		Min	Max	Min	Max	Min	Max	
1	Asynchronous Input Setup Time	20	—	20	—	10	—	ns
2	UDS, LDS Inactive to CS, IACK Inactive	—	100	—	80	—	60	ns
3	CLK Low (on Which UDS or LDS and CS or IACK Are Recognized) to Data-Out Valid (see Note 5)	—	1.2 + 150	—	1.2 + 120	—	1.2 + 90	Clk. Per. ns
4	CS or IACK High to Data-Out High Impedance	—	60	—	50	—	35	ns
5	LDS/DS High to Data-Out Hold Time (see Note 6)	0	—	0	—	0	—	ns
6	IACK or CS Low to DTACK High (Driving Three-State DTACK High)	—	80	—	70	—	60	ns
7	CLK Low (on Which UDS or LDS and CS or IACK Are Recognized) to DTACK Low (see Note 5)	—	2 + 90	—	2 + 80	—	2 + 60	Clk. Per. ns
8	CLK Low to DTACK Low	—	90	—	80	—	50	ns
9	Data-Out Valid to DTACK Low	20	—	20	—	20	—	ns
10	DTACK Low to UDS, LDS, CS, IACK High (Earliest)	100	—	80	—	60	—	ns
11	CS or IACK or Data Strobes (the Earliest) High to DTACK High (see Note 7)	—	60	—	50	—	40	ns
12	DTACK High to DTACK High Impedance (at End of Bus Cycle)	—	50	—	50	—	40	ns
13	UDS, LDS Inactive Time	1	—	1	—	1	—	Clk. Per.
14	CS, IACK Inactive Time	0	—	0	—	0	—	ns
15	A1–A2 Valid to UDS, LDS, CS (the Latest One) Low (Write)	30	—	20	—	20	—	ns
16	DTACK Low to Data and A1–A2 Hold Time	100	—	80	—	60	—	ns
17	UDS or LDS, CS or IACK (the Latest One) Low to Data-In Valid	—	80	—	70	—	60	ns
18	R/W Valid to UDS, or LDS, CS or IACK (the Latest One) Low	20	—	20	—	10	—	ns
19	UDS, LDS High to R/W High	0	—	0	—	0	—	ns
20	CLK High to IRQ Low	—	100	—	80	—	60	ns
21	Reserved							
22	Reserved							
23	CLK High to BR Low	—	60	—	55	—	40	ns
24	CLK High to BR High Impedance	—	55	—	50	—	40	ns
25	BGACK Low to BR High Impedance	20	—	20	—	10	—	ns
26	BG Active/Inactive to CLK Low Setup Time	20	—	20	—	10	—	ns
27	CLK Low to BGACK Low	—	60	—	55	—	40	ns
28	CLK High to BGACK High Impedance	—	45	—	40	—	30	ns
29	AS and BGACK High (the Latest One), to BGACK Low (When BG Is Previously Asserted)	2 + 20	3 + 80	2 + 20	3 + 70	2 + 10	3 + 50	Clk. Per. ns

— CONTINUED —

AC ELECTRICAL CHARACTERISTICS (Continued)

Num.	Characteristic	10 MHz		12.5 MHz		16.67 MHz		Unit
		Min	Max	Min	Max	Min	Max	
30	BG Low to BGACK Low (No Other Bus Master)	2 +20	3 +80	2 +20	3 +70	2 +10	3 +50	Clk. Per. ns
31	BR High Impedance to BG High	0	—	0	—	0	—	ns
32	Clock on Which BGACK Low to Clock on Which AS Low	1.5	1.5	1.5	1.5	1.5	1.5	Clk. Per.
33	Clock Low to BGACK High	—	55	—	50	—	40	ns
34	CLK on Which BR Low to CLK on Which BGACK Low (Assuming BG Is Active and BGACK and AS Are Inactive for at Least 2 CLK Periods)	1.5	1.5	1.5	1.5	1.5	1.5	Clk. Per.
35	CLK on Which AS is High to CLK on Which BGACK is High	—	1	—	1	—	1	Clk. Per.
36	CLK High to Address Valid	—	100	—	80	—	60	ns
37	CLK High to Address/FC High Impedance	—	70	—	60	—	50	ns
38	CLK High to FC Valid	—	60	—	55	—	50	ns
39	Address Valid to AS Valid	20	—	15	—	10	—	ns
40	CLK High to AS, UDS, LDS Low	—	50	—	40	—	30	ns
41	CLK to AS, UDS, LDS High	—	55	—	50	—	45	ns
42	AS High to Address/FC Invalid	20	—	10	—	10	—	ns
43	CLK High to AS, UDS, LDS High Impedance	—	70	—	60	—	45	ns
44	CLK to R/W High (see Note 4)	—	55	—	50	—	45	ns
45	CLK Low to R/W High Impedance	—	70	—	60	—	45	ns
46	UDS, LDS High to Data-In Invalid	0	—	0	—	0	—	ns
47	AS, UDS, LDS High to DTACK High (Earliest of AS, UDS, or LDS)	0	100	0	90	0	60	ns
48	Data-In to CLK Low Setup Time Required When DTACK Satisfies (1) (see Note 1)	10	—	10	—	5	—	ns
49	DTACK Low to Data-In Valid Required When DTACK Does Not Satisfy (1) (see Note 2)	—	65	—	50	—	40	ns
50	CLK High to R/W Low	—	60	—	55	—	40	ns
51	AS Low to Data-Out Valid (Write)	—	90	—	80	—	60	ns
52	CLK Low to Data-Out Valid	—	55	—	55	—	40	ns
53	Data-Out Valid to UDS, LDS Low	20	—	15	—	10	—	ns
54	UDS, LDS High to Data-Out Invalid	20	—	15	—	10	—	ns
55	CLK High to Data-Out Hold Time	0	100	0	80	0	60	ns
56	No Exception to BR (DTACK Active)	1.5 +20	2.5 +80	1.5 +20	2.5 +70	1.5 +10	2.5 +50	Clk. Per. ns
57	DTACK Low to Asynchronous Exception Active Required When DTACK Does Not Satisfy (1) (see Note 2)	—	55	—	35	—	30	ns
58	Exception Active to CLK Low Setup Time Synchronous Input ("Late Exception") Required When DTACK Satisfies (1) (see Note 1)	45	—	45	—	20	—	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Num.	Characteristic	10 MHz		12.5 MHz		16.67 MHz		Unit
		Min	Max	Min	Max	Min	Max	
59	Exception Active to CLK Low Setup Time Asynchronous Input (Required When DTACK Is Absent) (see Note 3)	20	—	20	—	10	—	ns
60	AS, UDS, LDS High to Exception Inactive	0	—	0	—	0	—	ns
61	Exception Inactive to CLK Low Setup Time (for Identification of No Exception)	20	—	20	—	10	—	ns
62	No Exception to BR (DTACK Inactive)	2.5 +20	3.5 +80	2.5 +20	3.5 +70	2.5 +10	3.5 +50	Clk. Per. ns
63	RESET (on BEC0–BEC2) Width	10	—	10	—	10	—	Clk. Per.
64	CLK Frequency	4	10	4	12.5	8	16.67	MHz
65	CLK Period	100	250	80	250	60	125	ns
66	CLK Width High (see Note 8)	45	125	35	125	25	62.5	ns
67	CLK Rise/Fall Time (see Note 8)	—	10	—	5	—	5	ns
68	CLK Width Low (see Note 8)	45	125	35	125	25	62.5	ns
69*	RXCLK, TXCLK Frequency	1	10	1	12.5	5	16.67	MHz
70	RXD Signals Setup Time	35	—	35	—	25	—	ns
71	RXD Signals Hold Time	5	—	5	—	5	—	ns
72	RXCLK, TXCLK Rise/Fall Time	—	10	—	10	—	5	ns
73*	RXCLK, TXCLK Width Low	40	525	40	525	25	100	ns
74*	RXCLK, TXCLK Width High	40	525	40	525	25	100	ns
75*	RXCLK, TXCLK Period	95	1050	80	1050	60	200	ns
76	TXCLK High to TXD Signals Output Delay	5	55	5	55	5	45	ns

*Parts with an S suffix have the following characteristics:

69	RXCLK, TXCLK Frequency	.01	10	.01	12.5	—	—	MHz
73	RXCLK, TXCLK Width Low	40	50,000	40	50,000	—	—	ns
74	RXCLK, TXCLK Width High	40	50,000	40	50,000	—	—	ns
75	RXCLK, TXCLK Period	95	100,000	80	100,000	—	—	ns

8

AC ELECTRICAL CHARACTERISTICS (Concluded)

NOTES:

1. High and low outputs are measured at 2.0 V minimum and 0.8 V maximum, respectively, except $\overline{SMREQ}$ and TXSYM0–TXSYM2, which are measured from 2.5 V and 0.5 V. High and low inputs are driven to 2.4 V and 0.5 V, respectively, for AC test purposes. However, input specifications are still measured from 2.0 V to 0.8 V.
2. If $\overline{DTACK}$ satisfies the asynchronous setup time (1), then (48) is required for the data-in setup time and (58) for the synchronous exception setup time. Erroneous behavior may occur if (58) is not satisfied.
3. If $\overline{DTACK}$ does not satisfy (1), then (49) is required for data-in and (57) for the exception. Erroneous behavior may occur if (57) is not satisfied.
4. Active exception when $\overline{DTACK}$ is absent must satisfy the asynchronous setup time (59).
5. R/W rises on the end of a write cycle (i.e., on the phase following S7). If the TBC relinquishes the bus, then R/W is three-stated one phase later. When the TBC takes the bus, R/W is three-stated until S1 and rises on that phase.
6. Data (3) and $\overline{DTACK}$ (7) will be timed from the earliest clock on which $\overline{CS}$ and either data strobe are recognized during an MPU cycle. Data (3) and $\overline{DTACK}$ will be timed from the earliest clock on which $\overline{IACK}$ and either data strobe are recognized during an $\overline{IACK}$ cycle.
7. If $\overline{CS}$ or $\overline{IACK}$ is negated before $\overline{UDS}/\overline{LDS}$, the data bus will be three-stated (4), possibly before $\overline{UDS}\cdot\overline{LDS}$ negation.
8. If an 8-bit bus is used, only $\overline{LDS}$ need be considered. If a 16-bit bus is used, both $\overline{UDS}$ and $\overline{LDS}$ must negate to apply to this specification.
9. The clock signal used during test has 5 ns of rise time and 5 ns of fall time. For system implementations that have less clock rise and fall time, the clock pulse minimum should be commensurately wider such that:
   1. System $(TCL + (TCR + TCF) \div 2) \geq (minimum\ TCYC) \div 2$
   2. System $(TCH + (TCR + TCF) \div 2) \geq (minimum\ TCYC) \div 2$
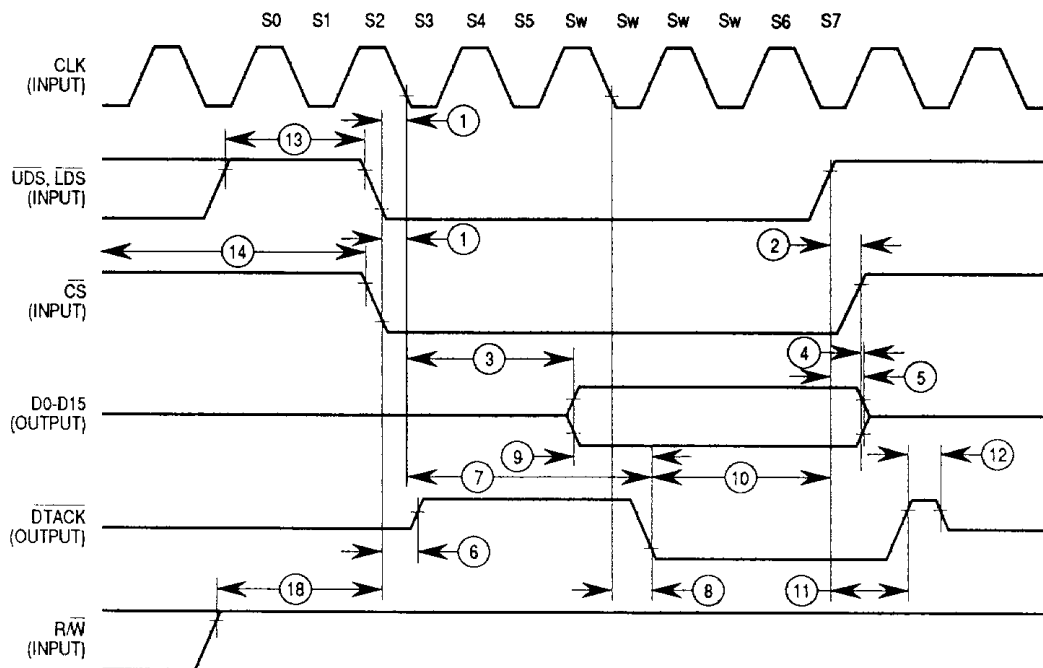10. For performance reasons, a frequency ratio of systems clock to serial clock must be greater than 1:1.
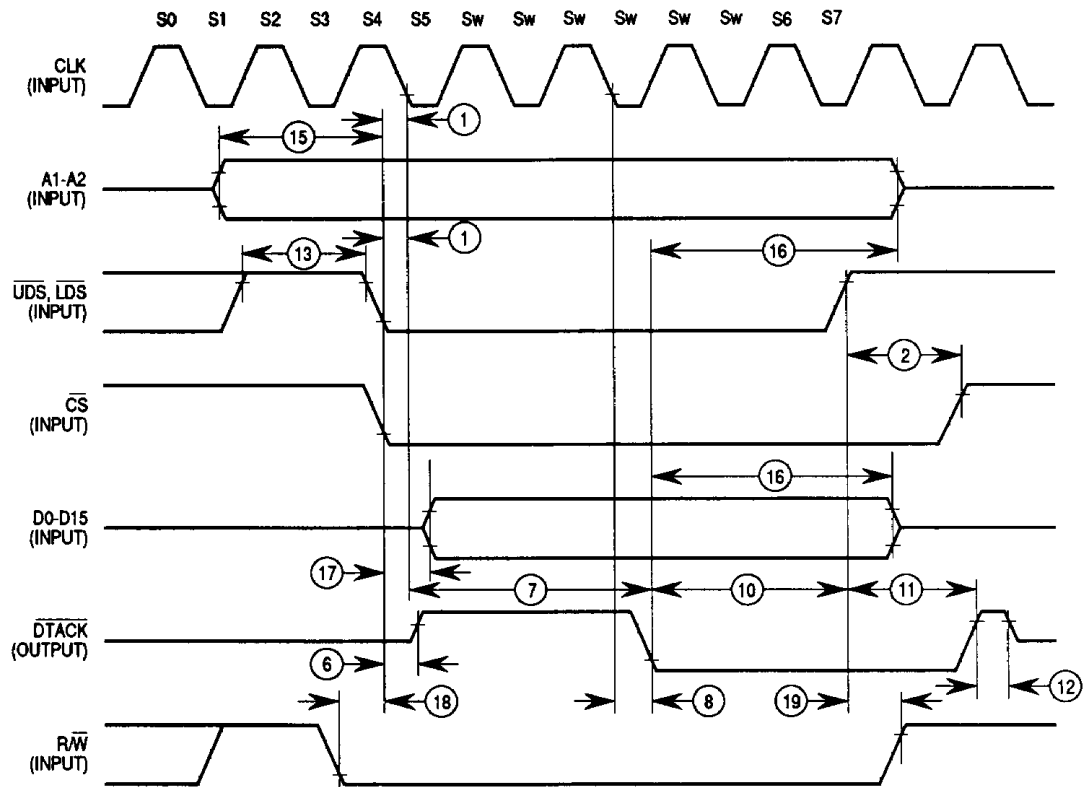

Figure 8. Host Processor Read Cycle
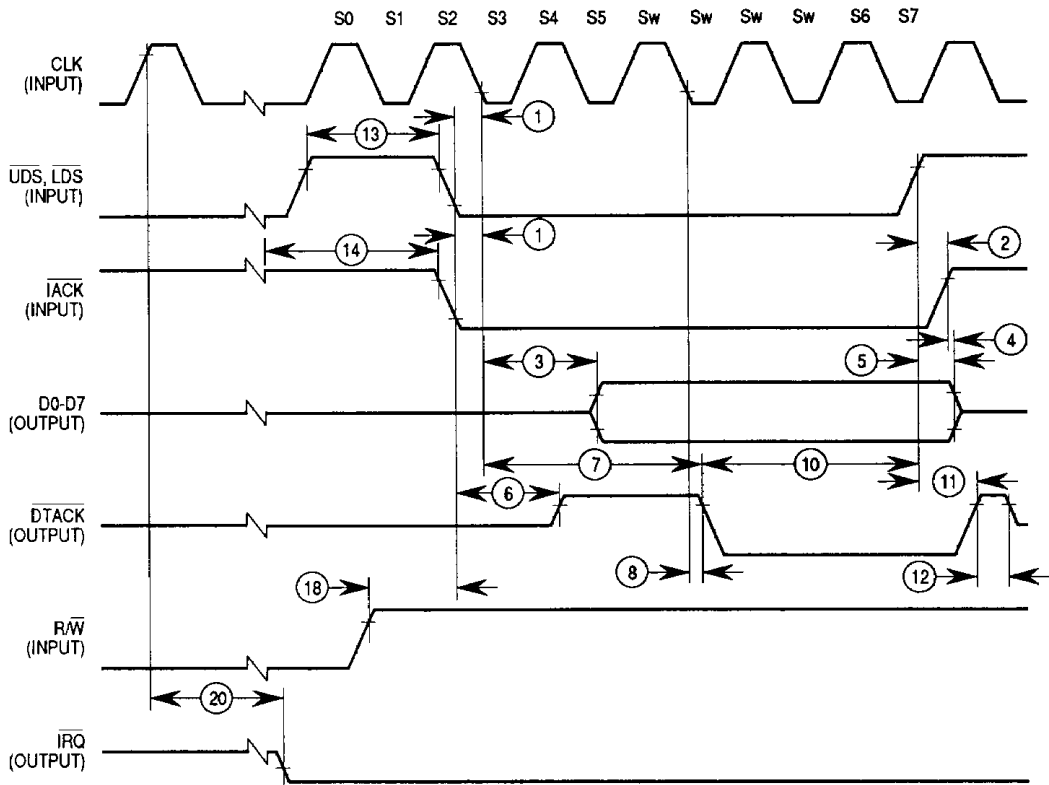
Figure 9. Host Processor Write Cycle

Figure 10. Interrupt Acknowledge Cycle

8

Figure 11. Bus Arbitration

M68000 FAMILY REFERENCE MANUAL MOTOROLA

8

Figure 12. Read Cycle and Slow Read Cycle
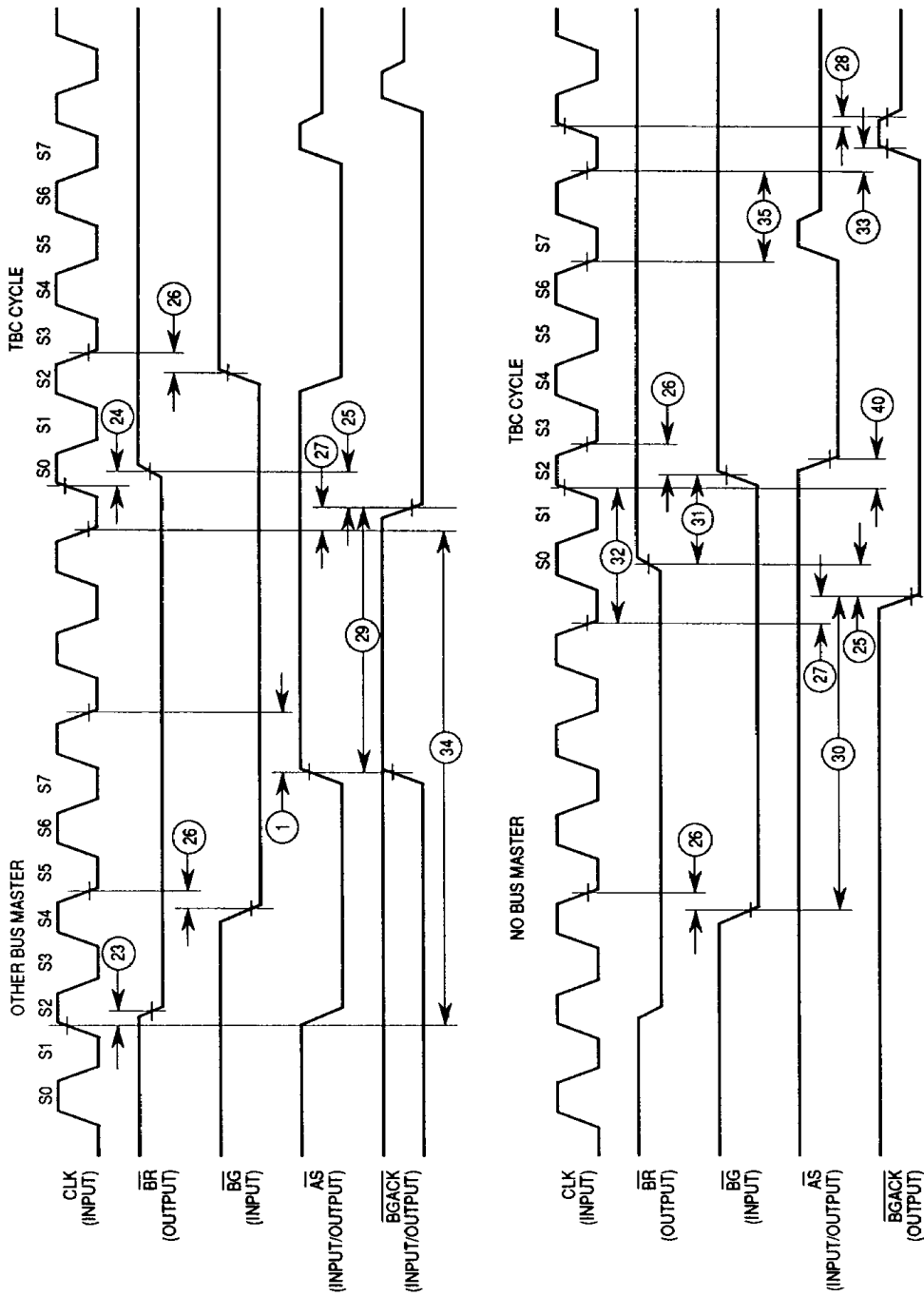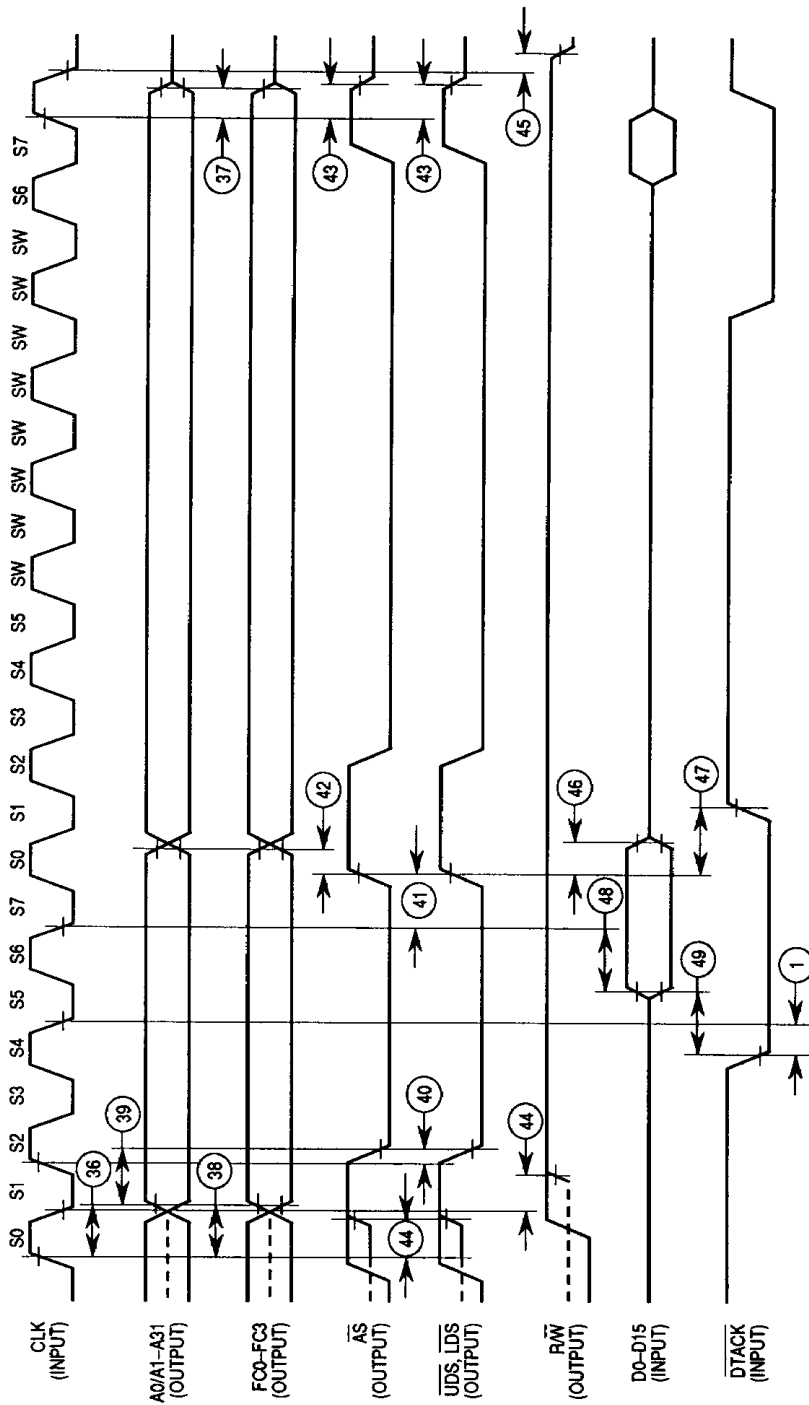
NOTE: The solid lines assume that the communication controller was bus master on the last cycle. The dotted lines assume that there was a different bus master.

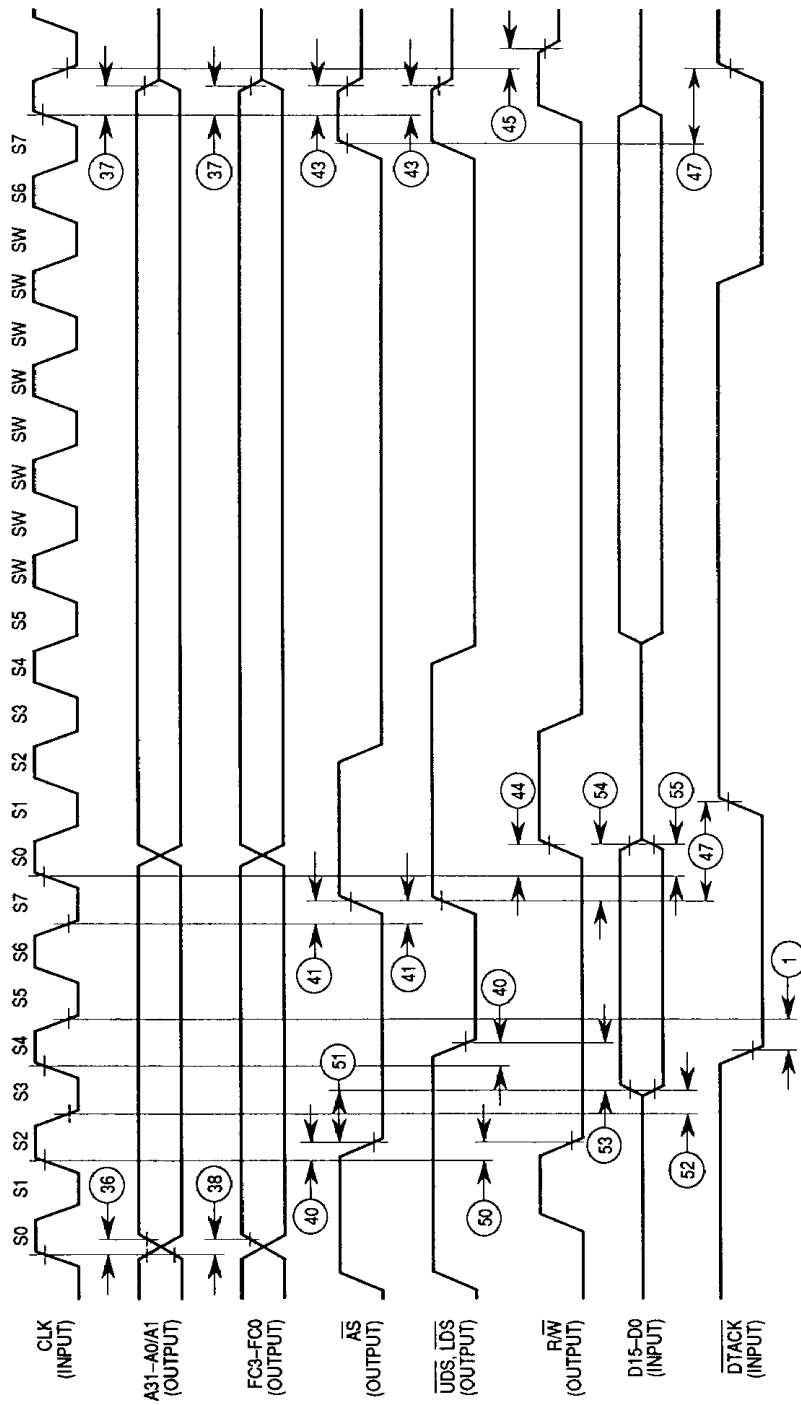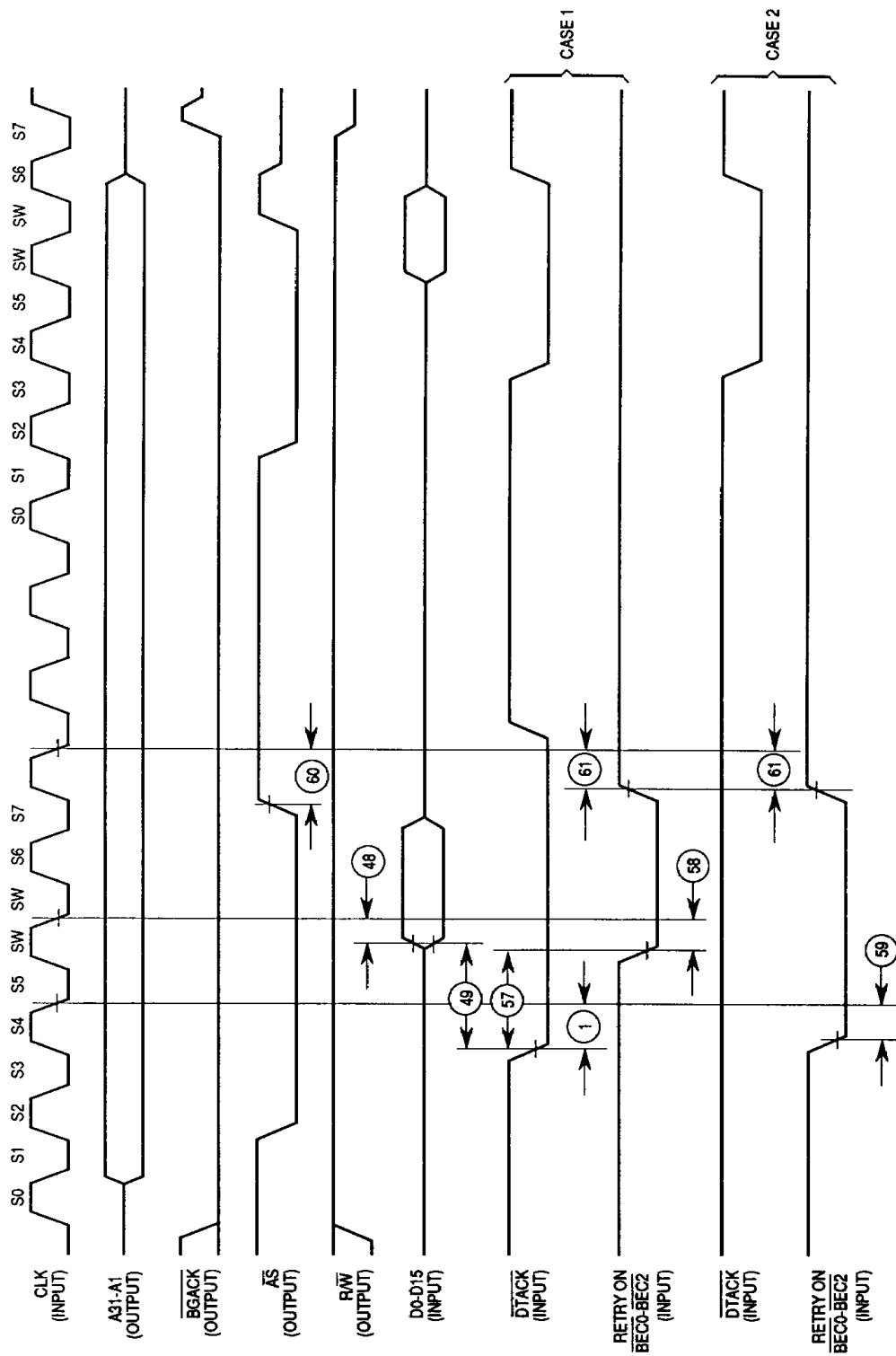Figure 13. Write Cycle and Slow Write Cycle

M68000 FAMILY REFERENCE MANUAL MOTOROLA

Figure 14. Read Cycle with RETRY

CASE 1: If $\overline{DTACK}$ satisfies (1), then (48) and (58) are required; if $\overline{DTACK}$ is active but does not satisfy (1), then (49) and (57) are required.
CASE 2: If $\overline{DTACK}$ is not active, then (59) is required for the exception active setup time. Parameter (61) is always required for the exception inactive setup time.
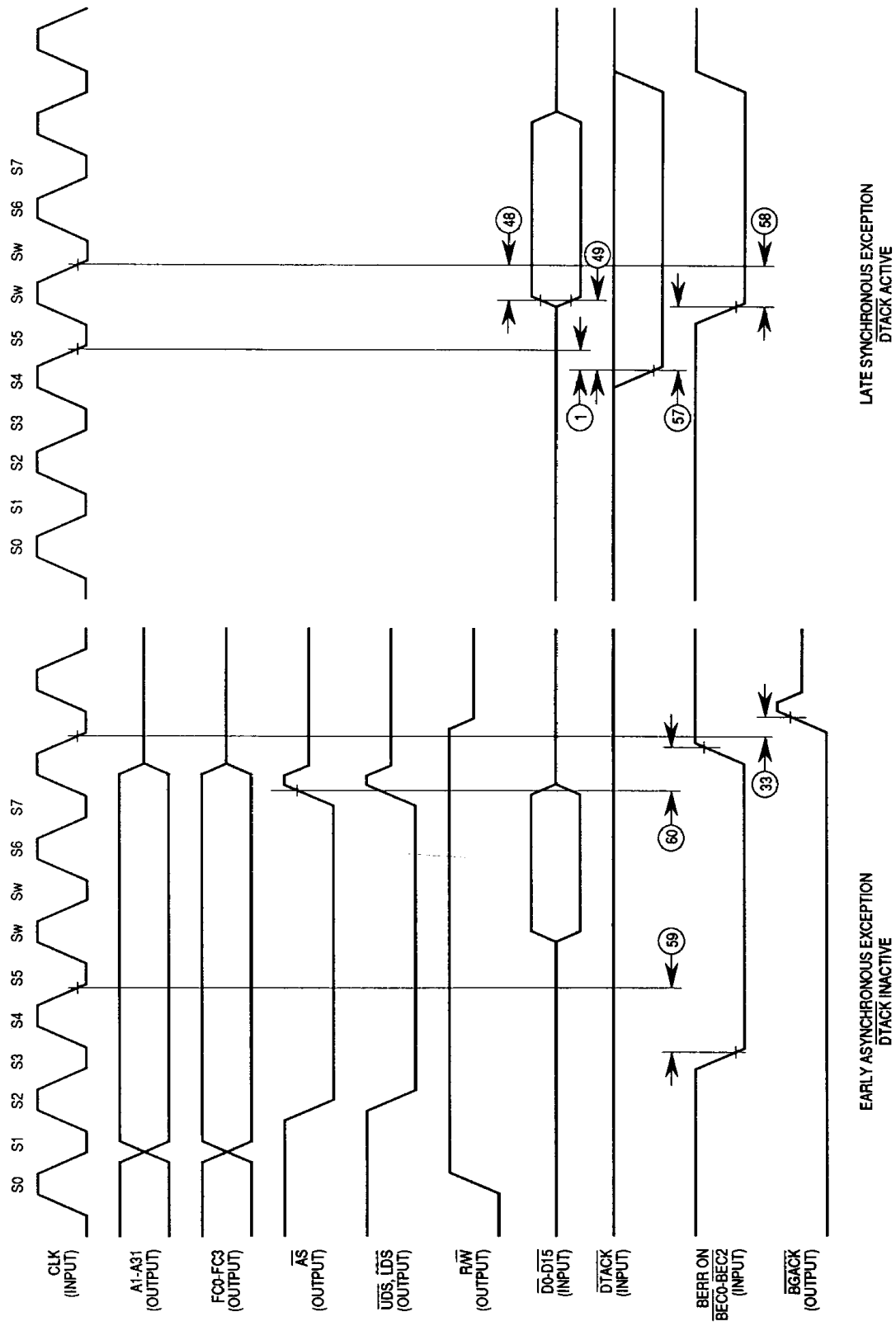
Figure 15. Read Cycle with Bus Error
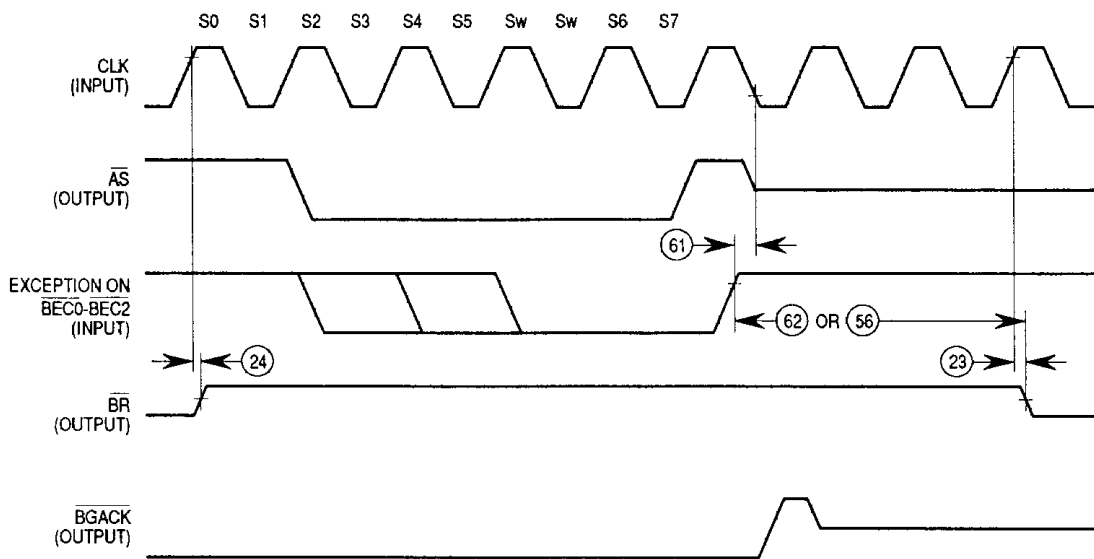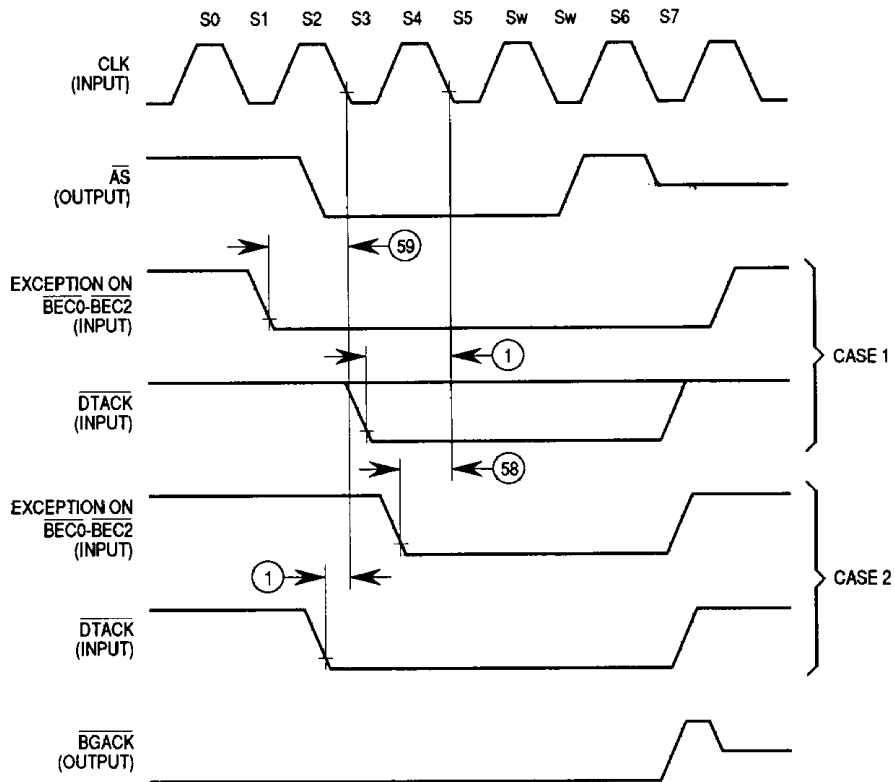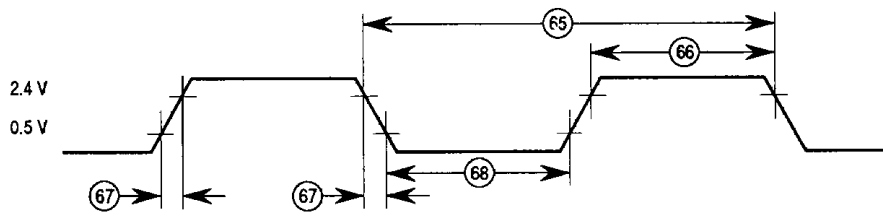
NOTE: The above occurs when the TBC requires the bus cycle after a previous exception.

Figure 16. BR After Previous Exception

8

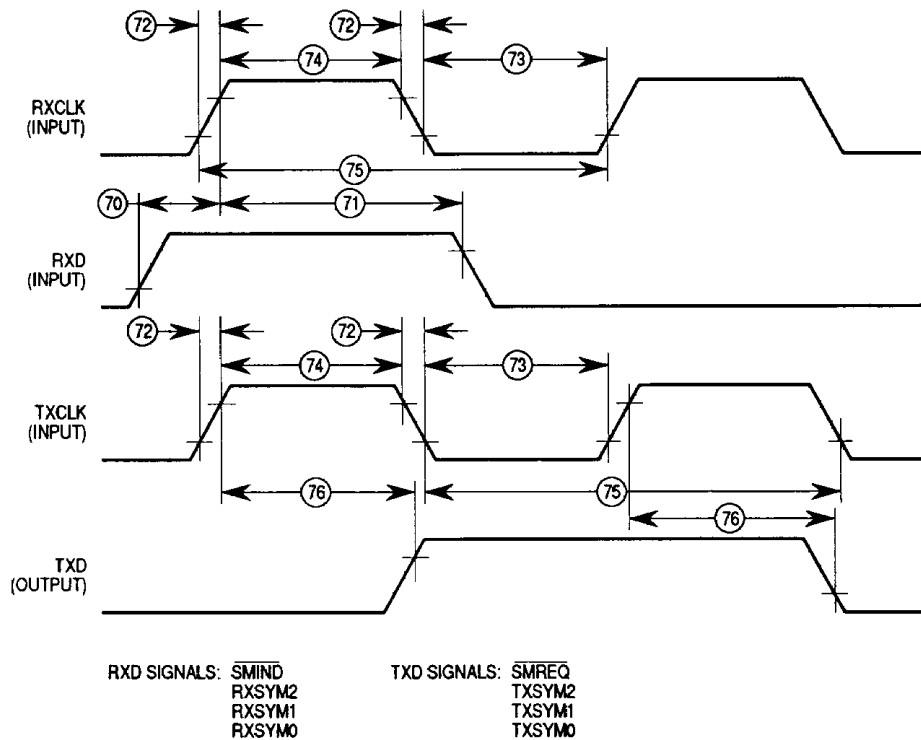NOTE: Two alternatives of DTACK and exception. Case 1 has DTACK occur after exception and case 2 has exception occur after DTACK.

Figure 17. Short Exception Cycle

Figure 18. Clock (CLK)

RXD SIGNALS: SMIND   TXD SIGNALS: SMREQ
            RXSYM2   TXSYM2
            RXSYM1   TXSYM1
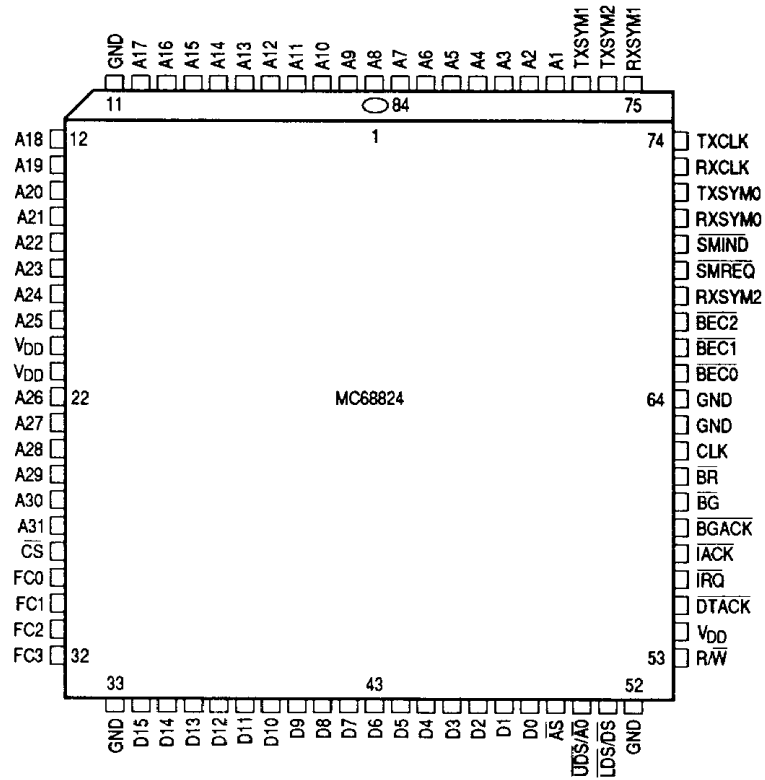   RXSYM0   TXSYM0

NOTE: If a serial speed of 10 Mbps is required, then the MC68824 system clock must run at 12.5 MHz or
      16.67 MHz. If a serial speed greater than 10 Mbps is required, then the MC68824 system clock
      must run at 16.67 MHz.

Figure 19. Serial Data (RXD and TXD) and Serial Clocks (RCLK and TCLK)

8

PIN ASSIGNMENTS

84-LEAD PLASTIC LEADED CHIP CARRIER

84-LEAD PIN GRID ARRAY

	1	2	3	4	5	6	7	8	9	10
K	TXSYM0	TXSYM2	TXSYM1	A3	A6	A8	A10	A12	A14	A16
J	SMIND	RXCLK	RXSYM1	A2	A5	A9	A13	A15	A17	A19
H	RXSYM2	RXSYM0	TXCLK	A1	A4	A7	A11	GND	A18	A20
G	BEC1	BEC2	SMREQ					A21	A22	A23
F	CLK	BEC0	V$_{SS}$		MC68824			V$_{DD}$	A24	A25
E	BR	BG	V$_{SS}$		(BOTTOM VIEW)			A26	A28	A27
D	BGACK	IACK	V$_{DD}$					CS	A31	A29
C	IRQ	DTACK	NOT USED	D0	D6	D9	D12	GND	FC1	A30
B	R/W	NC	UDS/A0	D2	D5	D8	D11	D15	FC3	FC0
A	LDS/DS	AS	D1	D3	D4	D7	D10	D13	D14	FC2

8