

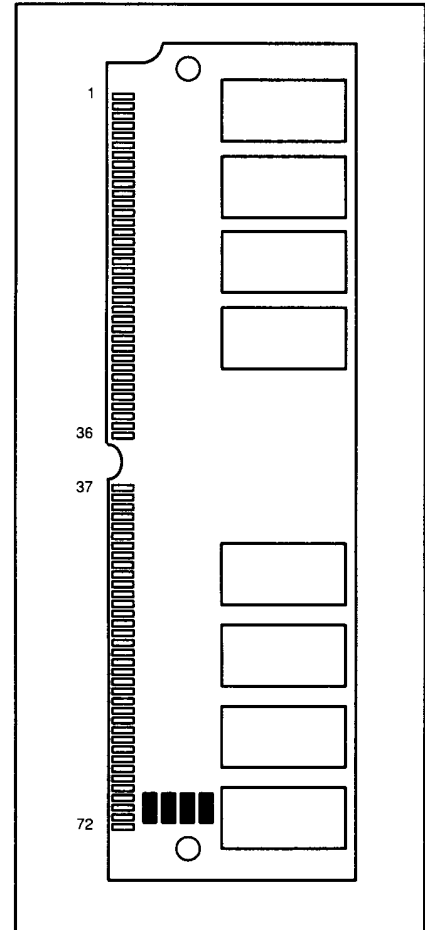
**MOTOROLA**  
**SEMICONDUCTOR**  
**TECHNICAL DATA**

**MCM32200**  
**MCM32L200**

*Advance Information*  
**2M × 32 Bit Dynamic Random  
Access Memory Module**

The MCM32200S is a 64M, dynamic random access memory (DRAM) module organized as 2,097,152 × 32 bits. The module is a 72-lead double sided single-in-line memory module (SIMM) consisting of sixteen MCM514400 DRAMs housed in standard 350-mil-wide SOJ packages mounted on a substrate along with a 0.22 μF (min) decoupling capacitor mounted under each DRAM. The MCM514400 is a CMOS high speed, dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$  Only Refresh
- $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  - MCM32200S = 16 ms (Max)
  - MCM32L200S = 128 ms (Max)
- Consists of Sixteen 1M × 4 DRAMs and Sixteen 0.22 μF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time ( $t_{\text{RAC}}$ ):
  - MCM32200S-80 = 80 ns (Max)
  - MCM32200S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM32200S-80 = 4.71 W (Max)
  - MCM32200S-10 = 4.05 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 176 mW (Max)
  - CMOS Levels = 88 mW (Max, MCM32200S)
  - CMOS Levels = 36 mW (Max, MCM32L200S)



**PIN OUT**

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V <sub>SS</sub>	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V <sub>SS</sub>	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V <sub>CC</sub>	42	$\overline{\text{CAS3}}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{\text{CAS1}}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	$\overline{\text{RAS3}}$	45	$\overline{\text{RAS1}}$	57	DQ12	69	PD3
10	V <sub>CC</sub>	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{\text{W}}$	59	V <sub>CC</sub>	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V <sub>SS</sub>

**PIN NAMES**

- A0-A9 ..... Address Inputs
- DQ0-DQ31 ..... Data Input/Output
- CAS0-CAS3 ... Column Address Strobe
- PD1-PD4 ..... Presence Detect
- RAS0-RAS3 ..... Row Address Strobe
- $\overline{\text{W}}$  ..... Read/Write Input
- V<sub>CC</sub> ..... Power (+ 5 V)
- V<sub>SS</sub> ..... Ground
- NC ..... No Connection

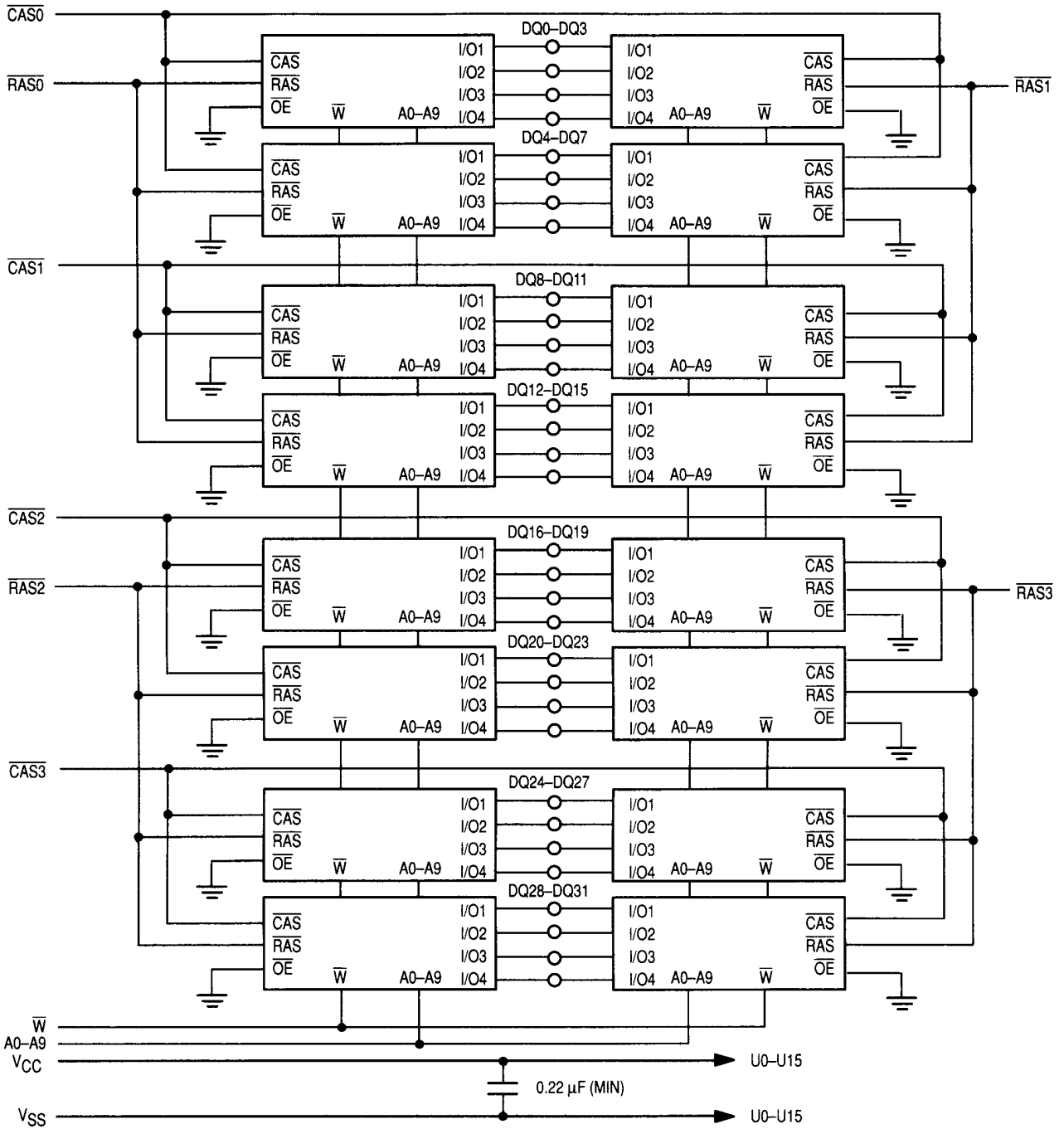
All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



**MOTOROLA**

## BLOCK DIAGRAM



**PRESENCE DETECT PIN OUT**

Pin Name	70 ns	80 ns	100 ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	VSS	NC	VSS
PD4	NC	VSS	VSS

**ABSOLUTE MAXIMUM RATINGS** (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	- 1 to + 7	V
Voltage Relative to $V_{SS}$ (For Any Pin Except $V_{CC}$ )	$V_{in}, V_{out}$	- 1 to + 7	V
Data Output Current per DQ Pin	$I_{out}$	50	mA
Power Dissipation	$P_D$	6.42	W
Operating Temperature Range	$T_A$	0 to + 70	°C
Storage Temperature Range	$T_{stg}$	- 55 to + 125	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**  
( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $T_A = 0\text{ to }70^\circ\text{C}$ , Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.0	5.5	V	1
	$V_{SS}$	0	0	0		
Logic High Voltage, All Inputs	$V_{IH}$	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	$V_{IL}$	- 1.0	—	0.8	V	1

**RECOMMENDED OPERATING CONDITIONS**

Characteristic	Symbol	Min	Max	Unit	Notes
$V_{CC}$ Power Supply Current MCM32200-80, $t_{RC} = 150\text{ ns}$ MCM32200-10, $t_{RC} = 180\text{ ns}$	$I_{CC1}$	—	856 736	mA	2
$V_{CC}$ Power Supply Current (Standby) ( $\overline{RAS} = \overline{CAS} = V_{IH}$ )	$I_{CC2}$	—	32	mA	
$V_{CC}$ Power Supply Current During $\overline{RAS}$ only Refresh Cycles MCM32200-80, $t_{RC} = 150\text{ ns}$ MCM32200-10, $t_{RC} = 180\text{ ns}$	$I_{CC3}$	—	856 736	mA	2
$V_{CC}$ Power Supply Current During Fast Page Mode Cycle MCM32200-80, $t_{RC} = 150\text{ ns}$ MCM32200-10, $t_{RC} = 180\text{ ns}$	$I_{CC4}$	—	576 496	mA	2
$V_{CC}$ Power Supply Current (Standby) ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2\text{ V}$ ) MCM32200 MCM32L200	$I_{CC5}$	—	16 6.4	mA	
$V_{CC}$ Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM32200-80, $t_{RC} = 150\text{ ns}$ MCM32200-10, $t_{RC} = 180\text{ ns}$	$I_{CC6}$	—	856 736	mA	2
Input Leakage Current ( $V_{SS} \leq V_{in} \leq V_{CC}$ )	$I_{lkg(I)}$	- 160	160	$\mu\text{A}$	
Output Leakage Current ( $\overline{CAS}$ at Logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$ )	$I_{lkg(O)}$	- 20	20	$\mu\text{A}$	
Output High Voltage ( $I_{OH} = - 5\text{ mA}$ )	$V_{OH}$	2.4	—	V	
Output Low Voltage ( $I_{OL} = 4.2\text{ mA}$ )	$V_{OL}$	—	0.4	V	

**NOTES:**

1. All voltages referenced to  $V_{SS}$ .
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.

**CAPACITANCE** (f = 1.0 MHz, T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit	Notes
Input Capacitance (A0–A9)	C <sub>I1</sub>	—	90	pF	1
Input Capacitance ( $\bar{W}$ )	C <sub>I2</sub>	—	122	pF	1
Input Capacitance ( $\bar{RAS0}$ – $\bar{RAS2}$ )	C <sub>I3</sub>	—	38	pF	1
Input Capacitance ( $\bar{CAS0}$ – $\bar{CAS3}$ )	C <sub>I4</sub>	—	38	pF	1
I/O Capacitance (DQ0–DQ31)	C <sub>DQ</sub>	—	24	pF	1

**NOTE:**

1. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation:  $C = 1 \Delta t / \Delta V$ .

**AC OPERATING CONDITIONS AND CHARACTERISTICS**  
(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

**READ AND WRITE CYCLES** (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM32200-80		MCM32200-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t <sub>RELREL</sub>	t <sub>RC</sub>	150	—	180	—	ns	5
Page Mode Cycle Time	t <sub>CELCEL</sub>	t <sub>PC</sub>	50	—	60	—	ns	
Access Time from $\bar{RAS}$	t <sub>RELQV</sub>	t <sub>RAC</sub>	—	80	—	100	ns	6, 7
Access Time from $\bar{CAS}$	t <sub>CELQV</sub>	t <sub>CAC</sub>	—	20	—	25	ns	6, 8
Access Time from Column Address	t <sub>AVQV</sub>	t <sub>AA</sub>	—	40	—	50	ns	6, 9
Access Time from Precharge $\bar{CAS}$	t <sub>CEHQV</sub>	t <sub>CPA</sub>	—	45	—	55	ns	6
$\bar{CAS}$ to Output in Low-Z	t <sub>CELQX</sub>	t <sub>CLZ</sub>	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t <sub>CEHQZ</sub>	t <sub>OFF</sub>	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t <sub>T</sub>	t <sub>T</sub>	3	50	3	50	ns	
$\bar{RAS}$ Precharge Time	t <sub>REHREL</sub>	t <sub>RP</sub>	60	—	70	—	ns	
$\bar{RAS}$ Pulse Width	t <sub>RELREH</sub>	t <sub>RAS</sub>	80	10,000	100	10,000	ns	
$\bar{RAS}$ Pulse Width (Fast Page Mode)	t <sub>RELREH</sub>	t <sub>RASP</sub>	80	100,000	100	100,000	ns	
$\bar{RAS}$ Hold Time	t <sub>CELREH</sub>	t <sub>RSH</sub>	25	—	25	—	ns	
$\bar{CAS}$ Hold Time	t <sub>RELCEH</sub>	t <sub>CSH</sub>	80	—	100	—	ns	
$\bar{CAS}$ Pulse Width	t <sub>CELCEH</sub>	t <sub>CAS</sub>	20	10,000	25	10,000	ns	
$\bar{RAS}$ to $\bar{CAS}$ Delay Time	t <sub>RELCEL</sub>	t <sub>RCD</sub>	20	60	25	75	ns	11
$\bar{RAS}$ to Column Address Delay Time	t <sub>RELAV</sub>	t <sub>RAD</sub>	15	40	20	50	ns	12

(continued)

**NOTES:**

1. V<sub>IH</sub> min and V<sub>IL</sub> max are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
2. An initial pause of 200 μs is required after power-up followed by 8  $\bar{RAS}$  cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
4. AC measurements t<sub>T</sub> = 5.0 ns.
5. The specifications for t<sub>RC</sub> (min) and t<sub>RWC</sub> (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (–200 μA, +4 mA) loads and 100 pF with the data output trip points set at V<sub>OH</sub> = 2.0 V and V<sub>OL</sub> = 0.8 V.
7. Assumes that t<sub>RCD</sub> ≤ t<sub>RCD</sub> (max).
8. Assumes that t<sub>RCD</sub> ≥ t<sub>RCD</sub> (max).
9. Assumes that t<sub>RAD</sub> ≥ t<sub>RAD</sub> (max).
10. t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t<sub>RCD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
12. Operation within the t<sub>RAD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RAD</sub> (max) is specified as a reference point only; if t<sub>RAD</sub> is greater than the specified t<sub>RAD</sub> (max), then access time is controlled exclusively by t<sub>AA</sub>.

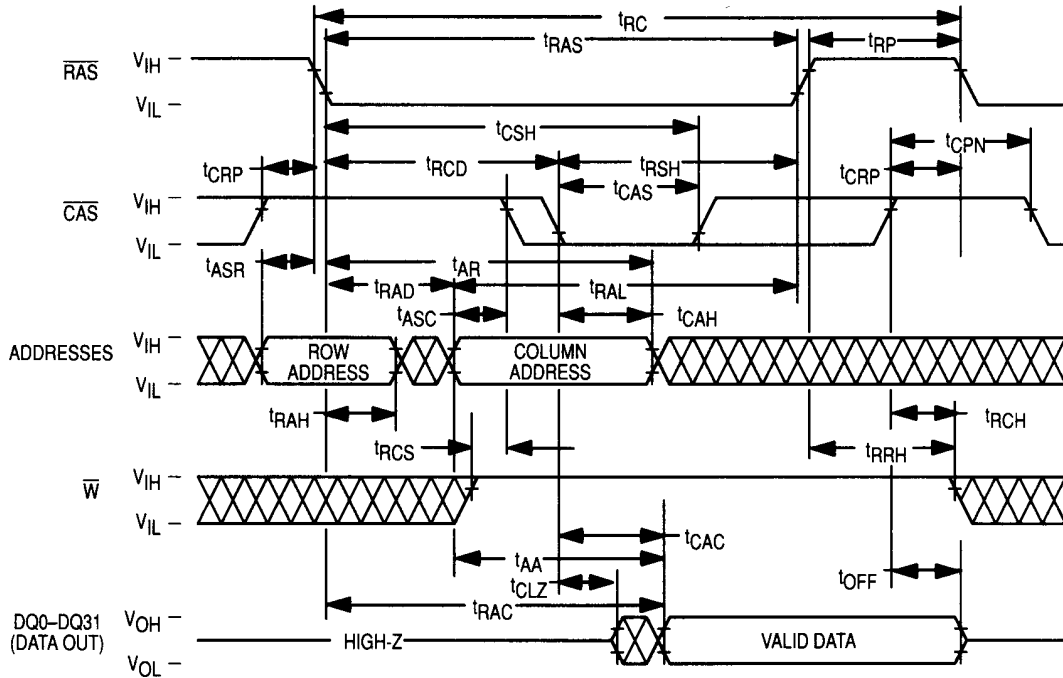
**READ AND WRITE CYCLES (Continued)**

Parameter	Symbol		MCM32200-80		MCM32200-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	$t_{\text{CEHREL}}$	$t_{\text{CRP}}$	5	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	$t_{\text{CEHCEL}}$	$t_{\text{CP}}$	10	—	10	—	ns	
Row Address Setup Time	$t_{\text{AVREL}}$	$t_{\text{ASR}}$	0	—	0	—	ns	
Row Address Hold Time	$t_{\text{RELAX}}$	$t_{\text{RAH}}$	10	—	15	—	ns	
Column Address Setup Time	$t_{\text{AVCEL}}$	$t_{\text{ASC}}$	0	—	0	—	ns	
Column Address Hold Time	$t_{\text{CELAX}}$	$t_{\text{CAH}}$	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	$t_{\text{RELAX}}$	$t_{\text{AR}}$	60	—	75	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	$t_{\text{AVREH}}$	$t_{\text{RAL}}$	40	—	50	—	ns	
Read Command Setup Time	$t_{\text{WHCEL}}$	$t_{\text{RCS}}$	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	$t_{\text{CEHWX}}$	$t_{\text{RCH}}$	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	$t_{\text{REHWX}}$	$t_{\text{RRH}}$	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	$t_{\text{CELWH}}$	$t_{\text{WCH}}$	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	$t_{\text{RELWH}}$	$t_{\text{WCR}}$	60	—	75	—	ns	
Write Command Pulse Width	$t_{\text{WLWH}}$	$t_{\text{WP}}$	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	$t_{\text{WLREH}}$	$t_{\text{RWL}}$	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	$t_{\text{WLCEH}}$	$t_{\text{CWL}}$	20	—	25	—	ns	
Data in Setup Time	$t_{\text{DVCEL}}$	$t_{\text{DS}}$	0	—	0	—	ns	14, 15
Data in Hold Time	$t_{\text{CELDX}}$	$t_{\text{DH}}$	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	$t_{\text{RELDX}}$	$t_{\text{DHR}}$	60	—	75	—	ns	
Refresh Period	MCM32200 MCM32L200	$t_{\text{RVRV}}$ $t_{\text{RFSH}}$	— —	16 128	— —	16 128	ms	
Write Command Setup Time	$t_{\text{WLCEL}}$	$t_{\text{WCS}}$	0	—	0	—	ns	15, 16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	$t_{\text{RELCEL}}$	$t_{\text{CSR}}$	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	$t_{\text{RELCEH}}$	$t_{\text{CHR}}$	30	—	30	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	$t_{\text{REHCEL}}$	$t_{\text{RPC}}$	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	$t_{\text{CEHCEL}}$	$t_{\text{CPT}}$	40	—	50	—	ns	
$\overline{\text{CAS}}$ Precharge Time	$t_{\text{CEHCEL}}$	$t_{\text{CPN}}$	10	—	15	—	ns	

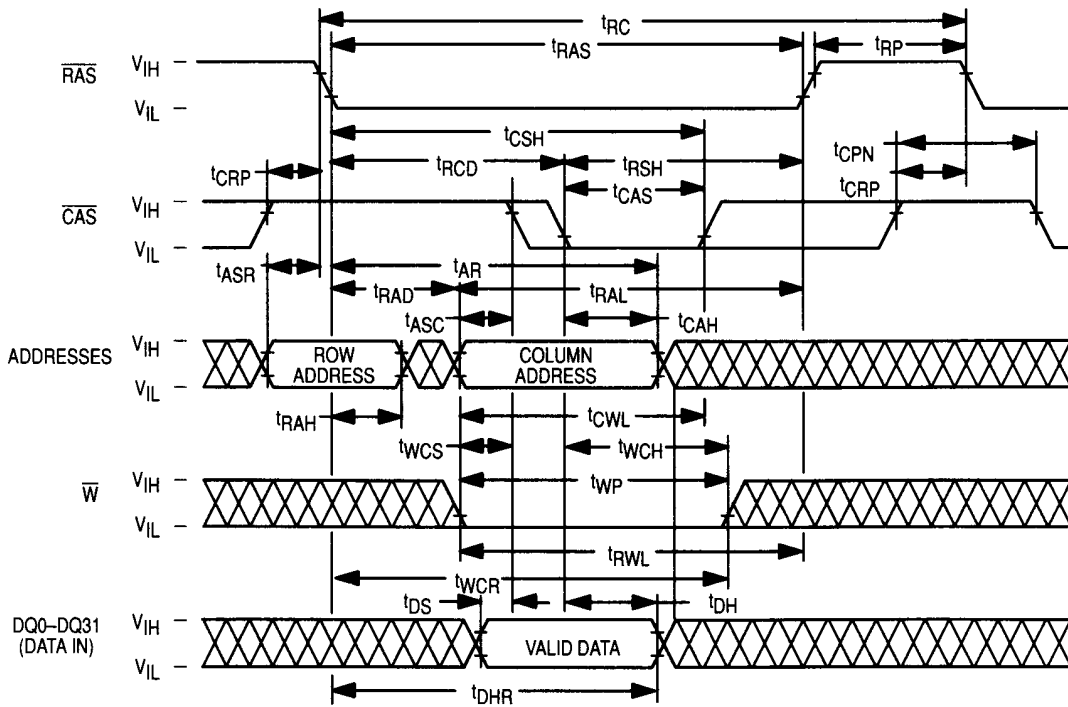
**NOTES:**

13. Either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be satisfied for a read cycle.
14. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in random write cycles.
15. Early write only ( $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ ).
16.  $t_{\text{WCS}}$  is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.
17. To avoid bus contention and potential damage to the module,  $\overline{\text{RAS0}}$  and  $\overline{\text{RAS1}}$  may not be active low simultaneously. Similarly,  $\overline{\text{RAS2}}$  and  $\overline{\text{RAS3}}$  may not be simultaneously active low.

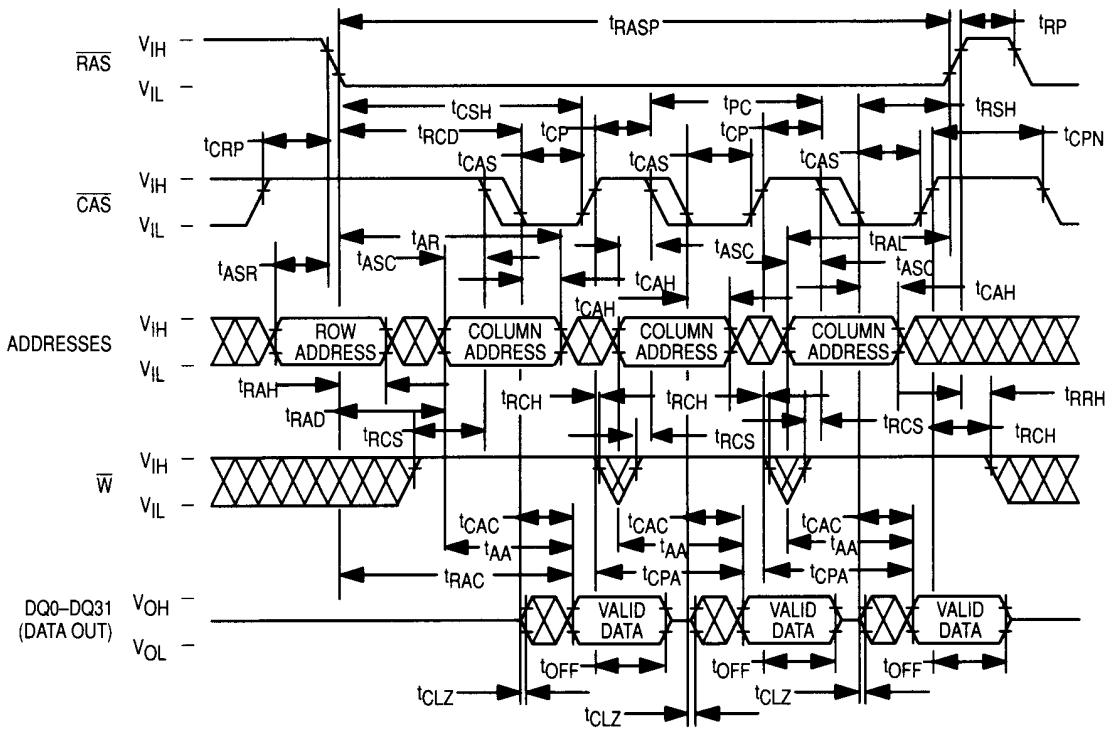
## READ CYCLE



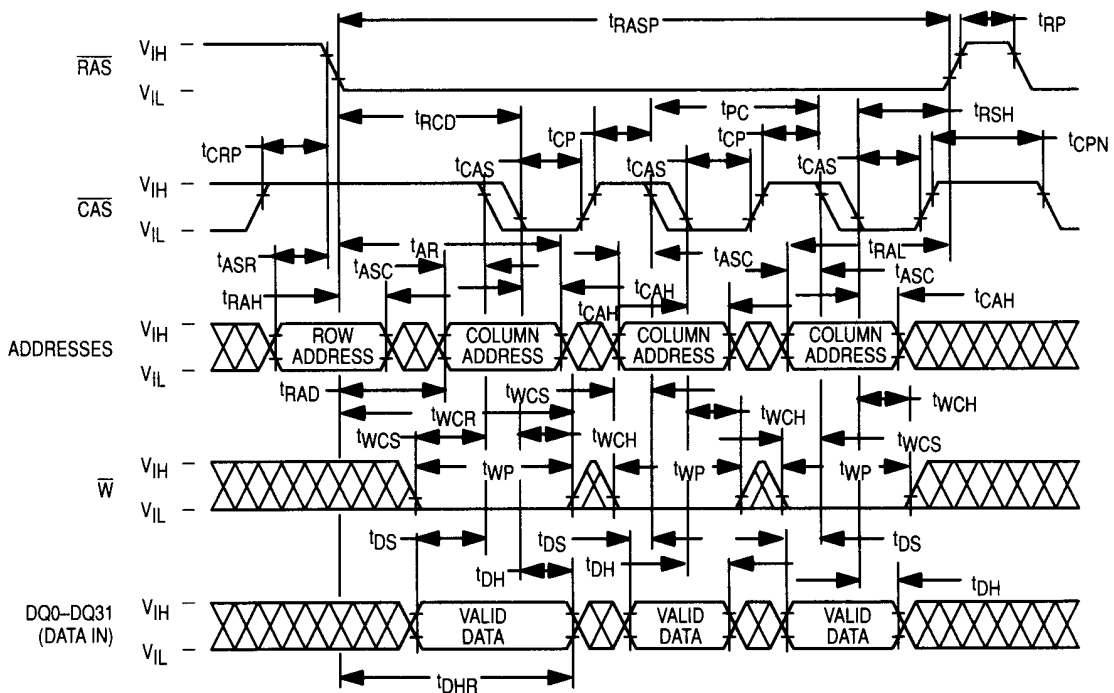
## EARLY WRITE CYCLE



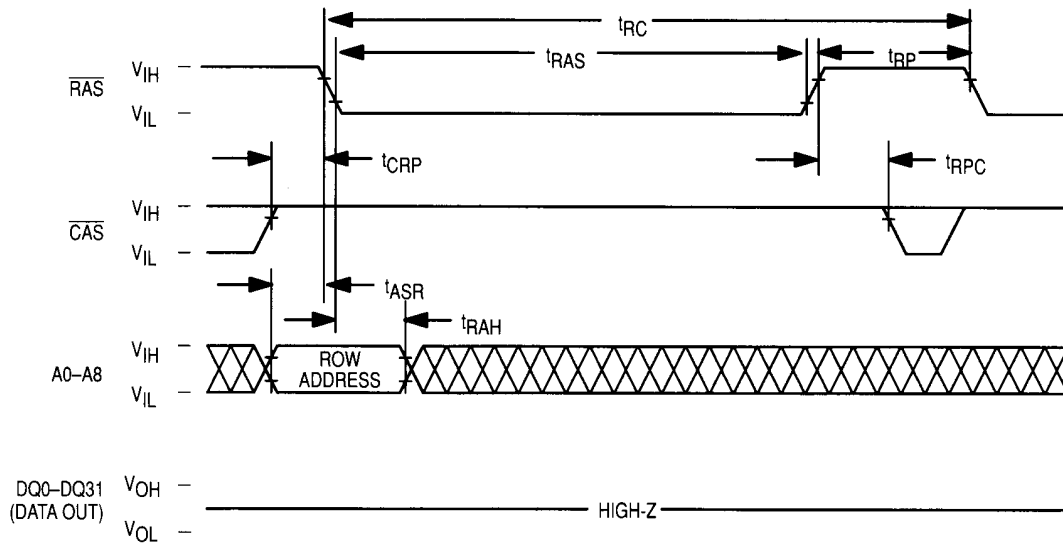
### FAST PAGE MODE READ CYCLE



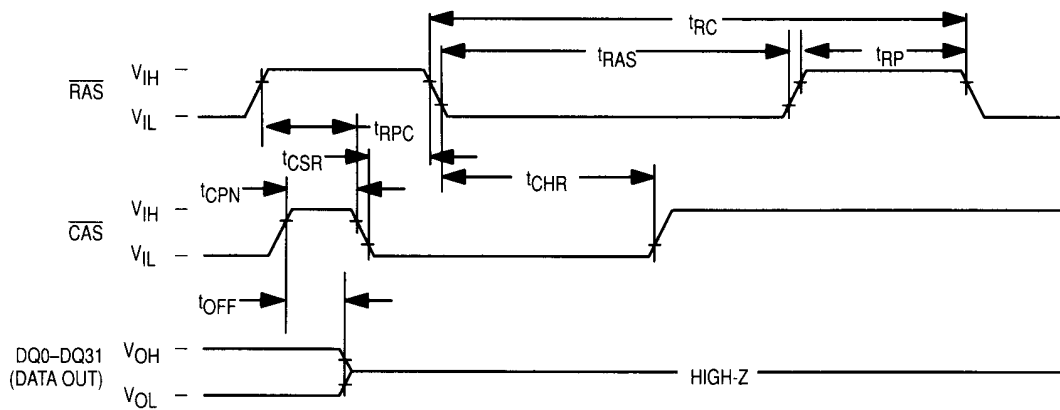
### FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



**RAS ONLY REFRESH CYCLE  
(W and A9 are Don't Care)**

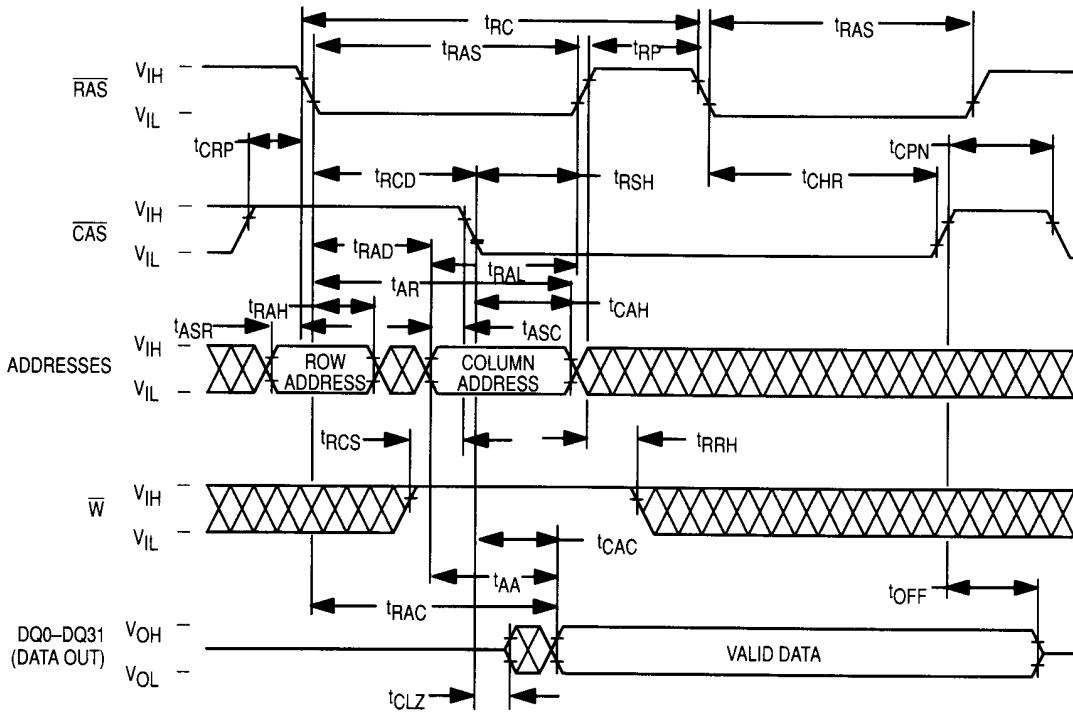


**CAS BEFORE RAS REFRESH CYCLE  
(W and A0 to A9 are Don't Care)**

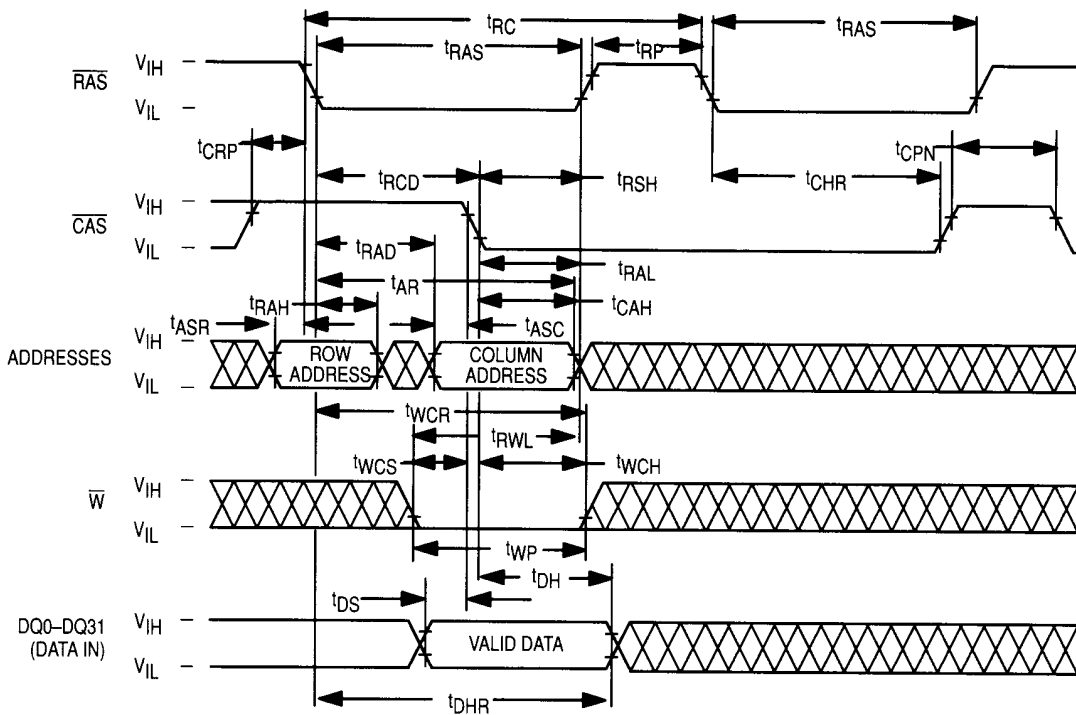




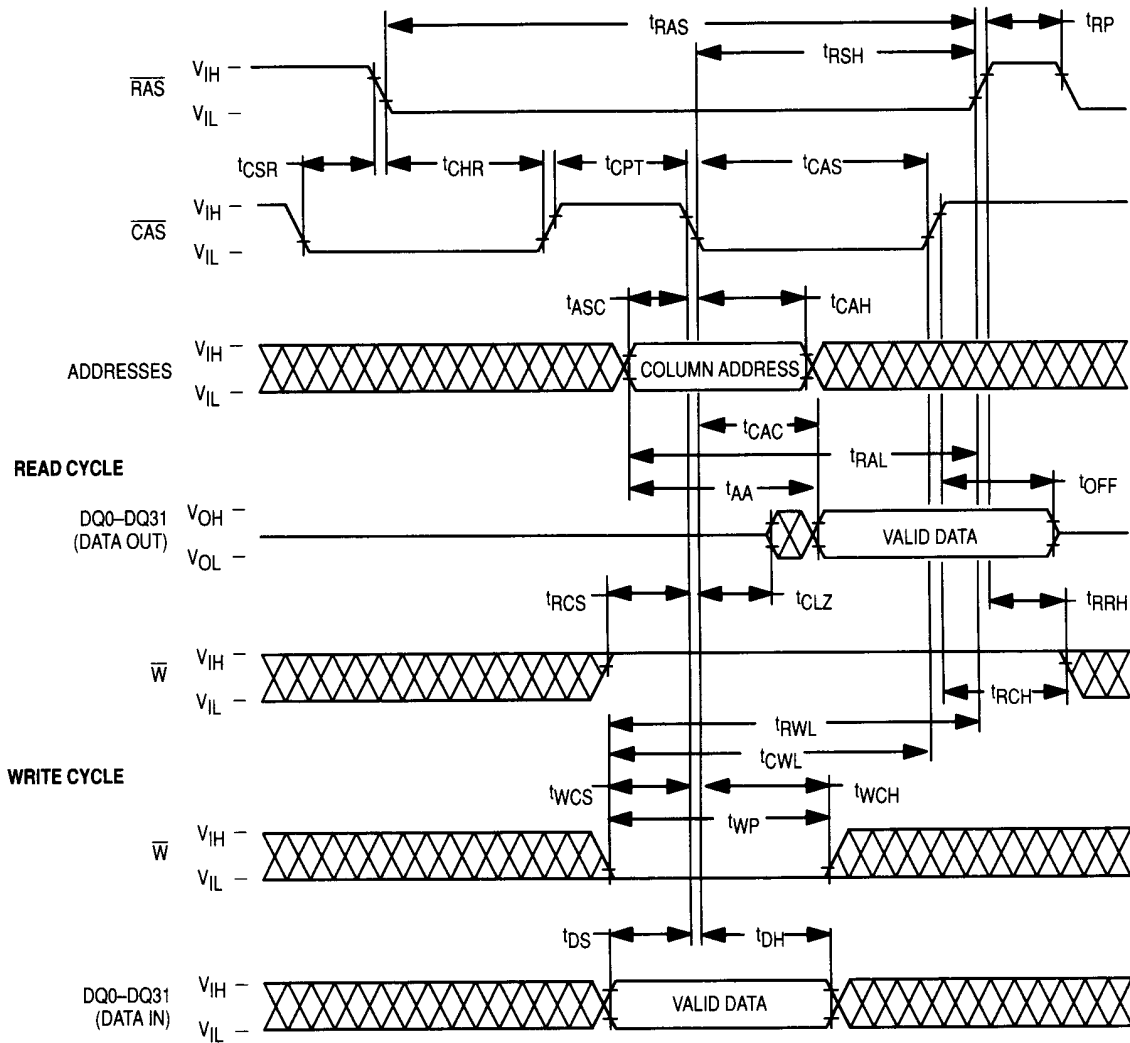
### HIDDEN REFRESH CYCLE (READ)



### HIDDEN REFRESH CYCLE (WRITE)



**CAS BEFORE RAS REFRESH COUNTER TEST CYCLE**



## DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

## ADDRESSING THE RAM

The ten address bus pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ( $\overline{RAS}$ ) and the column address strobe ( $\overline{CAS}$ ). A total of twenty address bits will decode one of the 2,097,152 word locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called  $t_{RCD}$ , which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. These are, however, two other variations in addressing the module, one is called the  $\overline{RAS}$  only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the  $\overline{RAS}$  clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called page mode, allows the user to column access all words within a selected row. (See **PAGE-MODE CYCLES** section.)

## READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the  $\overline{RAS}$  clock transitioning from  $V_{IH}$  to the  $V_{IL}$  level. The  $\overline{CAS}$  clock must also make a transition from  $V_{IH}$  to the  $V_{IL}$  level at the specified  $t_{RCD}$  timing limits when the column addresses are latched. Both the  $\overline{RAS}$  and  $\overline{CAS}$  clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the  $\overline{CAS}$  clock must be active before or at the  $t_{RCD}$  maximum specification for an access (data valid) from the  $\overline{RAS}$  clock edge to be guaranteed ( $t_{RAC}$ ). If the  $t_{RCD}$  maximum condition is not met, the access ( $t_{CAC}$ ) from the  $\overline{CAS}$  clock active transition will determine read access time. The external  $\overline{CAS}$  signal is ignored until an internal  $\overline{RAS}$  signal is available. This gating feature on the  $\overline{CAS}$  clock will allow the external  $\overline{CAS}$  signal to become active as soon as the row address hold time ( $t_{RAH}$ ) specification has been met and defines the  $t_{RCD}$  minimum specification. The time difference between  $t_{RCD}$  minimum and  $t_{RCD}$  maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the  $\overline{CAS}$  clock.

Once the clocks have become active, they must stay active for the minimum ( $t_{RAS}$ ) period for the  $\overline{RAS}$  clock and the mini-

mum ( $t_{CAS}$ ) period for the  $\overline{CAS}$  clock. The  $\overline{RAS}$  clock must stay inactive for the minimum ( $t_{RP}$ ) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the  $\overline{CAS}$  clock is active; the output will switch to the three-state mode when the  $\overline{CAS}$  clock goes inactive. To perform a read cycle, the write ( $\overline{W}$ ) input must be held at the  $V_{IH}$  level from the time the  $\overline{CAS}$  clock makes its active transition ( $t_{RCS}$ ) to the time when it transitions into the inactive ( $t_{RCH}$ ) mode.

## WRITE CYCLE

A write cycle is similar to a read cycle except that the write ( $\overline{W}$ ) clock must go active ( $V_{IL}$  level) at or before the  $\overline{CAS}$  clock goes active at a minimum  $t_{WCS}$  time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the  $\overline{CAS}$  clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time ( $t_{CWL}$ ) and the row strobe to write lead time ( $t_{RWL}$ ). These define the minimum time that  $\overline{RAS}$  and  $\overline{CAS}$  clocks need to be active after the write operation has started ( $\overline{W}$  clock at  $V_{IL}$  level).

## PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 1024 column locations on a selected row. Page access ( $t_{CAC}$ ) is typically half the regular  $\overline{RAS}$  clock access ( $t_{RAC}$ ) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the  $\overline{RAS}$  clock active while cycling the  $\overline{CAS}$  clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the  $\overline{RAS}$  clock, followed by the column address and  $\overline{CAS}$  clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter  $\overline{CAS}$  cycles ( $t_{PC}$ ). The  $\overline{CAS}$  cycle time ( $t_{PC}$ ) consists of the  $\overline{CAS}$  clock active time ( $t_{CAS}$ ), and  $\overline{CAS}$  clock precharge time ( $t_{CP}$ ) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

## REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 16 milliseconds. This is accomplished by sequentially cycling through the 1024 row address locations every 16 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

## $\overline{RAS}$ -Only Refresh

In this refresh method, the system must perform a  $\overline{RAS}$ -only cycle on 1024 row addresses every 16 milliseconds. The row addresses are latched in with the  $\overline{RAS}$  clock, and the associated internal row locations are refreshed. As the heading implies, the  $\overline{CAS}$  clock is not required and must be inactive or at a  $V_{IH}$  level.

### CAS Before RAS Refresh

This refresh cycle is initiated when  $\overline{RAS}$  falls, after  $\overline{CAS}$  has been low (by  $t_{CSR}$ ). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by  $\overline{CAS}$  in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as  $\overline{CAS}$  is held active (hidden refresh).

### Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding  $\overline{CAS}$  at  $V_{IL}$  and taking  $\overline{RAS}$  high and after a specified precharge period ( $t_{RP}$ ), executing a  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle. (See Figure 1.)

### CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a  $\overline{CAS}$  before  $\overline{RAS}$  refresh counter test. This refresh counter

test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of 8 **CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

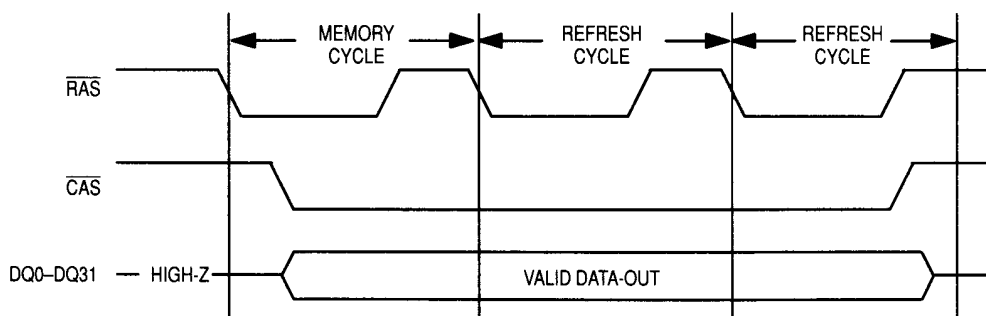
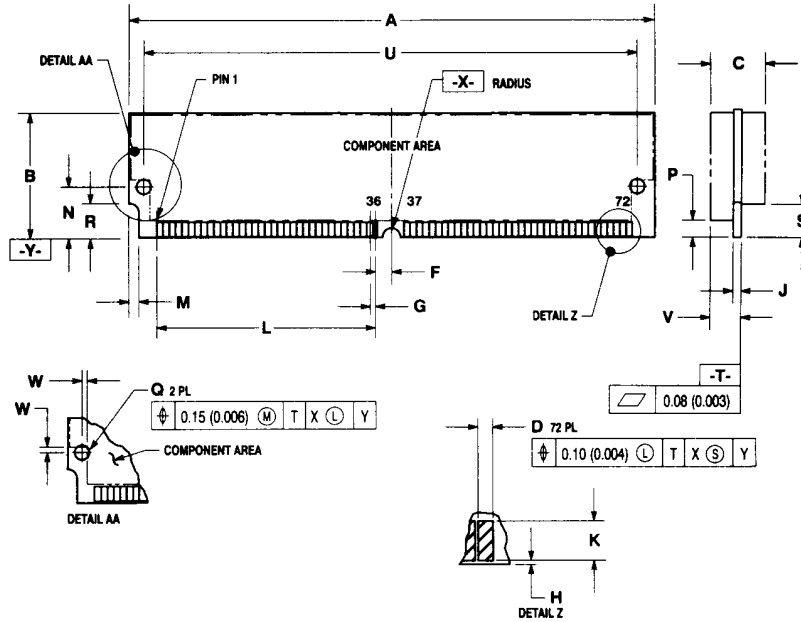


Figure 1. Hidden Refresh Cycle

# PACKAGE DIMENSION

## S PACKAGE SIMM MODULE CASE 866A-02

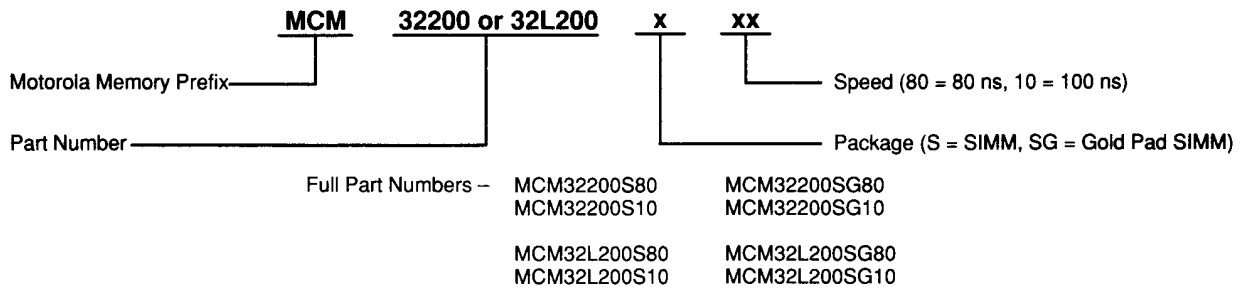


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	107.82	108.08	4.245	4.255
B	31.62	31.88	1.245	1.255
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC		0.125 BSC	
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.90	2.16	0.075	0.085
N	10.16 BSC		0.400 BSC	
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC		3.984 BSC	
V	—	5.28	—	0.208
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

### ORDERING INFORMATION (Order by Full Part Number)



NOTE: Contact your Motorola representative for further information on the Gold Pad SIMM packages.