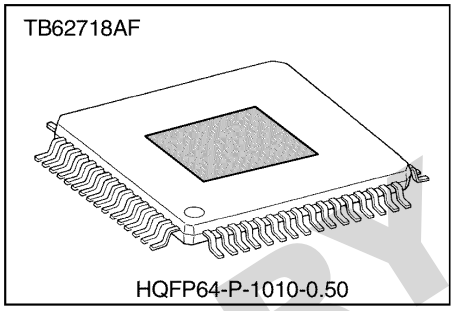
TOSHIBA Bi-CMOS INTEGRATED CIRCIUTS

T B 6 2 7 1 8 A F

Full color LED module and panel special controller and LED driver

TB62718AF is the LED-driver which is suitable for lighting of the full color LED module. This device builds in a PWM gray scale function and each output current value compensation function, and 16s LED can turn it on. Then, heat-sink connection side is on the surface of the package, and heat-sink is used, and this device can ease rise in temperature of the device. Furthermore, this device builds in TSD (ThermalShutDown) and an output open detection function as a protection function.

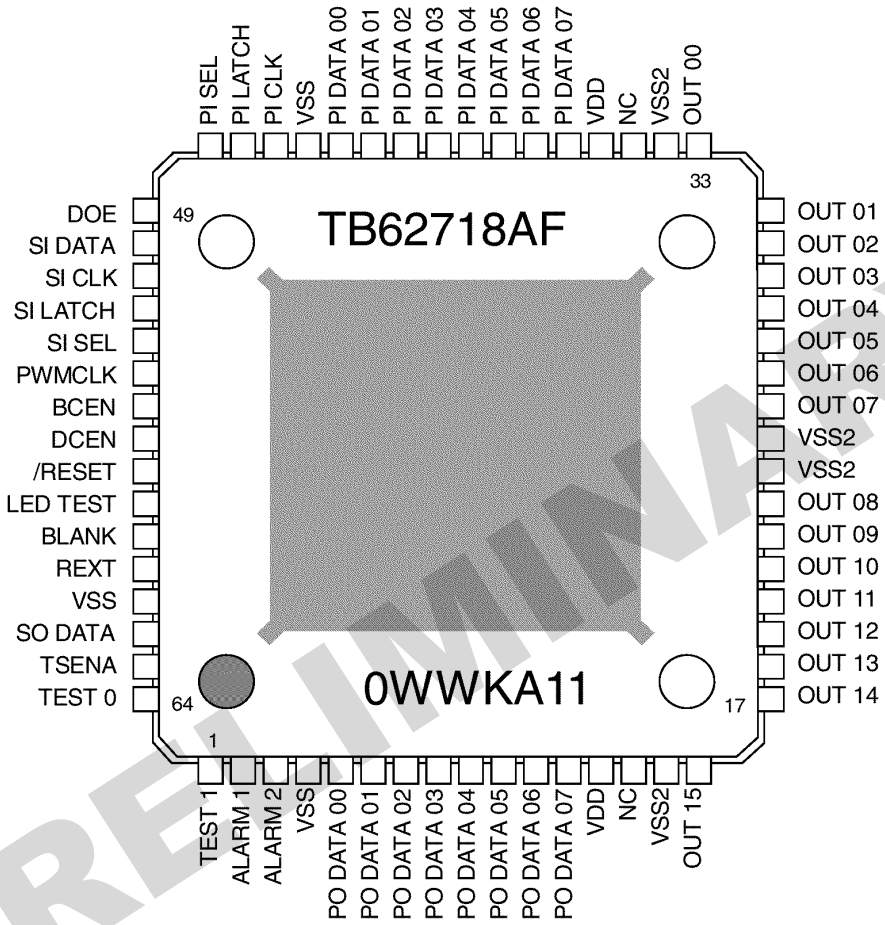


Weight: @ @ @ @(Typ.)

*Output Current Capability and the number of the output :
90mA X 16 outputs
*Constant Current Range : 5 to 90mA
*Application Output Voltage : 0.7V (output current 5 to 80 mA)
*Various Adjustment Functions
1:Standard Current Adjustment (Input 8bits by the serial data.)
This function supports standard current adjustment by the REXT resistance.
MSB side 2 bits --- Adjust Output Current 25%-100 % range in 4 step.
LSB side 6 bits --- Adjust Output Current 40%-100 % range in 64 step.
2:Dot Adjustment (Input it 128 bits by the serial data.)
This function adjusts the current value of each output.
--- Adjust Output Current 20-100% range in 64 step.
3: All Bit Adjustment 1(Input it 8bits by the parallel data.)
This function adjusts brightness for each LED module.
LSB side 5 bits --- Adjust Output Current 50%-100 % range in 32 step.
4: All Bit Adjustment 2 (Input it 8bits by the parallel data.)
This function changes the frequency of PWM clock, and adjusts brightness of the display greatly.
MSB side 3 bits --- Adjust PWM clock frequency 1/1 - 1/8 renge in 8 step.
5: 256 gray scale PMW function (Input it 8 bits by the parallel data.)
This function controls the pulse width of each output with 256 gray scale.
PWM clock frequency 10MHz (all the temperature ranges, muximum). Minimum pulse width 2 micro second.
*Protection Function
1: The Thermal Shut Down Function (TSD)
This function watches rise in temperature of the junction.
Connect pull up resistor with the ALARM1 terminal, and it can be monitored.
2: Output Terminal Open Detection Function
This function detects that output terminal opens.
Connect pull up resistor with the ALARM2 terminal, and it can be monitored.
*For Annode Common LED
*Input Signal Voltage Level : CMOS Level (Shmitt Triggered Input)
*Power Supply Voltage Range VDD=4.5 to 5.5V
*Muximum output terminal voltage 26V
*Serial and Pararell Data Transfer Rate 20MHz (max, Cascade Connection)
*Operation Temperature Range Topr= -40 to 85 degrees
*Package : HQFP64-P-1010-0.50. Heat-Sink can be connected.
*Attention point in application :
There is fear of the device destruction in the short circuit of the output terminal to GND and the power supply.
Be fully careful of wiring of the output terminal, the power supply terminal, the GND terminal (VSS, VSS2).
Don't do soldering, increasing electric potential (Plus, minus aren't asked to it.) to heat-sink terminal.

Pin layout(TOP VIEW) and marking

Pakage type : HQFP64-P-1010-0.50

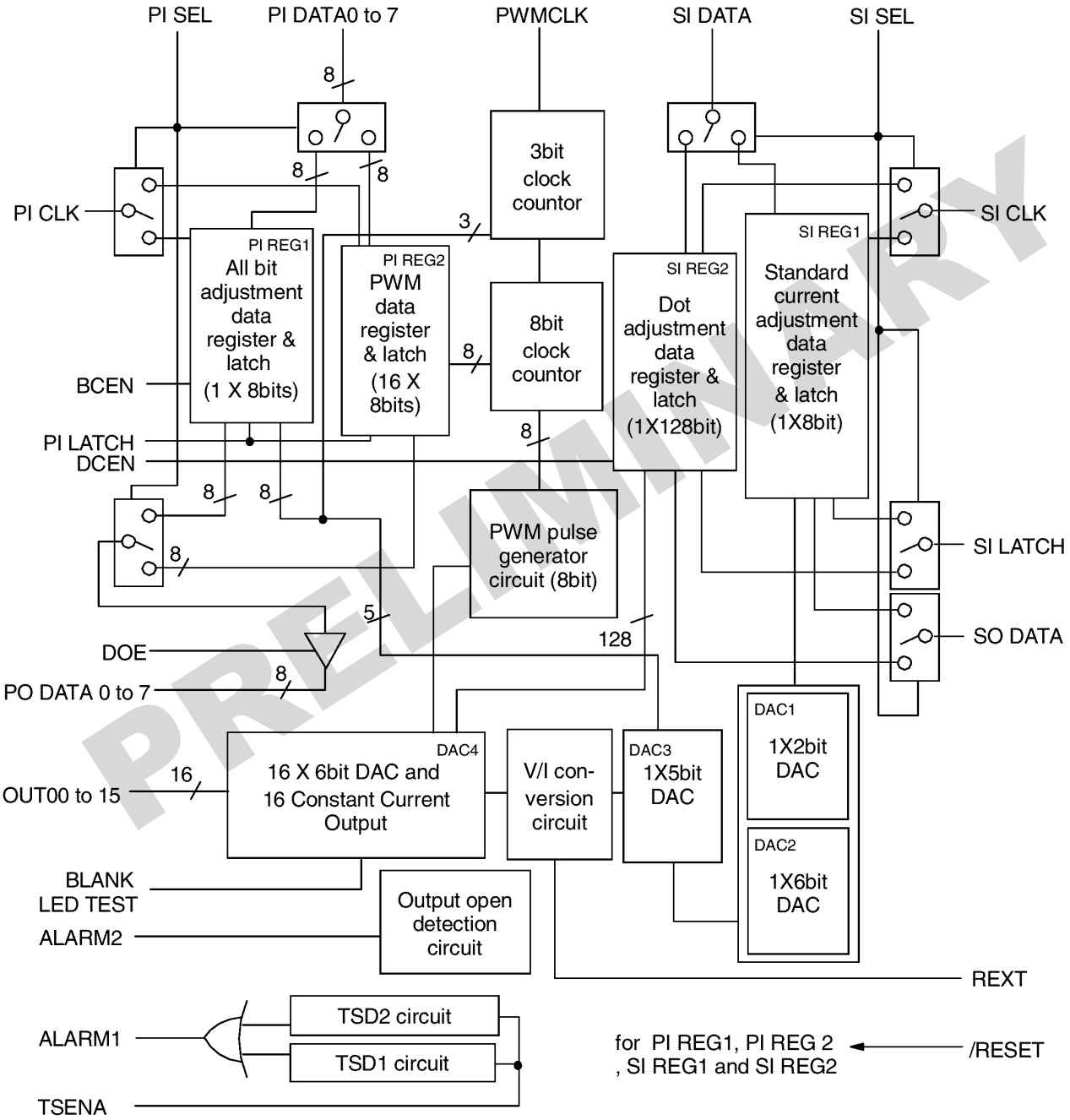


Note : Indicate device name on the upside of the package.
Indicate weekly code bottomside of the package.

The details of the weekly code of the bottom side :
From the left of the weekly code,
1st Character = A.D. rightmost digit.
Write 0 in the case of 2000, and write 1 in the case of 2001.
2nd and 3rd Character = Write that it was manufactured in a what week of the year. Muximum 52.
4th Character = Manufacture factory indication.
("K" is the meaning of our Kita Kyushu factory production.)
5th to 7th Character = Write manufacture lot number out of 1 week.

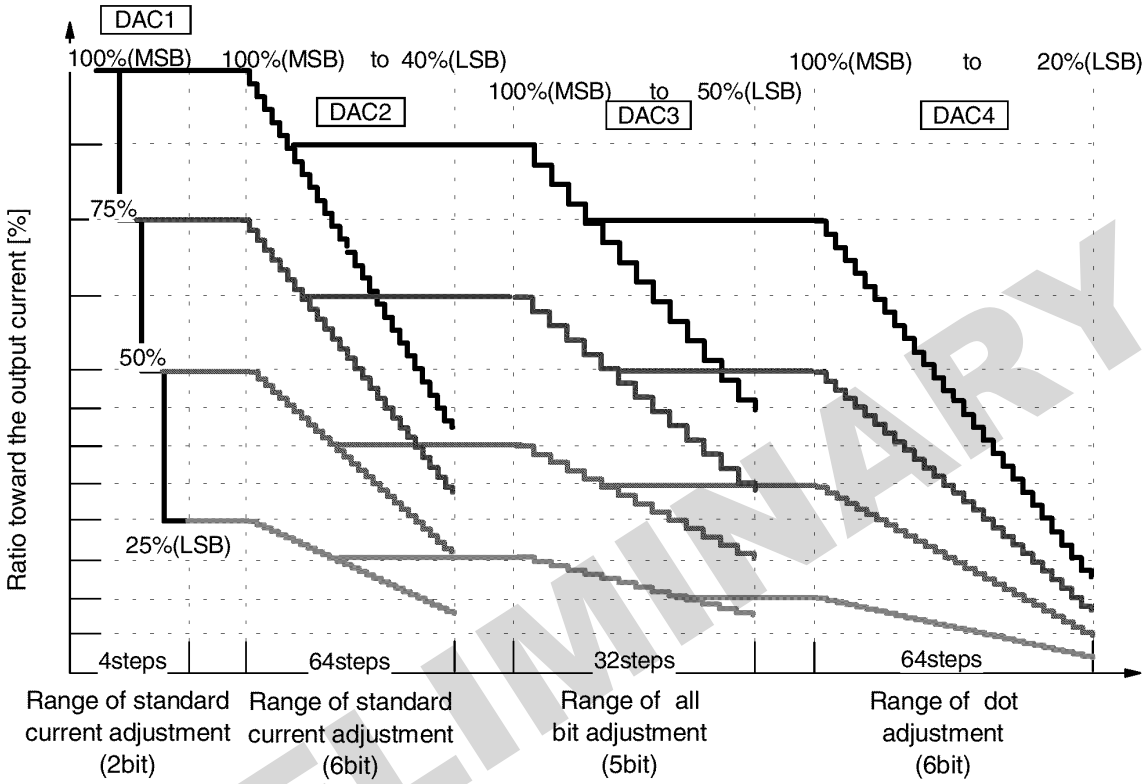
Write the 1st Lot with A11. 2nd Lot with A1 and 3rd Lot with A.
Write the 4th Lot with B11. 5th Lot with B1 and 6th Lot with B.
Write the 64th Lot with Z11. 65th Lot with Z1 and 66th Lot with Z.
Four characters of "I", "M", "O", "W" aren't used in consideration of the correctness of marking.

Block Diagram (whole figure)



Constant current adjustment range (image)

GRAPH: : Currnet adjustment range that it was done based on 100%



Note : The mutual relationship of the front step DAC and the rear step DAC makes the adjustment result of the former step 100%.

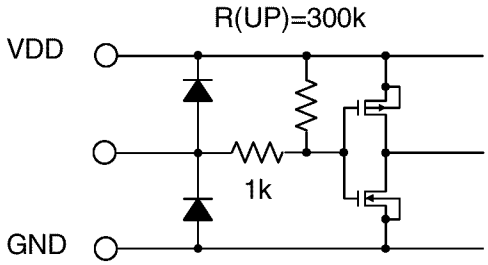
Reference :
About each current adjustment function.
DAC1 to DAC3 is the current adjustment function of all the output.
The adjustment width of DAC1 is big and rough. (about 1LSB= 25%)
The adjustment width of DAC2 is the smallest, and the error of it is big. (about 1LSB= 0.9%)
The adjustment width of DAC3 is small, and it is the high performance DAC whose error is small.
(about 1LSB=1.61%)
Therefore, recommend using it for the change of the absolute value of the REXT resistance and the adjustment of the REXT resistance dispersion with DAC1 and DAC2.
Recommend using it for brightness adjustment between the module with DAC3.
(After it was set and it had DAC4 adjusted to the dot.)
The beginning is set in about 75% of the middle value, and it is effective to use +- 25% of set width.
DAC4 is the current adjustment function of each output.
The adjustment width of DAC4 is small, and it is the high performance DAC whose error is small.
(about 1LSB= 1.27%)
And, DAC4 has very wide set range.
Therefore, adjust DAC4 including brightness dispersion of LED which rank classification hasn't been carried out on.
Then, it is presumed that brightness dispersion of all the output is adjusted to the one within 1.27%(Note1).

Note 1 : It is when it guesses that there is correlation between the output current and LED brightness.

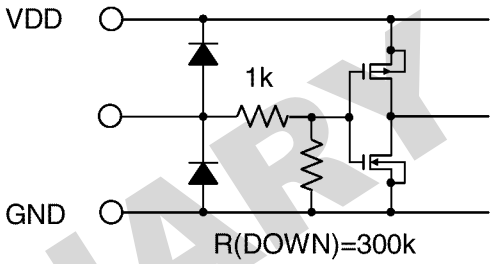
Equivalent input and output schematics

(Resistance value is standard value)

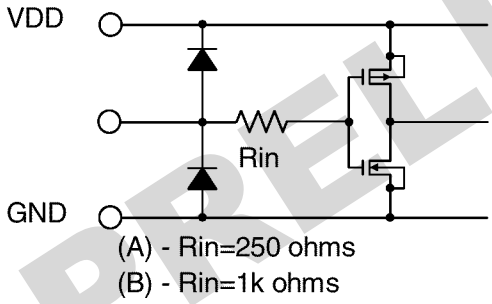
1. Input terminal with the pull up resistor
TSENA, BLANK, BCEN, DCEN



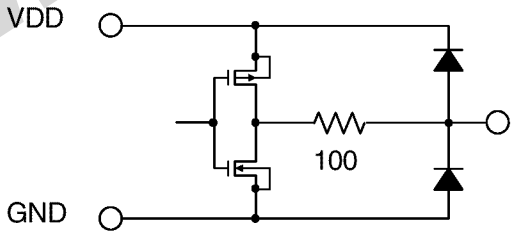
2. Input terminal with the pull down resistor.
SI/PI LATCH, PI DATA0 to 7. LEDTEST



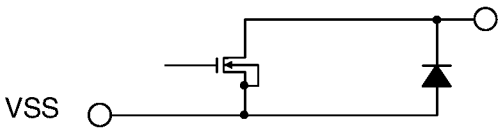
3. Input terminal.
SI DATA, SI/PI CLK, PWMCLK -(A)
/RESET, DOE, PI/SI SEL -(B)



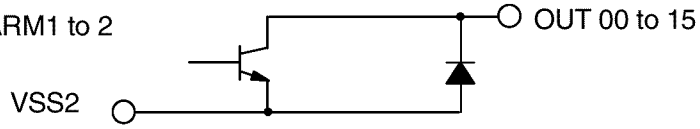
4. Output terminal
ALARM1 to 2, PO DATA 0 to 7, SO DATA



5. Protection circuit monitor terminal



6. Constant current output terminal



TERMINAL FUNCTION EXPLANATION TABLE

TERMINAL				FUNCTION EXPLANATION
NO.	NAME	I/O		
4,45	VSS	P	-	These are logic ground terminals. Please, must use all.
35,14	NC	-	-	These are the terminals which haven't been used.
63	TSENA	I	Pull Up	This is the terminal which does resetting of the TSD circuit. Cancel it on the edge of the rise of this input signal when TSD circuit moves and the condition that it offs all has all the output. The data that latch is worn aren't reset. TSD circuit moves regardless of the voltage level of this terminal.
15,24,25,34	VSS2	P	-	These are the ground terminals of the output. Please, must use all.
13,35	VDD	P	-	These are logic power supply input terminals. Please, must use all.
16,23,26,33	OUT00 to 15	O	-	These are LED drive output terminals. Connect cathode of LED.
50	SI DATA	I	-	This is a serial data input terminal. Input standard current adjustment data and dot adjustment data.
51	SI CLK	I	-	This is a serial data transfer clock input terminal. Transfer data by up edge.
52	SI LATCH	I	Pull Down	This is a serial data latch signal input terminal. Hold data by up edge.
53	SI SEL	I	-	This is a serial data choice terminal. Choose either standard current adjustment data or dot adjustment data.
62	SO DATA	O	-	This is a serial data output terminal. Output data are chosen with SI SEL.
37 to 44	PI DATA 0 to 7	I	Pull Down	These are pararell data input terminals. Input all the output adjustment data and PWM data.
45	PI CLK	I	-	This is pararell data transfer clock input terminal. Transfer data by up edge.
47	PI LATCH	I	Pull Down	This is pararell data latch signal input terminal. Hold data by up edge.
48	PI SEL	I	-	This is pararell data choice terminal. Choose either all the output adjustment data or PWM data.
5 to 12	PO DATA 0 to 7	O	-	This is pararell data output terminal. Output data are chosen with PISEL.
49	DOE	I	-	This is the control terminal of pararell data output PODATA. PIDATA is outputted by input of H level. And, it is set up in the high impedance by input of L level.
59	BLANK	I	Pull Up	This terminal is a PWM circuit movement control signal input terminal. It becomes output off by input of H level. And, start PWM output by input of L level.
54	PWMCLK	I	-	This is the standard clock input terminal of the PWM circuit. This clock 1 cycle is equivalent to the minimum pulse width of the PWM output.
55	BCEN	I	Pull Up	This is the use choice signal input terminal of all the output adjustment functions. All output adjustment is fixed on 100% in the L level. And, all bit adjustment becomes effective in the H level.
56	DCEN	I	Pull Up	This is the use choice signal input terminal of the dot adjustment function. Dot adjustment value is fixed on 100% in the L level. And, dot adjustment becomes effective in the H level.
57	/RESET	I	-	This is a reset signal input terminal. Reset all the register data in the L level. Or, use it for a release of TSD.
58	LED TEST	I	Pull Down	This is the connection confirmation signal input terminal of LED. All the output ons in the H level. Use it in the L level usually.
60	REXT	P	-	This is the connection terminal of the standard current set resistance.
2	ALARM1	O	-	This is open drain type with the monitor terminal of the TSD circuit. TSD circuit detects unusual temperature, and ons. Pull up does by the resistance to monitor it. ALARM1 moves independently in the /RESET signal.
3	ALARM2	O	-	This is open drain type with the monitor terminal of the output open detection circuit. Output opening is detected, and ALARM2 ons.
1,64	TEST 0 to 1	I	-	These are the terminals to use for the device test. Connect all with the L level.

Terminal attribute) P : Power Supply/Ground/Others, I : Input Terminal, O : Output Terminal
Recommend not making terminal with the pull up/down resistor open.
There is fear of faulty operation by the circumference noise.

Absolute Maximum Ratings

(Topr = 25 degC, unless otherwise noted.)

DC Characteristic	Symbol	Rating	Unit	Notes
Supply voltage	VDD	-0.3 to 7	V	
Constant current output voltage	VO	-0.3 to 26		
Output current	IOUT	90	mA/bit	
Logic output voltage	VOUT	-0.3 to VDD+0.3	V	
Logic input voltage	VIN	-0.3 to VDD+0.3	V	
VSS2 current in total	IVSS2	1440	mA	Must use VSS2 (4 terminal) all. When all isn't used, all characteristic guarantees can't be done.
Power dissipation	Pd	1.00	W	Free Air
		1.19		On PCB 100X100X 1.6mm
		5.0		On PCB of the Infinity
Saturation heat resistance of package	Rth(j-a)	125	degC/W	Free Air
		105		On PCB 100 X 100 X 1.6mm
	Rth(j-c)	25		On PCB of the Infinity
Operating temperature	Topr	-40 to 85	degC	
Strage temperature	Tstg	-55 to 150		

NOTE :
Subtract 0.95 mW/degC from the muximum rating value about 1 degC if operation temperature exceeds 25 degC. On PCB 100 X 100 X 1.6mm.

Recommended Operating Condition

DC characteristic	Symbol	Condition & Terminal	Min	Typ	Max	Unit
Supply voltage	VDD		4.5	5.0	5.5	V
High level input voltage	VIH	PI DATA, PI CLK, PI SEL, PI LATCH, SI DATA, SI CLK, SI SEL, SI LATCH, PWMCLK	0.7VDD		VDD	
Low level input voltage	VIL	BLANK, LED TEST, TSENA,DOE, DCEN, BCEN	VSS		0.3VDD	
High level output current	IOH	DATA PO0 to 7 , DATA SO			-1	mA
Low level output current	IOL	VDD=4.5V, ALARM1 to 2			+1	
Constant current cutput	IOUT	OUT00 to 15	+5		+80	mA/bit
Output voltage	VO	OUT00 to 15 off.			+26	V
	VOH	ALARM1 to 2 off.			+5	
Operating temperature	Topr		-40		+85	degC

Recommended Operating Condition (continue)

(VDD= 4.5 to 5.5V, Topr = -40 to 85 degC, unless otherwise noted.)

AC characteristics	Symbol	Condition & Terminal	Min	Typ	Max	Unit
Clock frequency	fPWM	Ratio of High/Low Level = 50%, PWMCLK			10	MHz
	fPI1	PI CLK, Solo			15	
	fPI2	PI CLK, cascade connected			10	
	fSI1	SI CLK			15	
	fSI2	SI CLK, cascade connected			10	
Minimum pulse width	twH/twL	PWM CLK	30			ns
		PI CLK, SI CLK	30			
	twltH/tpltL	PI LATCH. SI LATCH	50			ns
	twrstH/twrstL	/RESET	50			
	twblkH/twblkL	BLANK	400			
	twledH/twledL	LED TEST	400			
Setup time	tsetup	PI DATA -> PI CLK	10			ns
		PI LATCH -> PI CLK	10			
		SI DATA -> SI CLK	10			
		SI LATCH -> SI CLK	10			
		SI LATCH -> SI SEL	50			
Hold time	thold	PI DATA -> PI CLK	5			
		PI LATCH -> PI CLK	5			
		SI DATA -> SI CLK	5			
		SI LATCH -> SI CLK	5			
		SI LATCH -> SI SEL	50			

Electrical Characteristics 1

(Typ:VDD=5.0V, Topr=25degC, Min/Max:VDD=4.5 to 5.5V, Topr=-40 to 85 degC)

Parameter	Symbol	Test Condition & Terminal	Min	Typ	Max	Unit
High level output voltage	VOH	IOH=-1mA, PO DATA0 to 7, SO DATA	VDD -0.4			V
Low level output voltage	VOL	IOL=1mA, PO DATA0 to 7, SO DATA			0.4	
		IOL=+1.0mA, ALARM1 to 2			0.3	
Tristate output leakage current	IOZ	VOUT=VDD or VSS, PO DATA0 to 7		+-0.5	+-5	uA
Input current	II	All terminal which pull up/pull down resistor is not in.			+-1	
Supply current	IDD1	PI DATA=1/2 PI CLK SI DATA=1/2 SI CLK PI CLK=SI CLK=20MHz PWMCLK = "L", BLANK = "H" Set condition *1		20	30	mA
	IDD2	PI DATA=SI DATA="L" PI CLK=SI CLK="L" PWM CLK=20MHz Set condition *5a		75	105	
	IDD3	PI DATA=1/2 PI CLK SI DATA=1/2 SI CLK PI CLK=SI CLK=PWMCLK=20MHz Set condition *5a		80	115	
	IDD4	PI DATA=SI DATA="L" PI CLK=SI CLK="L" PWM CLK=20MHz, Set condition *6a		90	140	
	IDD5	PI DATA=1/2 PI CLK SI DATA=1/2 SI CLK PI CLK=SI CLK=PWM CLK=20MHz Set condition *6a		95	150	

NOTE: Electrical Characteristics Set Condition

(OUT0 to 15 All on, VO=0.7V and REXT=2.7kohms, unless otherwise norted)

No.	Set Condition	All bit adjustment "DAC3"	Constant Output Currnet (typ)
*1	Output all off, VO=26V, DAC1-2- 4=MSB, BLANK=H	DAC3=31	IOUT=0mA
*2	DAC1=0, DAC2= 0, DAC4=63, BLANK=L		IOUT=7.1mA
*3a	DAC1=0, DAC2=17, DAC4=63, BLANK=L		IOUT=10mA
*4a	DAC1=1, DAC2=17, DAC4=63, BLANK=L		IOUT=20mA
*5a	DAC1=2, DAC2=37, DAC4=63, BLANK=L		IOUT=40mA
*6a	DAC1=3, DAC2=51, DAC4=63, BLANK=L		IOUT=60mA
*7	DAC1=3, DAC2=63, DAC4=63, BLANK=L		IOUT=71mA
*3b	DAC1=0, DAC2=17, DAC4=63, BLANK=L	DAC3=00	IOUT=5mA
*4b	DAC1=1, DAC2=17, DAC4=63, BLANK=L		IOUT=10mA
*5b	DAC1=2, DAC2=37, DAC4=63, BLANK=L		IOUT=20mA
*6b	DAC1=3, DAC2=51, DAC4=63, BLANK=L		IOUT=30mA

Electrical Characteristics 2

(Typ:VDD=5.0V, Topr=25degC, Min/Max:VDD=4.5 to 5.5V, Topr=-40 to 85 degC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Constant Cuurnet Output (within current error between bits)	IO1	Set condition *7	60.4	71	81.6	mA
	IO2	Set condition *6a	51.2	60	69.2	
	IO3	Set condition *5a	34.1	40	46.1	
	IO4	Set condition *4a	16.5	20	23.2	
	IO5	Set condition *3a	7.8	10	12.2	
	IO6	Set condition *2	4.54	7.1	9.65	
Constant current output depends on temperature	%TOPR1	Set condition *6a,VOUT=1.0V, Topr is changed from -40 to 85degC.		+-50	+-80	uA /degC
	%TOPR2	Set condition *4a,VOUT=1.0V, Topr is changed from -40 to 85degC.		+-25	+-50	
Leakage current of the constant current output	IOLK	Set condition *1, VOUT=26V		0.05	0.1	uA
Constant Current Error bitween bits	dIOUT1	Set condition *6a, VOUT=0.7V		+-2.5	+-6	%
	dIOUT2	Set condition *5a, VOUT=0.7V		+-3.5	+-6	
	dIOUT3	Set condition *4a, VOUT=0.7V		+-5.5	+-7	
	dIOUT4	Set condition *3a, VOUT=0.7V		+-7	+-12	
Dot adjustment deviation between bits (When DAC3 data were changed from MSB to LSB.)	%IOUT1	Set condition is changed from *6a to *6b.		+-1	+-3	
	%IOUT2	Set condition is changed from *5a to *5b.		+-1.5	+-3	
	%IOUT3	Set condition is changed from *4a to *4b.		+-3.5	+-5	
	%IOUT4	Set condition is changed from *3a to *3b.		+-6	+-12	
Constant current output depends on output voltage	%VOUT	Set condition *6a, VO is changed from 0.7V to 3V.		+-5	+-8	
		Set condition *4a, VO is changed from 0.7V to 3V.		+-3	+-6	
Constant current output depends on supply voltage	%VDD	Set condition *6a, VDD is changed from 4.5V to 5.5V		+-1	+-2	
TSD detection temperature	Tsd1		120	140	160	degC
	Tsd2		140	160	180	
Output open detection voltage	VARL	ALARM2		0.04VDD		V
Pull up/down resistor	Rup /Rdw		150k	300k	600k	ohms

NOTE: Electrical Characteristics Set Condition

(OUT0 to 15 All on, VO=0.7V and REXT=2.7kohms, unless otherwise norted)

No.	Set Condition	All bit adjustment "DAC3"	Constant Output Currnet (typ)
*1	Output all off, VO=26V, DAC1-2- 4=MSB, BLANK=H	DAC3=31	IOUT=0mA
*2	DAC1=0, DAC2= 0, DAC4=63, BLANK=L		IOUT=7.1mA
*3a	DAC1=0, DAC2=17, DAC4=63, BLANK=L		IOUT=10mA
*4a	DAC1=1, DAC2=17, DAC4=63, BLANK=L		IOUT=20mA
*5a	DAC1=2, DAC2=37, DAC4=63, BLANK=L		IOUT=40mA
*6a	DAC1=3, DAC2=51, DAC4=63, BLANK=L		IOUT=60mA
*7	DAC1=3, DAC2=63, DAC4=63, BLANK=L		IOUT=71mA
*3b	DAC1=0, DAC2=17, DAC4=63, BLANK=L	DAC3=00	IOUT=5mA
*4b	DAC1=1, DAC2=17, DAC4=63, BLANK=L		IOUT=10mA
*5b	DAC1=2, DAC2=37, DAC4=63, BLANK=L		IOUT=20mA
*6b	DAC1=3, DAC2=51, DAC4=63, BLANK=L		IOUT=30mA

Switchin characterictics

(Typ : VDD=5V, Topr=25degC, CL=50pF,

Min/Max : VDD=4.5 to 5.5V, Topr=-40 to 85degC, CL=50pF, unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tristate output propagation delay for enable	tpZH/ZL	DOE -> PO DATA 0 to 7	8	16	30	ns
Tristate output propagation delay for disenable	tpHZ/LZ	DOE -> PO DATA 0 to 7	8	16	30	
Rise time	tr	OUT 00 to 15	10	17	30	
		ALARM1 to 2	0.2	0.4	0.8	us
Fall time	tf	OUT 00 to 15	20	40	70	ns
		ALARM1 to 2	2	4	8	ns
Propagation delay	tpHL	BLANK -> OUT 00 to 15	30	60	120	ns
	tpLH	PWM CLK -> OUT 00 to 15	70	120	200	
	tpHL		40	70	140	
	tpLH	LED TEST -> OUT00 to 15	60	110	190	
	tpHL		30	60	130	
	tpHL	/RESET -> OUT 00 to 15	30	60	130	
	tpd	PI CLK -> PO DATA 0 to 7	20	30	70	
		PI SEL -> PO DATA 0 to 7	20	30	70	
		SI CLK -> SO DATA	10	18	40	
		SI SEL -> SO DATA	10	20	40	

Operating explanation and truth value table (1/12 pages)

Serial data transfer : standard current adjustment DAC1 and DAC2
(about the data register SI REG[7 : 0])

	SI DATA	SI CLK	SI LATCH	SI SEL	SO DATA	Operating and function
1	H or L	(8times)	L	H	H or L	Choose the input data of standard current adjustment (8 bits,2bits and 6bits) with SI SEL=H. Transfer data to SI REG1 by up edge 8times input of SI CLK.
2		L	(1time)	H	No Change	Hold the data transferred to SI REG1 by up edge of SI LATCH. Set is reflected on standard current adjustment from the moment when it is held.

Figure 1-1 : serial data transfer timing figure
(standard current adjustment, the case of SI SEL= H, for example of 1 device.)

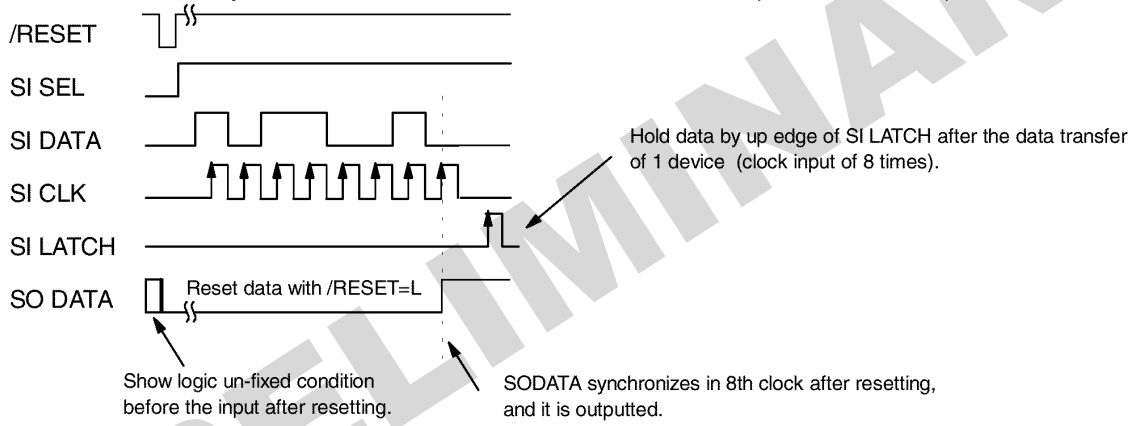
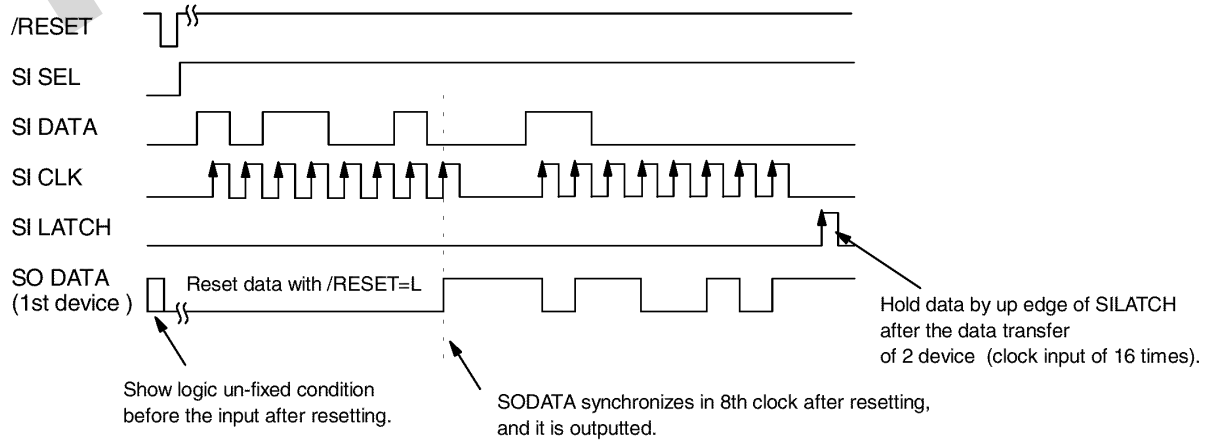


Figure 1-2: serial data transfer timing figure
(standard current adjustment, the case of SI SEL=H,
for example of cascade connected of 2 devices.)



Operating explanation and truth value table (2/12 pages)

Serial data transfer : dot adjustment DAC4.
(about the data register SI REG2[127 : 0])

	SI DATA	SI CLK	SI LATCH	SI SEL	SO DATA	Operating and function
1	H or L	(128 times)	L	L	H or L	Choose the input data of dot adjustment (128 bits) with SI SEL=L. Transfer data to SI REG2 by up edge 128 times input of SI CLK.
2		L	(1time)	L	No Change	Hold the data transferred to SI REG2 by up edge of SI LATCH. Set is reflected on dot adjustment from the moment when it is held.

Figure 2-1 : serial data transfer timing figure
(dot adjustment, the case of SI SEL= L, for example of 1 device.)

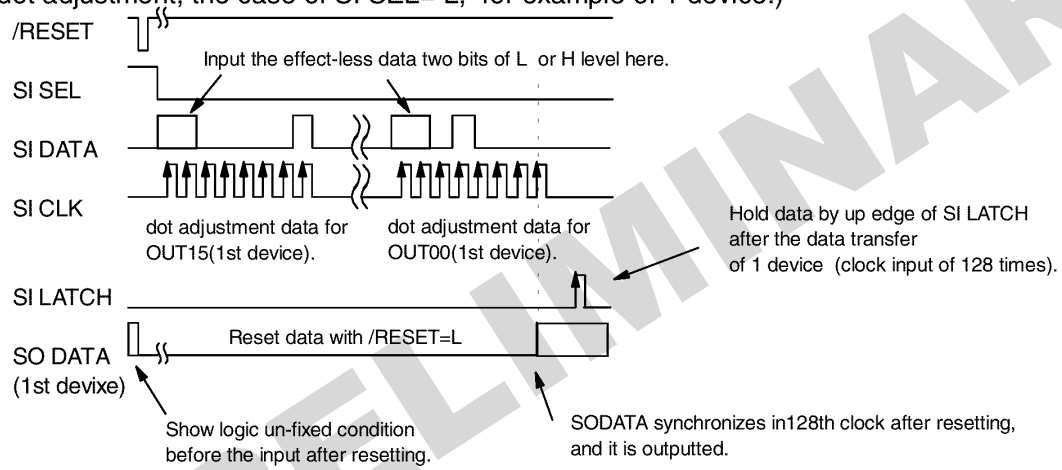
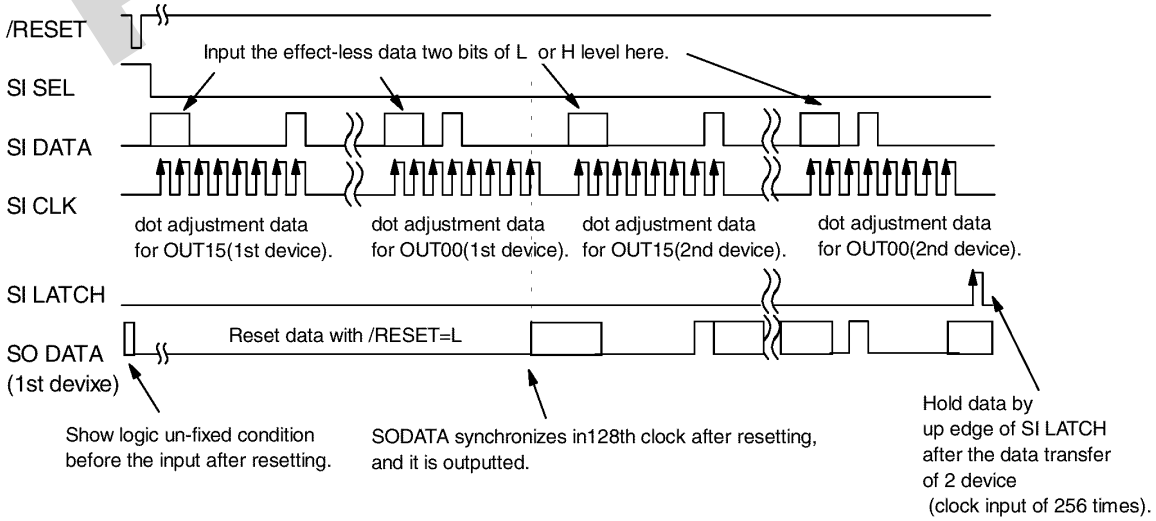


Figure 2-2 : serial data transfer timing figure
(dot adjustment, the case of SI SEL=L, for example of cascade connected of 2 devices.)



Operating explanation and truth value table (3/12 pages)

DAC1 Set details of standard current adjustment DAC1 (about data SIREG1[7 : 6])

/RESET	SI SEL	SI REG [7:6]	SI REG [5:0]	Current Rate	Operation and function	Notes
H	H	HH	XXXXXX	100[%]	It is based on the current value set with REXT, and set in 100 %.	When SI SEL= H is chosen, MSB sides 2 bits are equivalent to set of standard current adjustment DAC1. Output current is set in 4 step.
H	H	HL	XXXXXX	75[%]	It is set in the same way in 75 %.	
H	H	LH	XXXXXX	50[%]	It is set in the same way in 50 %.	
H	H	LL	XXXXXX	25[%]	It is set in the same way in 25 %.	
⌐‾‾‾	X	LL	LLLLLL	25[%]	Early condition after resetting is set by 25 %.	

DAC2 Set details of standard current adjustment DAC2 (about data SIREG1[5 : 0])

/RESET	SI SEL	SI REG [7:6]	SI REG [5:0]	Current Rate	Operation and function	Notes
H	H	XX	HHHHHH	100[%]	It is based on the current value set with DAC1, and set in 100 %.	When SI SEL= H is chosen, LSB sides 6 bits are equivalent to set of standard current adjustment DAC2. Output current is set in 64 step.
H	H	XX	HHHHHL to LLLLLH	99.0[%] to 40.9[%]	Set 64 steps is possible from the current range 100 to 40%. (1LSB=0.95 %)	
H	H	XX	LLLLLL	40[%]	It is set in the same way in 40 %.	
⌐‾‾‾	X	LL	LLLLLL	40 [%]	Early condition after resetting is set by 40 %.	

Operating explanation and truth value table (4/12 pages)

The polarity of the input serial data of
standard current adjustment(SI REG1[7:0]) and dot adjustment(SI REG2[127:0])

Figure 3-1 : the case of serial data transfer timing figure
(SI SEL=H, select data input of standard current adjustment for DAC1 and DAC2)

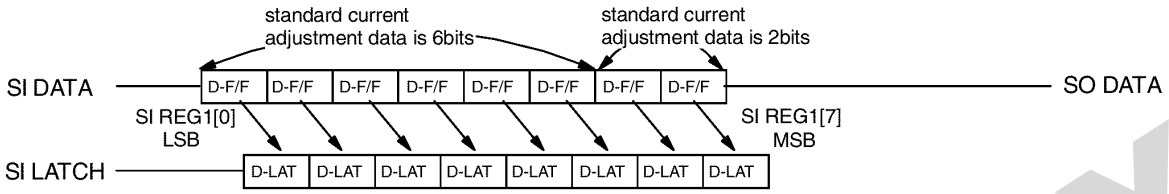
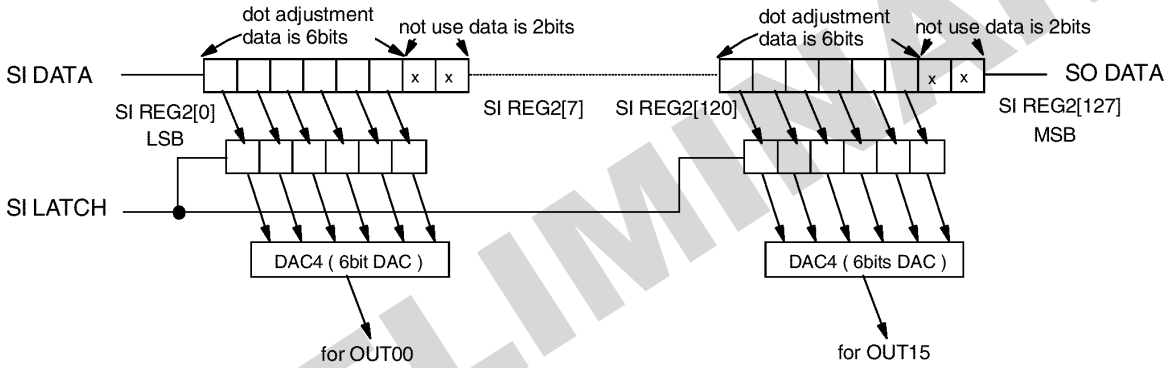


Figure 3-2 : the case of serial data transfer timing figure
(SI SEL=L, select data input of dot adjustment for DAC4.)



DAC4 Set details of dot adjustment DAC4 (about data SIREG2[127 : 0])

/RESET	SISEL	DCEN	About 8bits unit of SIREG2[127:0]	Current Rate	Operation and function	Notes
H	L	H	XXHHHHHH	100[%]	It is based on the current value set with DAC1 to DAC3 and set in 100 %.	When SISEL= "L" is chosen, 8 bits out of 128 bits are equivalent to set of each output, and the LSB sides 6 bits of 8 bits are data on dot adjustment. Output current is set in 64 step. SIREG2[7:0] -> adjustment data of OUT00. SIREG2[15:8] -> adjustment data of OUT01. SIREG2[127:120] -> adjustment data of OUT15.
H	L	H	XXHHHHHL to XXLLLLLH	98.7[%] to 21.3[%]	Set 64 steps is possible from the current range 100 to 20%. (1LSB=1.27 %)	
H	L	H	XXLLLLLL	20[%]	It is set in the same way in 20 %.	
⌝⌞	X	H	XXLLLLLL	20[%]	Early condition after resetting is set by 20 %.	
H	X	L	XXHHHHHH	100[%]	It is set in the same way in 100 %.	Input of data is possible in the case of the DCEN=L level as well. Adjustment is done when it is made DCEN=H level.

Operating explanation and truth value table (5/12 pages)

Pararell data transfer : all bit adjustment DAC3.

(about the data register PI REG1[7 : 0])

	PI DATA [7:0]	PI CLK	PI LATCH	PI SEL	PO DATA [7:0]	Operation and function
1	H or L	(1time)	L	H	H or L	Choose the input data of all bit adjustment (8bit, 5bit and 2bit) with PI SEL=H. Transfer data to PI REG1 by up edge 1 time input of PI CLK.
2		L	(1time)	H	No change	Hold the data transferred to PI REG1 by up edge of PI LATCH. Set is reflected on all bit adjustment from the moment when it is held.

Figure 4-1 : pararell data transfer timing figure

(all bit adjustment, the case of PI SEL= H, for example of 1 device.)

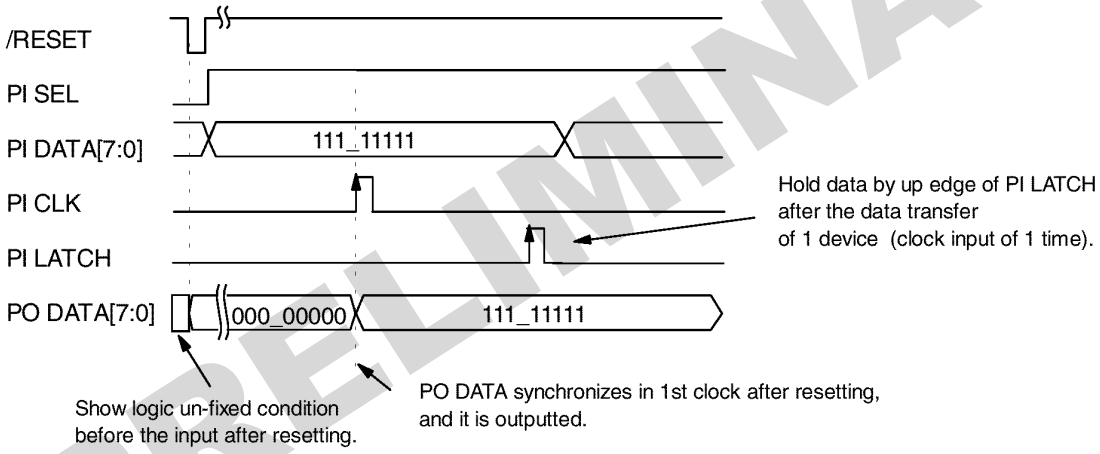
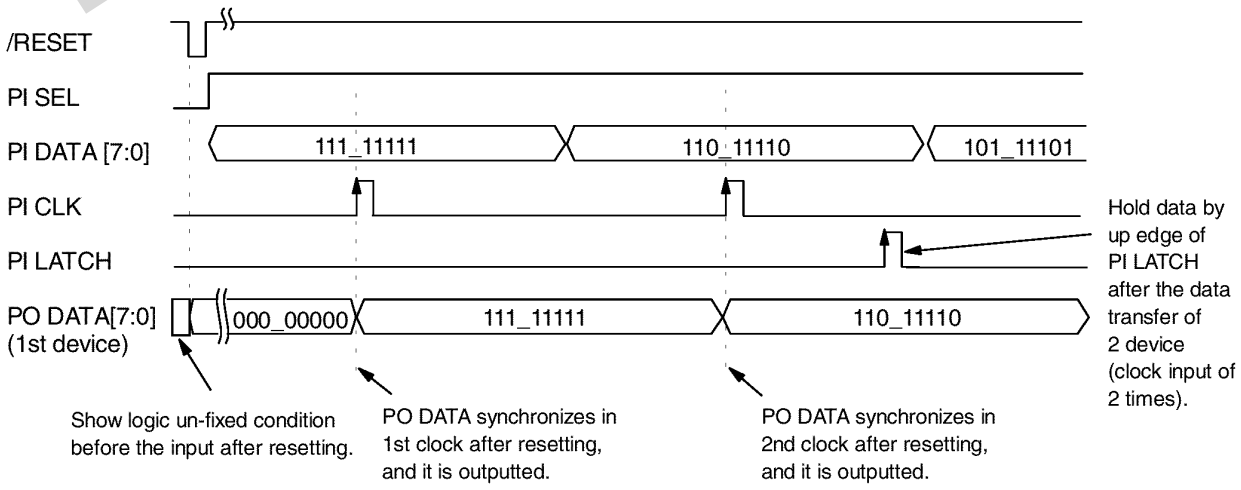


Figure 4-2 : pararell data transfer timing figure

(all bit adjustment, the case of PI SEL=H, for example of cascade connected of 2 devices.)



Operating explanation and truth value table (6/12 pages)

Pararell data transfer : PMW 256 Gray Scale.
(about the data register PI REG2[127:0])

	PI DATA [7:0]	PI CLK	PI LATCH	PI SEL	PO DATA [7:0]	Operation and function
1	H or L	↑ (16times)	L	L	H or L	Choose the input data of PWM 256 Gray scale (8bit X 16) with PI SEL=L. Transfer data to PI REG2 by up edge 16 times input of PI CLK.
2		L	↑ (1time)	L	No change	Hold the data transferred to PI REG2 by up edge of PI LATCH. Set is reflected on PWM 256 Gray scale from the next BLANK=L when it is held.

Figure 5-1 : pararell data transfer timing figure
(PWM 256 Gray scale, the case of PI SEL= L, for example of 1 device.)

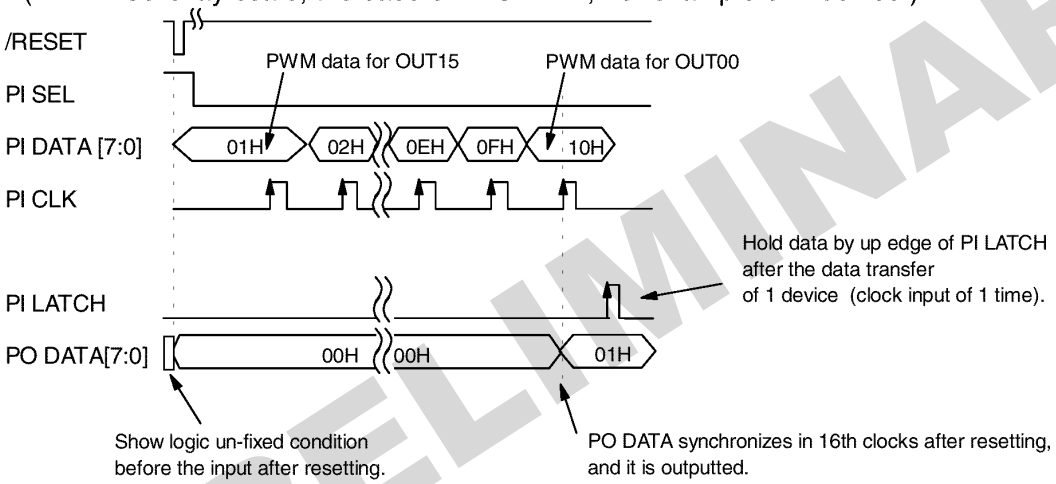
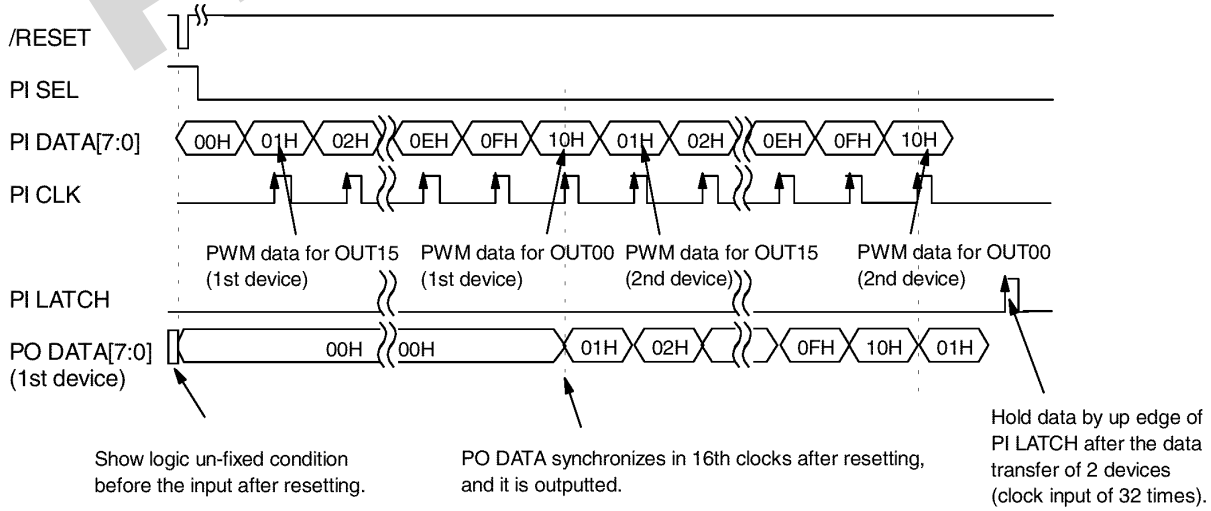


Figure 5-2 : pararell data transfer timing figure
(PWM 256 Gray scale, the case of PI SEL= L, for example of cascade connected of 2 devices.)



Operating explanation and truth value table (7/12 pages)

Set details of all bit adjustment by PWMCLK dividing. (about data PIREG1[7 : 5])

/RESET	PI SEL	BC EN	PI REG1 [7:5]	PWMCLK dividing rate	Operation and function	Notes
H	H	H	LLL	PWMCLK =8/8PWMCLK	The time width of 1 cycle of PWMCLK becomes the amount of change in pulse width of the PWM data 1LSB.	When PI SEL= H is chosen, MSB sides 3 bits are equivalent to set of all bit adjustment by PWMCLK dividing. PIREG1[7:5] varies the minimum pulse width of the PWM pulse output in 8 step. This set influences all output.
H	H	H	LLH to HHL	7/8PWMCLK to 2/8PWMCLK	Variable does the frequency of PWMCLK to 1/8 of the minima. It is set in 8 step.	
H	H	H	HHH	PWM CLK =1/8PWMCLK [Hz]	The time width of 8 cycle of PWMCLK becomes the amount of change in pulse width of the PWM data 1LSB.	
⊓	X	H	LLL	PWM CLK =8/8PWM CLK[Hz]	The time width of 1 cycle of PWMCLK becomes the amount of change in pulse width of the PWM data 1LSB.	
H	H	L	XXX	It doesn't influence it.	It doesn't influence it.	Input of data is possible in the case of the BCEN=L level as well. Adjustment is done when it is made BCEN=H level.

DAC3 Set details of all bit adjustment DAC3 (about data PI REG2[4 : 0])

/RESET	PI SEL	PI REG1 [4:0]	BC EN	Current Rate	Operation and function	Notes
H	H	HHHHH	H	100[%]	It is based on the current value set with DAC1 to DAC2 and set in 100 %.	When PI SEL= "H" is chosen, LSB side 5 bits are equivalent to set of all bit adjustment, Output current is set in 32 step.
H	H	HHHHL to LLLLH	H	98.3[%] to 51.6[%]	Set 32 steps is possible from the current range 100 to 50%. (1LSB=1.61 %)	
H	H	LLLLL	H	50[%]	It is set in the same way in 50 %.	
⊓	X	HHHHH	H	100 [%]	Early condition after resetting is set by 100 %.	
H	X	HHHHH	L	100 [%]	It is set in the same way in 100 %.	Input of data is possible in the case of the BCEN=L level as well. Adjustment is done when it is made BCEN=H level.

Operating explanation and truth value table (8/12 pages)

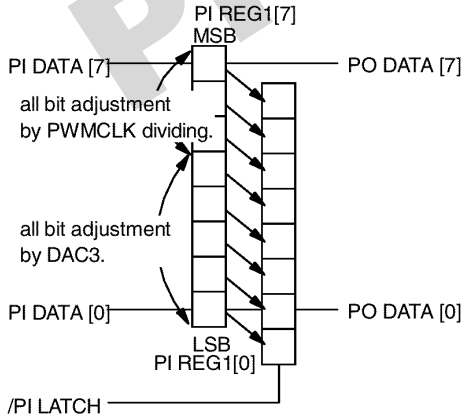
Set details of all PWM 256 Gray scale (about data PI REG2 [127:0], 8bit X 16)

/RESET	PI SEL	1words(8bit) of PI REG2	Outpiut Pulse Rate	Operation and function	Notes
H	L	HHHHHHHH	255/255	Output pulse width is muximum value when input data are "FF".	PISEL= "L" is chosen, and PWM gray scale controls output pulse width. Transfer 1 word (eight bits) X 16 word as pararell data. 1 word is the PWM data of each Output pulse width is set in 256 step. PI REG2[7:0] -> PWM data of OUT00. PIREG2[15:8] -> PWM data of OUT01. PIREG2[127:120] -> PWM data of OUT15. Output minimum pulse width is 1/PWMCLK.
H	L	HHHHHHHL to LLLLLLLH	254/255 to 1/255	The PWM pulse control of 1 - 255 gray scale is possible by the input data.	
H	L	LLLLLLLL	0/255	It is output off when input data are "00".	
⌐¯	X	LLLLLLLL	0/255	Early condition after the reset signal input is set in 0/255 (output off).	

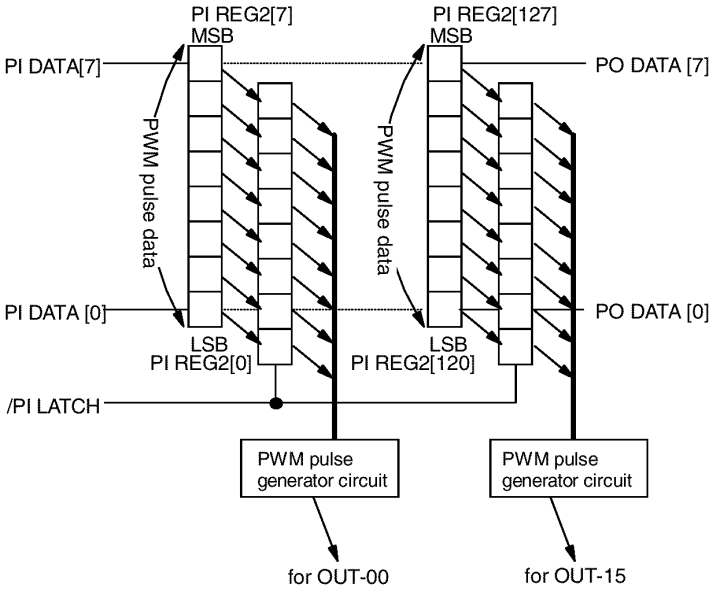
The polarity of the input serial data of all bit adjustment(PI REG1[7:0]) and PWM256Gray sclae (PI REG2[127:0])

Figure 6-1 : the case of Pararell data transfer timing figure

(PI SEL=H, select data input of all bit adjustment for DAC3)



(PI SEL=L, select data input of PWM256 Gray scale)



Operating explanation and truth value table (9/12 pages)

Reference table : output current set value (1)

	DAC1	(2 bit)		DAC2	(6 bit)		DAC3	(5bit)		DAC4	(6bit)
No	Input Data	Current rate1	No	Input Data	Current rate2	No	Input Data	Current rate3	No	Input Data	Current rate4
3	11	1.00	63	111111	1.000	31	**11111	**1.000	63	111111	63
2	10	0.75	62	111110	0.990	30	11110	0.984	62	111110	62
1	01	0.50	61	111101	0.981	29	11101	0.968	61	111101	61
0	**00	**0.25	60	111100	0.971	28	11100	0.952	60	111100	60
			59	111011	0.962	27	11011	0.936	59	111011	59
			58	111010	0.952	26	11010	0.919	58	111010	58
			57	111001	0.943	25	11001	0.903	57	111001	57
			56	111000	0.933	24	11000	0.887	56	111000	56
			55	110111	0.924	23	10111	0.871	55	110111	55
			54	110110	0.914	22	10110	0.855	54	110110	54
			53	110101	0.905	21	10101	0.839	53	110101	53
			52	110100	0.895	20	10100	0.823	52	110100	52
			51	110011	0.886	19	10011	0.807	51	110011	51
			50	110010	0.876	18	10010	0.790	50	110010	50
			49	110001	0.867	17	10001	0.774	49	110001	49
			48	110000	0.857	16	10000	0.758	48	110000	48
			47	101111	0.848	15	01111	0.742	47	101111	47
			46	101110	0.838	14	01110	0.726	46	101110	46
			45	101101	0.829	13	01101	0.710	45	101101	45
			44	101100	0.819	12	01100	0.694	44	101100	44
			43	101011	0.820	11	01011	0.677	43	101011	43
			42	101010	0.800	10	01010	0.661	42	101010	42
			41	101001	0.791	9	01001	0.645	41	101001	41
			40	101000	0.781	8	01000	0.629	40	101000	40
			39	100111	0.771	7	00111	0.613	39	100111	39
			38	100110	0.762	6	00110	0.597	38	100110	38
			37	100101	0.752	5	00101	0.581	37	100101	37
			36	100100	0.743	4	00100	0.565	36	100100	36
			35	100011	0.733	3	00011	0.549	35	100011	35
			34	100010	0.724	2	00010	0.532	34	100010	34
			33	100001	0.714	1	00001	0.516	33	100001	33
			32	100000	0.705	0	00000	0.500	32	100000	32
			31	011111	0.695				31	011111	31
			30	011110	0.686				30	011110	30
			29	011101	0.676				29	011101	29
			28	011100	0.667				28	011100	28
			27	011011	0.657				27	011011	27
			26	011010	0.648				26	011010	26
			25	011001	0.638				25	011001	25
			24	011000	0.629				24	011000	24
			23	010111	0.619				23	010111	23
			22	010110	0.610				22	010110	22
			21	010101	0.600				21	010101	21
			20	010100	0.591				20	010100	20
			19	010011	0.581				19	010011	19
			18	010010	0.571				18	010010	18
			17	010001	0.562				17	010001	17
			16	010000	0.552				16	010000	16
			15	001111	0.543				15	001111	15
			14	001110	0.533				14	001110	14
			13	001101	0.524				13	001101	13
			12	001100	0.514				12	001100	12
			11	001011	0.505				11	001011	11
			10	001010	0.495				10	001010	10
			9	001001	0.486				9	001001	9
			8	001000	0.476				8	001000	8
			7	000111	0.467				7	000111	7
			6	000110	0.457				6	000110	6
			5	000101	0.448				5	000101	5
			4	000100	0.438				4	000100	4
			3	000011	0.429				3	000011	3
			2	000010	0.419				2	000010	2
			1	000001	0.410				1	000001	1
			0	**000000	**0.4				0	**000000	**0

The formula of set resistance :This value is theory value. Actual current value contains error and so on in this value.
REXT [k ohms] =
(1.9 X Current Rate1 X Current Rate2 X Current Rate3 / Output Current [mA]) X (1+(7 X Current Rate4/105)) X19.4
And, ** mark is after the initialization value of the resetting (/RESET=L) .

Operating explanation and truth value table (10/12 pages)

Reference table : output current set value (2)

**The reference value of the standard current adjustment under a some condition.
(REXT=2.7 kohms fixation surface brightness adjustment =MSB dot adjustment =MSB)

Unit : mA

	DAC2															
DAC1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	7.1	7.3	7.4	7.6	7.8	7.9	8.1	8.3	8.5	8.6	8.8	9.0	9.1	9.3	9.5	9.6
1	14.2	14.5	14.9	15.2	15.6	15.9	16.2	16.6	16.9	17.2	17.6	17.9	18.3	18.6	18.9	19.3
2	21.3	21.8	22.3	22.8	23.3	23.8	24.3	24.9	25.4	25.9	26.4	26.9	27.4	27.9	28.4	28.9
3	28.4	29.1	29.6	30.4	31.1	31.8	32.5	33.1	33.8	34.5	35.2	35.8	36.5	37.2	37.9	38.6

	DAC2															
DAC1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	9.8	10.0	10.1	10.3	10.5	10.7	10.8	11.0	11.2	11.3	11.5	11.7	11.8	12.0	12.2	12.3
1	19.6	19.9	20.3	20.6	21.0	21.3	21.6	22.0	22.3	22.7	23.0	23.3	23.7	24.0	24.3	24.7
2	29.4	29.9	30.4	30.9	31.4	32.0	32.5	33.0	33.5	34.0	34.5	35.0	35.5	36.0	36.5	37.0
3	39.2	39.9	40.6	41.2	41.9	42.6	43.3	44.0	44.6	45.3	46.0	46.7	47.3	48.0	48.7	49.4

	DAC2															
DAC1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
0	12.5	12.7	12.9	13.0	13.2	13.4	13.5	13.7	13.9	14.0	14.2	14.4	14.5	14.7	14.9	15.0
1	25.0	25.4	25.7	26.0	26.4	26.7	27.0	27.4	27.7	28.1	28.4	28.7	29.1	29.4	29.8	30.1
2	37.5	38.0	38.6	39.0	39.6	40.1	40.6	41.1	41.6	42.1	42.6	43.1	43.6	44.1	44.6	45.1
3	50.0	50.7	51.4	52.1	52.7	53.4	54.1	54.8	55.4	56.1	56.8	57.5	58.1	58.8	59.5	60.2

	DAC2															
DAC1	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
0	15.2	15.4	15.6	15.7	15.9	16.1	16.2	16.4	16.6	16.7	16.9	17.1	17.2	17.4	17.6	17.8
1	30.4	30.8	31.1	31.4	31.8	32.1	32.5	32.8	33.1	33.5	33.8	34.1	34.5	34.8	35.2	35.5
2	45.6	46.1	46.7	47.2	47.7	48.2	48.7	49.2	49.7	50.2	50.7	51.2	51.7	52.2	52.7	53.2
3	60.9	61.5	62.2	62.9	63.6	64.2	64.9	65.6	66.3	66.9	67.6	68.3	69.0	69.6	70.3	71.0

Operating explanation and truth value table (11/12 pages)

Temperature detection function (It can be monitored with the ALARM1 terminal.)
Do two-step temperature detection as mentioned in the bottom table. (TSD1/TSD2)

Juction Temperature [degC]	ALARM1	OUT00 to 15	Function
-40 to 120	Off	Normal Operation	
Over 120	On	Normal Operation	On (L level) does ALARM1 terminal when chip temperature reaches the following range (TSD1). It doesn't influence other functions.
Over 140	On	Off	When chip temperature reaches the following range (TSD2), on (L level) does ALARM1 terminal, and output terminal offs. Do a release of this output off with the input of up edge of the TSENA terminal or the /RESET terminal =L. At this time, inside data aren't reset. All inside data are reset in the case of the /RESET terminal =L, too.

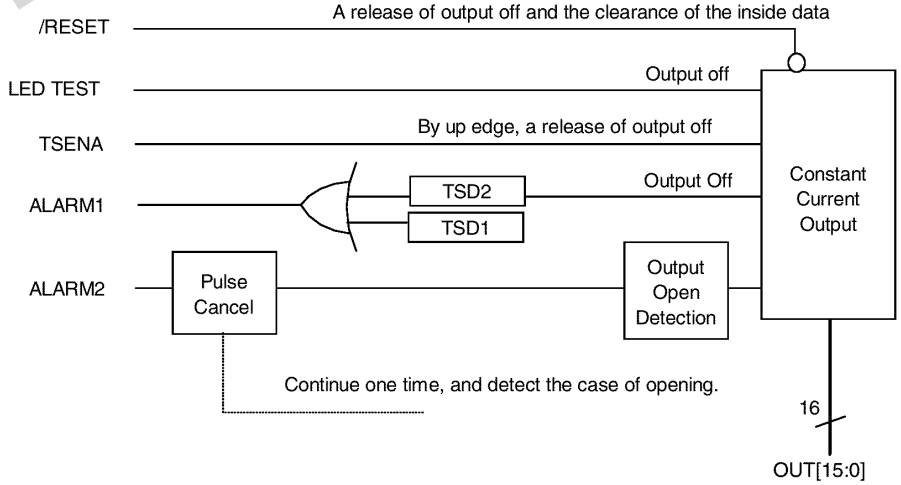
Output open detection function (It can be monitored with the ALARM2 terminal.).
Do output open detection as mentioned in the bottom table.

Output Voltage [V]	ALARM2	Function
>=VDD X 0.04	Off	
=<VDD X 0.04	On	Output opening is detected by the following voltage, and on (L level) does ALARM2 terminal. (Or, when output voltage almost became a GND voltage for some reasons.)

Pulse cancellation circuit (When it is monitored from the output open detection ALARM2 terminal.)

PWMCLK	ALARM2	Function
Input	Operating	Open detection detects the case that output continues the fixed time and opens.
No Input	Always Off	Pulse cancellation circuit is built in to ignore moment detection by the switching noise of the output and so on. ALARM2 output doesn't do on (L level) when PWMCLK isn't inputted because PWMCLK is being used.

The block diagram of the protection circuit



Operating explanation and truth value table (12/12 pages)

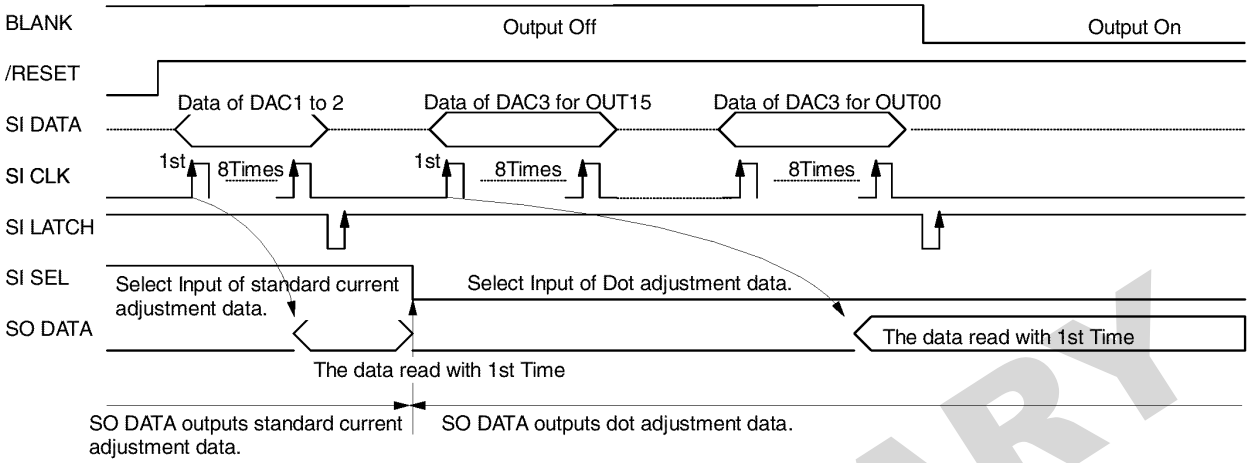
Look it over about the protection circuit function.

Operating chart (about TESNA terminal and ALARM1 and output terminal OUT00 to 15)

TS ENA	/RESET	Juction Temperature Unit:degC			ALARM1	OUT 00 to 15	Function
		Tj <= 120	TSD1 Tj <= 120	TSD2 Tj <= 140			
X	L	○	-	-	Off	On	Condition of device resetting
X	H	○	-	-	Off	On	Output is usually operating.
X	L	-	○	-	On	On	Condition of device resetting
X	H	-	○	-	On	Normal Operation	ALARM1 shows L level, and warns of rise in temperature. Output is usually operating.
X	L	-	-	○	On	Off	Even if resetting is inputted, when Juction temperature is high, output off
X	H	-	-	○	On	Off	ALARM1 shows L level, and warns of rise in temperature. Output is usually operating.

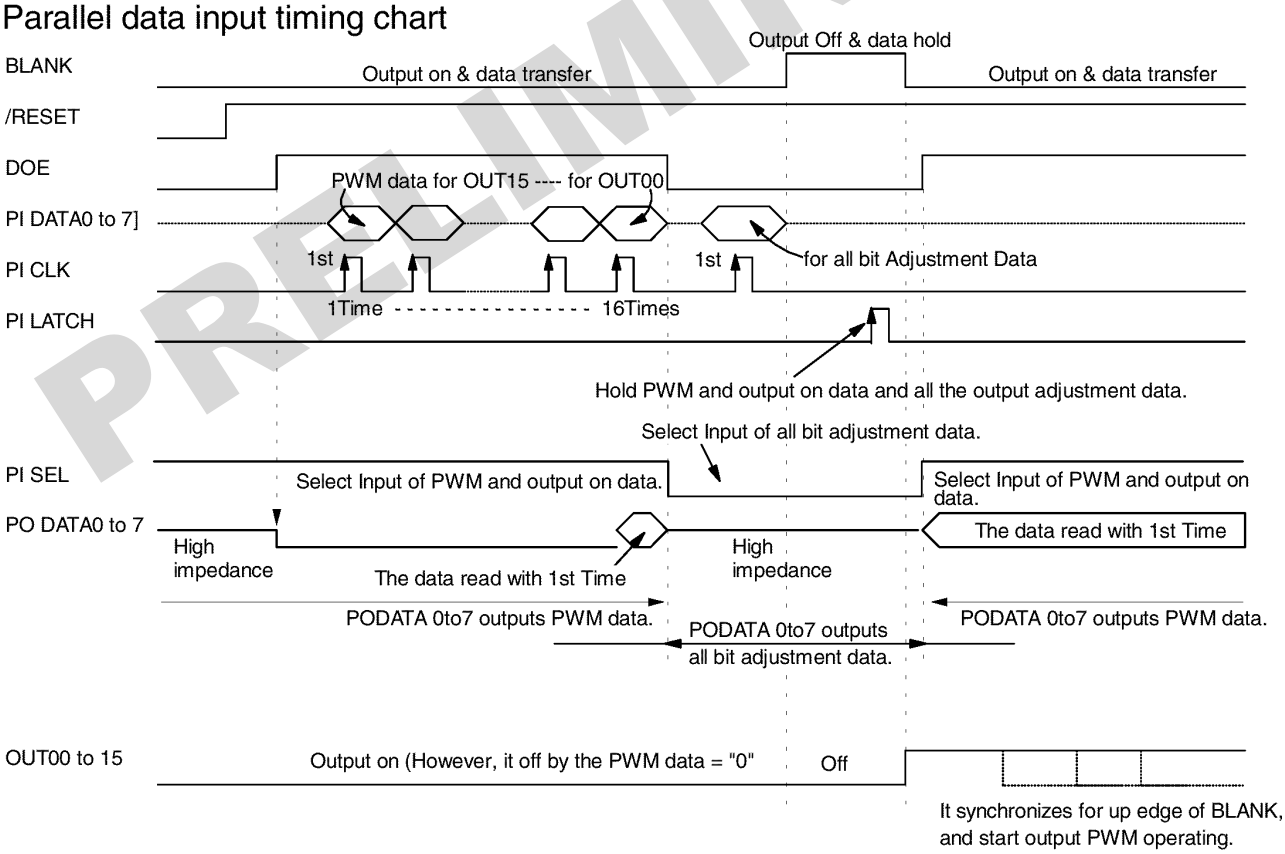
Note : Inside TSD circuit moves regardless of the input voltage of the TSENA terminal and the input voltage of the /RESET terminal.

Serial data input timing chart



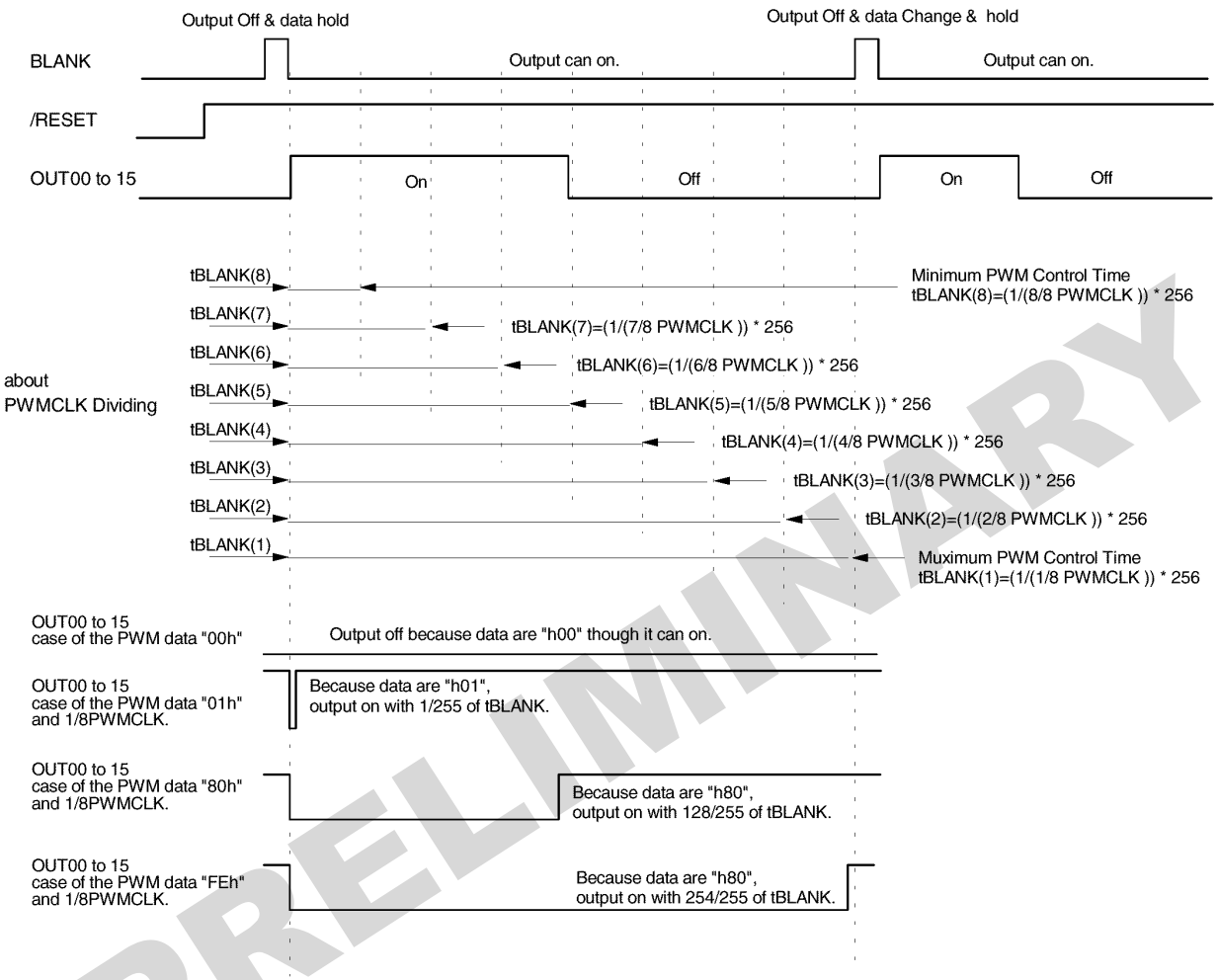
Complement : There are no relations in output on off, and the input of the serial data can be inputted.
The moment it is held by SI LATCH signal, serial data influences output current value, output pulse width.

Parallel data input timing chart



Complement : There are no relations in the BLANK signal, and pararell data transfer can be inputted.
Control PWM pulse by the BLANK signal. Recommend what is done after data transfer is made BLANK=H and made output off.

PWM operating timing chart and all bit adjustment by PWMCLK dividing.

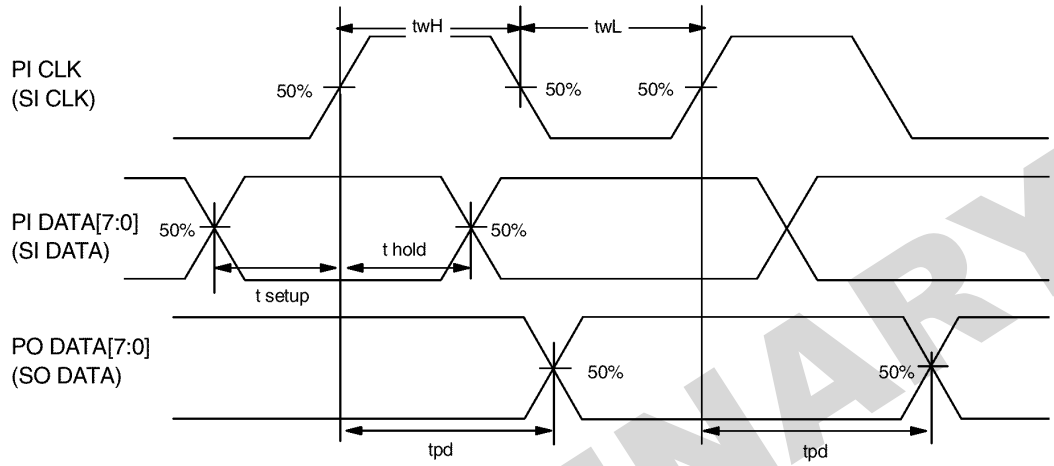


PWM Operaring Timing :
Output terminal starts PWM pulse output when BLANK signal is made L level from the H level.
(It is simultaneous with 16 output as well.)
Output output pulse only once toward BLANK signal's changing once in L from H.
Therefore, when the same PWM data again are used, must make BLANK signal L level again from the H level.

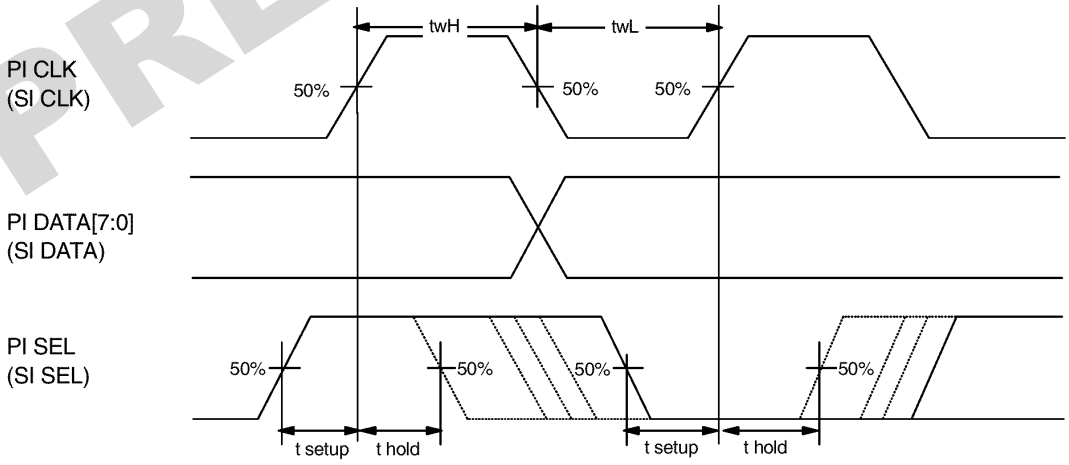
PWMCLK Dividing :
See the center of the upper figure. Brightness of the LED module can be changed to eight steps by divide of PWMCLK without adjusting current value.
As for brightness adjustment in the big range, recommend using divide of PWMCLK.

Logic input and output timing wave form (1)

1.PI CLK(SI CLK) vs PI DATA0 to 7 (SI DATA)
PI CLK(SI CLK) vs PO DATA0 to 7 (SO DATA)

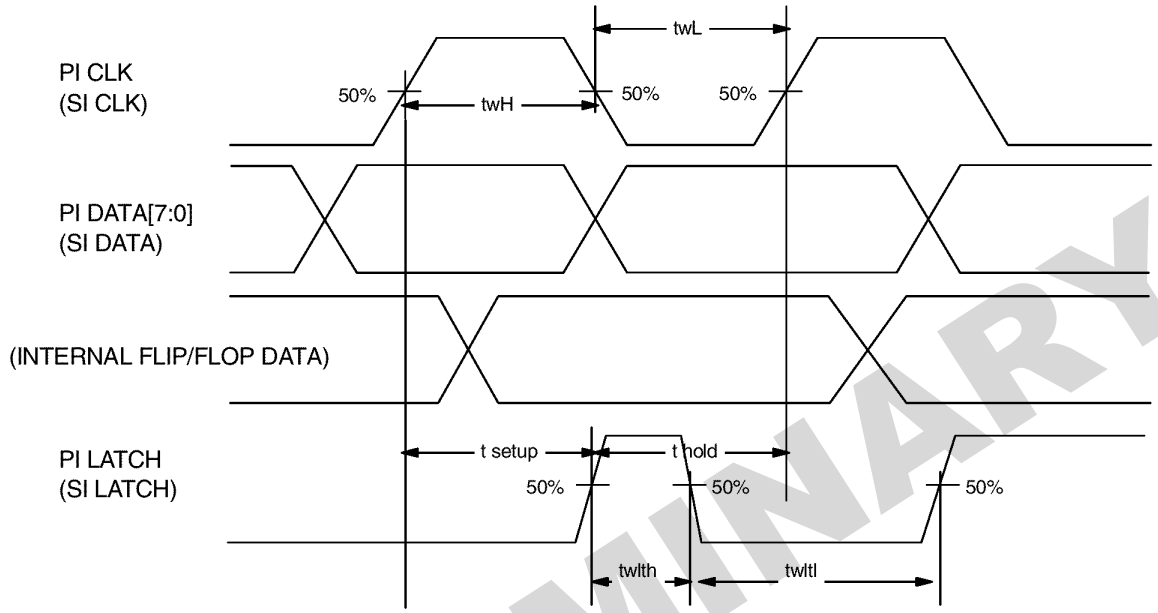


2. PI SEL(SI SEL) vs PI CLK(SI CLK)

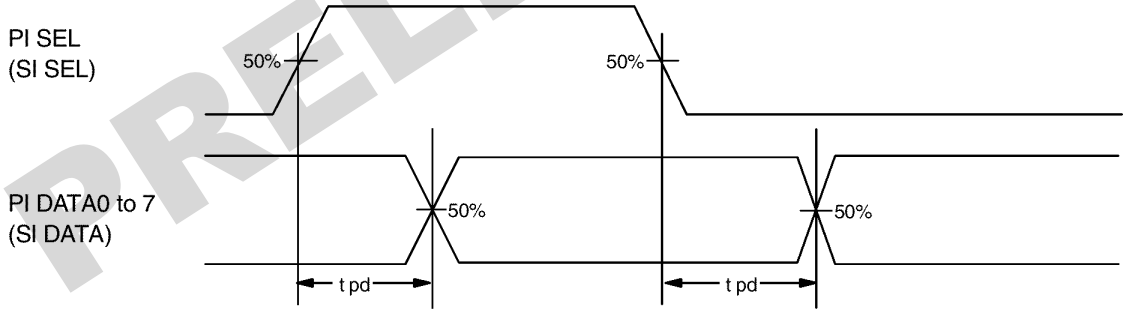


Logic input and output timing wave form (2)

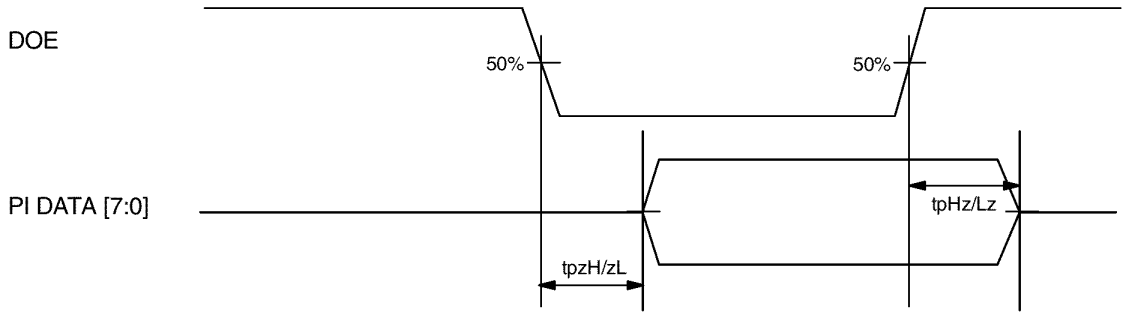
3. PI LATCH(SI LATCH) vs PI CLK(SI CLK)



4. PI SEL(SI SEL) vs PO DATA0 to 7 (SO DATA)

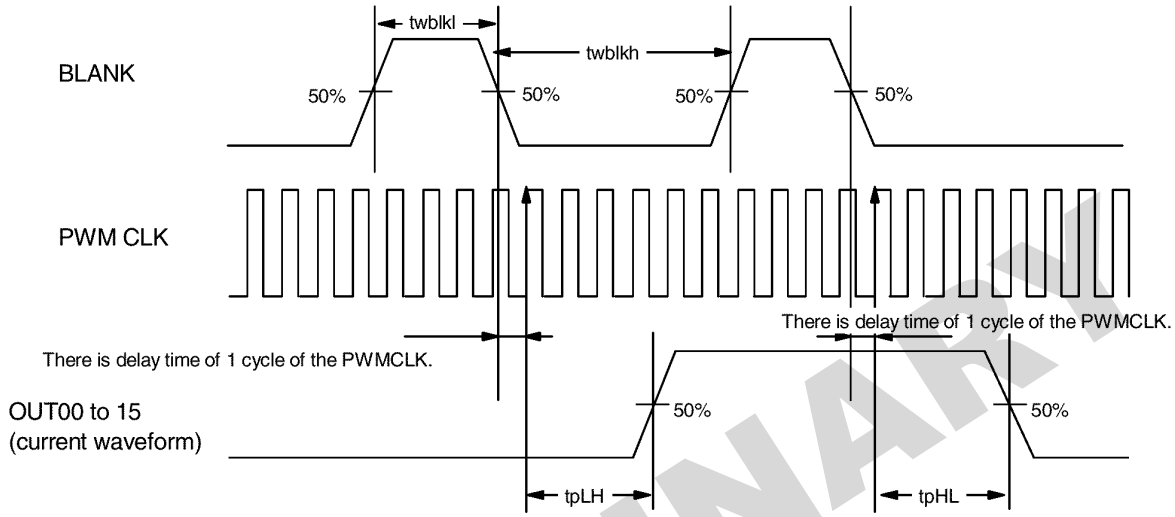


5. DOE vs PO DATA0 to 7

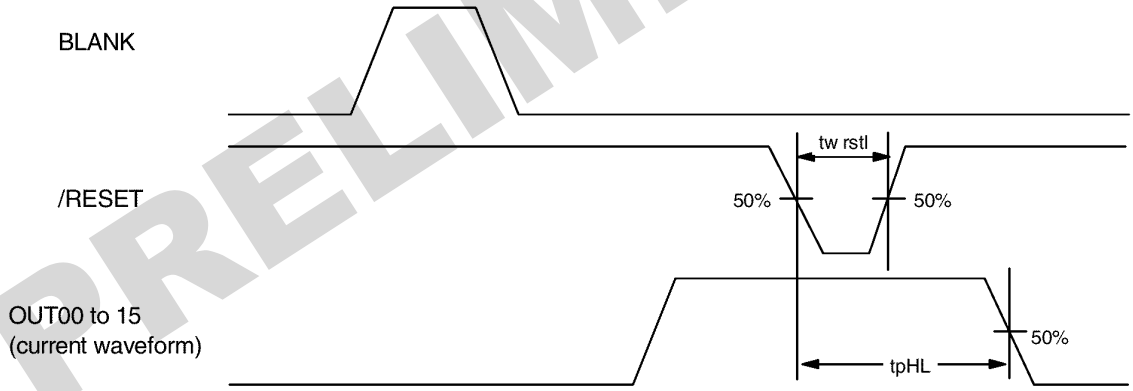


Logic input and Constant Current Output timing wave form

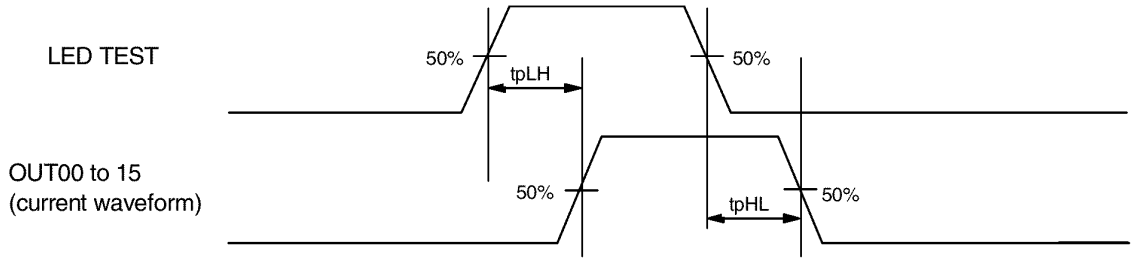
6. BLANK vs OUT00 to 15 with PWM CLK



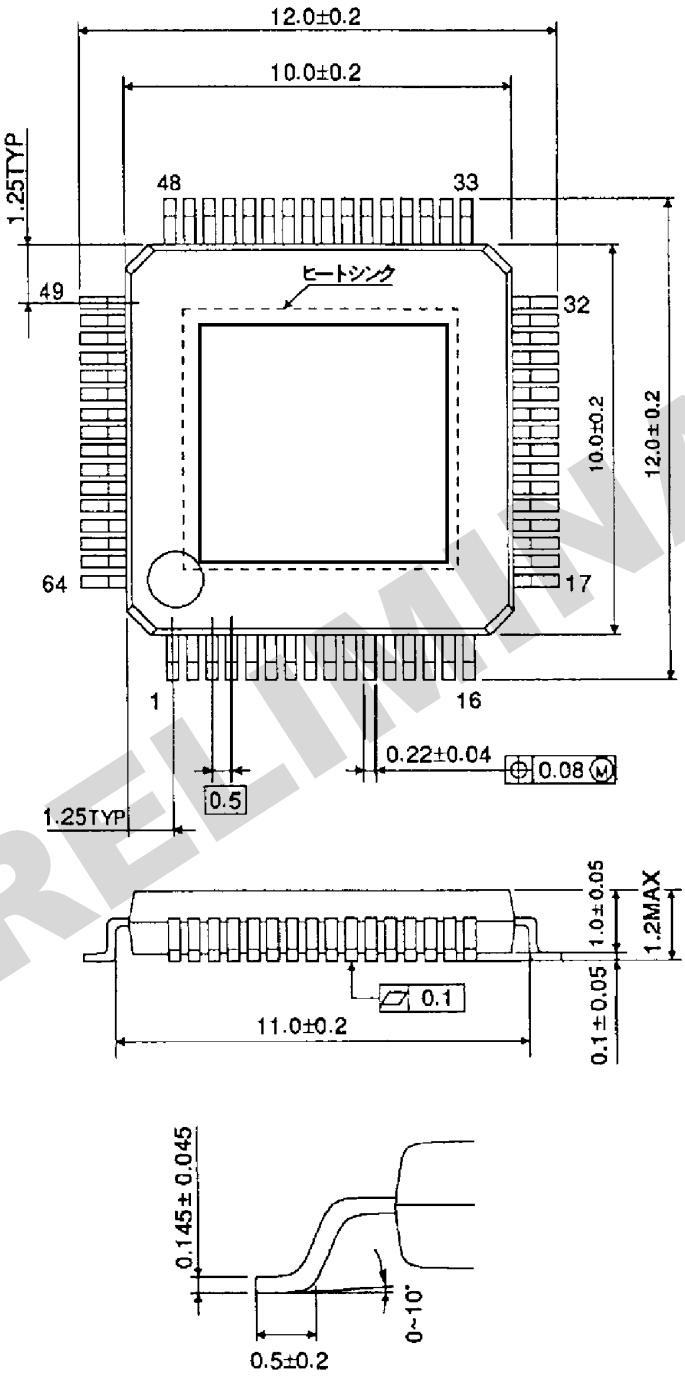
7. /RESET vs OUT00 to 15



8. LED TEST vs OUT00 to 15



HQFP64-P-1010-0.50 Unit : mm



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