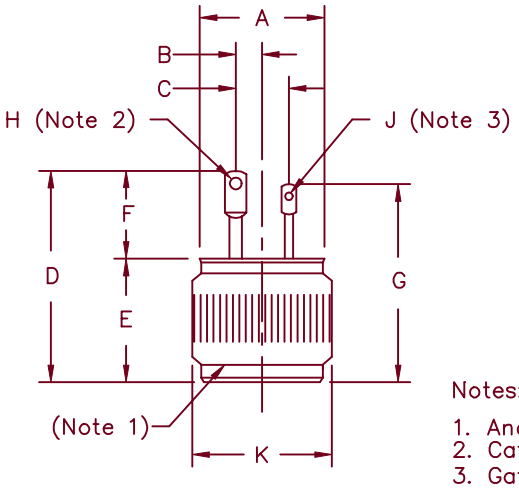
Silicon Controlled Rectifier
Series 023



Notes:
1. Anode connected to case
2. Cathode terminal
3. Gate terminal

Dim.	Inches		Millimeters		
	Min.	Max.	Min.	Max.	Notes
A	0.495	0.505	12.57	12.83	
B	0.068	0.080	1.73	2.03	
C	0.150	0.160	3.81	4.06	
D	0.705	0.754	17.91	19.15	
E	0.350	0.374	8.89	9.50	
F	0.345	0.380	8.76	9.65	
G	0.600	0.714	15.24	18.14	
H	0.070	0.087	1.78	2.21	Dia.
J	0.050	0.065	1.27	1.65	Dia.
K	0.503	0.508	12.83	13.08	Dia.

Microsemi Catalog Number	Forward & Reverse Repetitive Blocking	Reverse Transient Blocking
0230200L	200V	200V
0230300L	300V	300V
0230400L	400V	400V
0230500L	500V	500V
0230600L	600V	600V

- dv/dt – 200V/µS
- 300 Amperes surge current
- Low forward on–state voltage
- Economical for medium power applications
- V_{DRM}/ V_{RRM} 200V to 600V

Electrical Characteristics

Max average on–state current	$I_{T(AV)}$ 23 Amps	T_C = 68°C sine wave, $R_{\theta JC}$ = 1.65°C/W
Max peak on–state voltage	V_{FM} 1.8 Volts	I_T = 100A: T_J = 25°C
Max holding current	I_H 80 mA	
Max peak one cycle surge current	I_{TSM} 300 A	T_J = 125°C, 8.3mS pulse
Max I^2t capability for fusing	I^2t 370 A^2s	t = 8.3mS

Thermal and Mechanical Characteristics

Storage temp range	T_{STG}	–55°C to 125°C
Operating junction temp range	T_J	–55°C to 125°C
Max thermal resistance	$R_{\theta JC}$	1.65°C/W junction to case
Typical thermal resistance	$R_{\theta CS}$	1.0°C/W case to sink
Weight		0.255 ounces (7.23 grams) typical

8–28–00 Rev. 2

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Switching

Critical rate of rise of on-state current (note 1)	di/dt	100A/usec.	T_J = 125°C
Typical delay time (note 1)	t_d	0.5 usec.	
Typical rise time (note 1)	t_r	3.0 usec.	
Typical turn-on time	t_o	3.5 usec.	
Typical circuit commuted turn-off time (note 2)	t_q	50 usec.	T_J = 125°C

Note 1: I_{TM} = 20A, V_D = V_{DRM}. V_{GT} = 12V open circuit, 20 ohm-0.1 usec. rise time
Note 2: I_{TM} = 20A, di/dt = 5A/usec., V_R = 50V, dv/dt = 20V/usec., Rated V_{DRM}

Triggering

Max. gate trigger voltage	V_{GT}	2.0V	
Max. nontriggering gate voltage	V_{GD}	0.25V	T_J = 125°C
Max. gate trigger current	I_{GT}	40mA	
Max. peak gate power	P_{GM}	5.0W	
Average gate power	$P_{G(AV)}$	0.5W	
Max. peak gate current	I_{GM}	3.0A	
Max. peak gate voltage (forward)	V_{GM}	10.0V	
Max. peak gate voltage (reverse)	V_{GM}	5.0V	

Blocking

Max. forward leakage current	I_{DRM}	10uA	V_{DRM}, T_J =25° C
Max. reverse leakage current	I_{RRM}	10uA	V_{RRM}, T_J =25° C
Max. forward leakage current	I_{DRM}	3.0mA	V_{DRM}, T_J =125° C
Max. reverse leakage current	I_{RRM}	3.0mA	V_{RRM}, T_J =125° C
Critical rate of rise of off-state voltage	dv/dt	200V/usec.	T_J =125° C

HEAT SINK MOUNTING

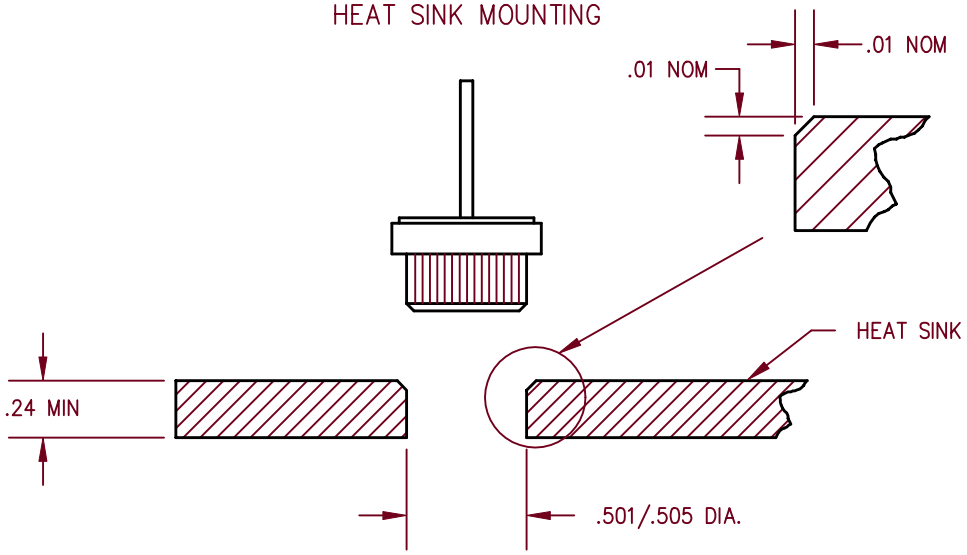

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Figure 1
Typical Forward Characteristics

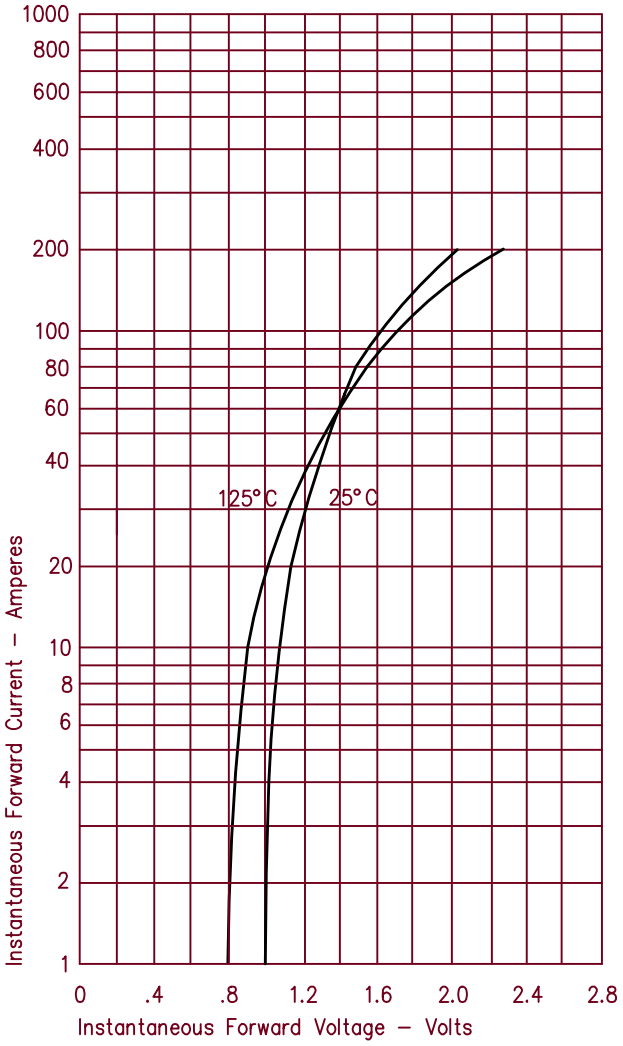

Figure 2
Forward Current Derating

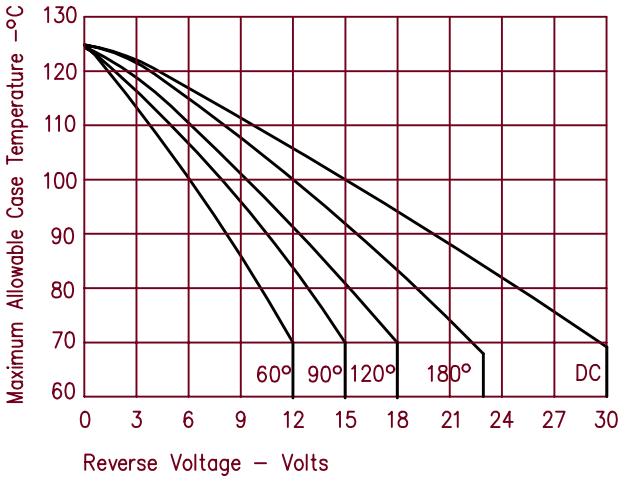

Figure 3
Maximum Forward Power Dissipation