

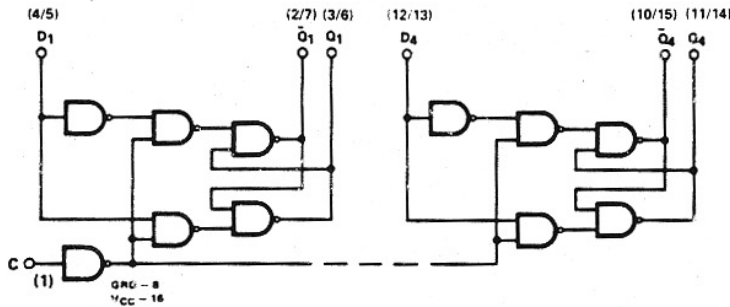
**Features**

- IDEAL FOR STORAGE APPLICATIONS
- COMPLEMENTARY DATA OUTPUTS
- COMMON CLOCK FOR SYNCHRONOUS OPERATION
- CLOCK ACTS AS ENABLE CONTROL WITH 1 UL
- PULLUP RESISTORS ON CHIP

**General Description**

The 370 contains four clocked D-type flip-flops with a common clock input acting as an enable line. Each stage has complementary outputs with passive pullup. Applications include quad latches and registers with parallel inputs and outputs.

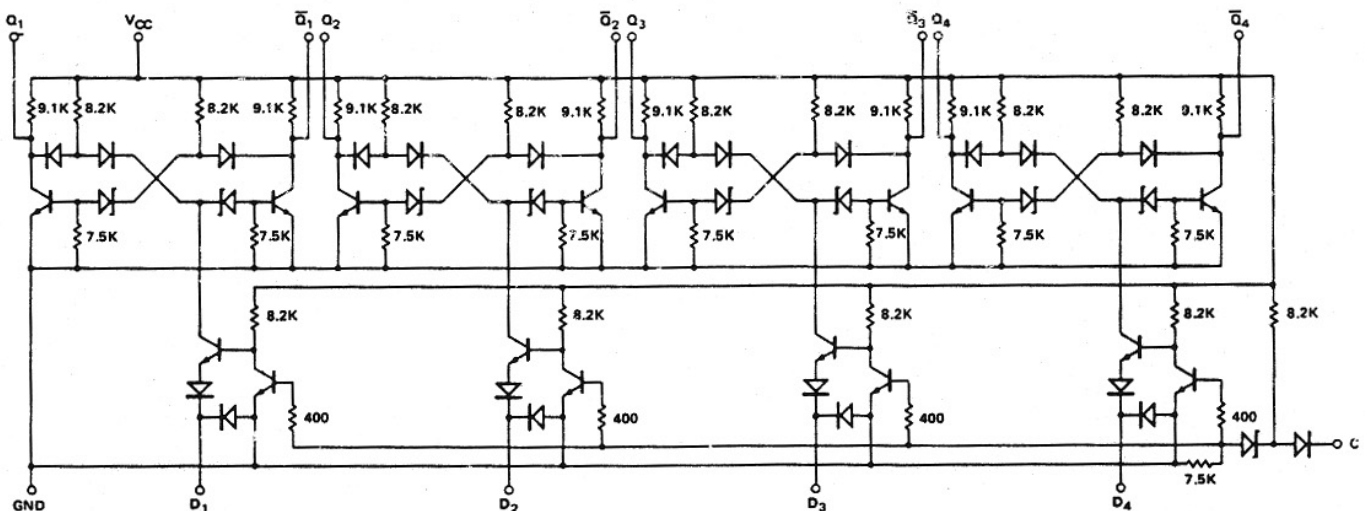
**Logic Diagram**



**TRUTH TABLE**

C	D	$Q^{n+1}$
1	1	$Q^n$
1	0	$\bar{Q}^n$
0	1	1
0	0	0

**Equivalent Circuit**



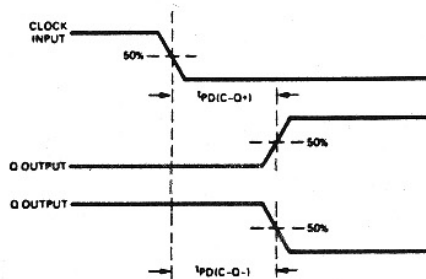
## Key Specifications

$I_{CC}$ (WORST-CASE)	38 mA @ 13V, 48 mA @ 16V	
$t_{PD}$	750 ns	750 ns
I/O FUNCTION FOR $t_{PD}$	C-Q+	C-Q-

Note:  $I_{CC}$  is tested at  $V_{CC} + 1$  Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range.  $t_{PD}$  is guaranteed at  $V_{CC} \pm 1V$  and across the applicable temp range with the output loaded with 4 unit loads.

See page 12 for electrical summary data.

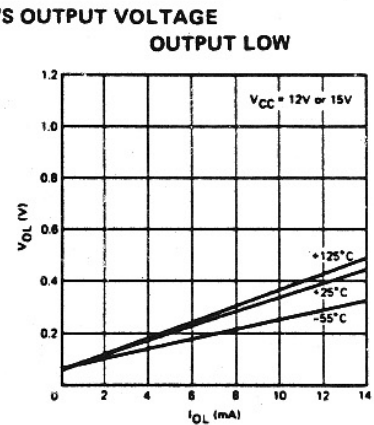
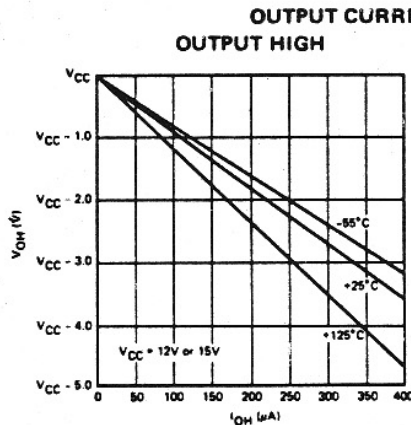
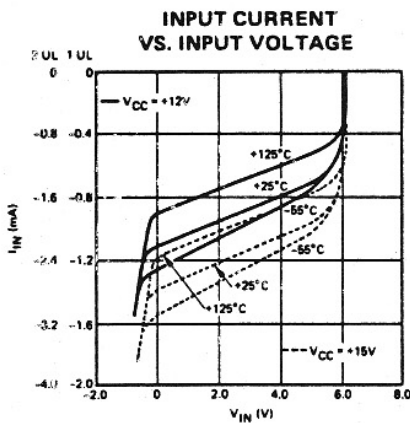
## Switching Time Waveforms



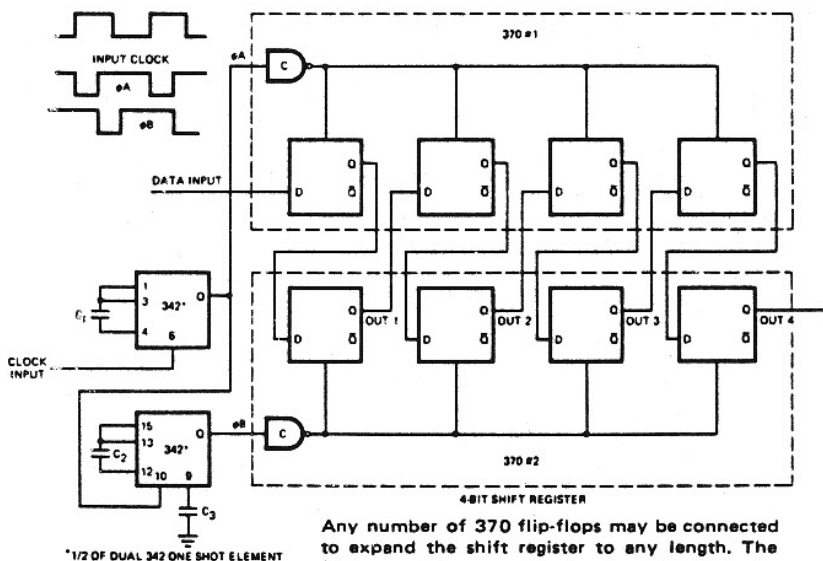
## Loading Table

PINS	FUNCTION	LOADING
D	Data inputs	2 UL
C	Clock input	1 UL
Q, $\bar{Q}$	Outputs	4 UL

## Typical Performance Characteristics



## Typical Applications



Any number of 370 flip-flops may be connected to expand the shift register to any length. The 342 one-shots generate the two-phase clock signals.

Whenever the clock line is high, the flip-flops ignore the data on the D inputs, allowing the clock line to be used as a common input enable control. When the clock line is low, new data can enter the flip-flops and become available on the outputs, as shown by the truth table.