mosaic

Mosaic Semiconductor Inc.

128K x 8 EEPROM

MEM8129-15/20/25

Issue 1.3 : July 1993

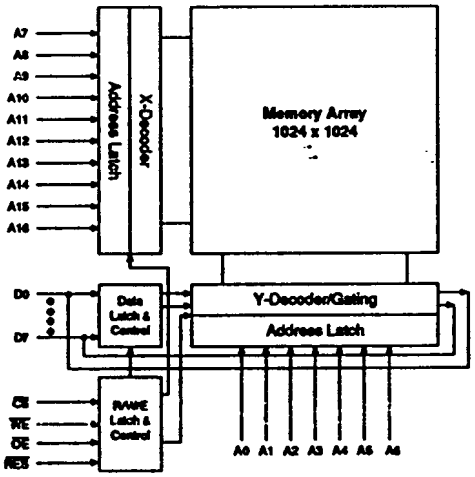
ADVANCE PRODUCT INFORMATION

131,072 x 8 bit MNOS EEPROM

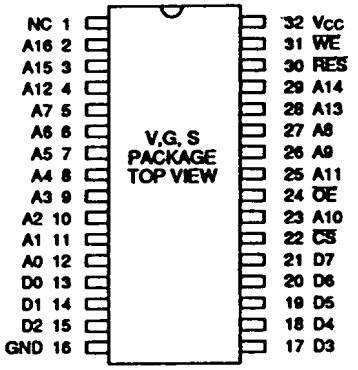
Features

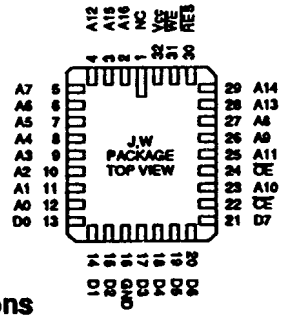
- Fast Access Time of 150/200/250 ns.
- Operating Power 200 mW typical.
- Standby Power 5mW TTL (Max)
  100µA CMOS (Max)
- Software Data Protection.
- Data Polling
- Byte or Page Write Cycle: 5ms typical.
- 128 Byte Page Size
- High Density VIL™ Package.
- Data Retention > 10 years.
- Endurance > 10^4 Write Cycles.
- Data Protection by $\overline{RES}$ pin.
- May be Processed to MIL-STD-883 Method 5004, non-compliant.

Block Diagram



Pin Definition





Pin Functions

A0-16	Address Inputs
D0-7	Data Inputs/Outputs
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RES}$	Reset
NC	No Connect
Vcc	Power (+5V)
GND	Ground

Package Details (See package details section for details)

Pin Count	Description	Package Type	Material	Pin Out
32	100 mil Vertical-In-Line	VIL™	Ceramic	ASIC
32	600 mil Dual-In-Line	DIP	Ceramic	ASIC
32	Bottom Brazed Flatpack	Flatpack	Ceramic	ASIC
32	Leadless Chip Carrier	LCC	Ceramic	ASIC
32	J-Leaded Chip Carrier	JLCC	Ceramic	ASIC

Absolute Maximum Ratings

Voltage on any pin relative to GND	V_T	-0.6 to +7.0	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) V_T can be -3.0V pulse of less than 50ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH} (2)	2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (MEM8129I)
	T_{AM}	-55	-	125	°C (MEM8129M,MB)

Note: (1) V_{IL} can be -1.0V pulse of less than 50ns.
(2) Except $\overline{RES}$ pin.

DC Electrical Characteristics (T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=GND to V_{CC}	-	2	µA
Output Leakage Current	I_{LO}	$V_{I/O}$=GND to V_{CC}	-	2	µA
Average Current	I_{CC1}	$I_{I/O}$=0mA,Duty = 100%, Cycles = 200ns	-	40	mA
Standby Current TTL	I_{SB}	$\overline{CE}$=V_{IH}	-	1	mA
Standby Current CMOS	I_{SB1}	$\overline{CE}$ =V_{CC}, $\overline{OE}$ =V_{IL}, $I_{I/O}$=0mA	-	20	µA
Output Voltage	V_{OL}	I_{OL}=2.1mA	-	0.4	V
	V_{OH}	I_{OH}=-400 µA	2.4	-	V

Note: (1) I_{LI} on $\overline{RES}$ = 100µA max

Capacitance (V_{CC}=5V±10%,T_A=25°C, f=1MHz)

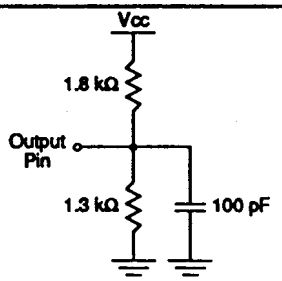
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	C_{IN}	V_{IN} = 0V	-	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	-	12	pF

Note: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

* Input pulse levels: 0.4V to 2.4V
* Input rise and fall times: 20ns
* Input and Output timing reference levels: 0.8V,1.8V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Output Test Load



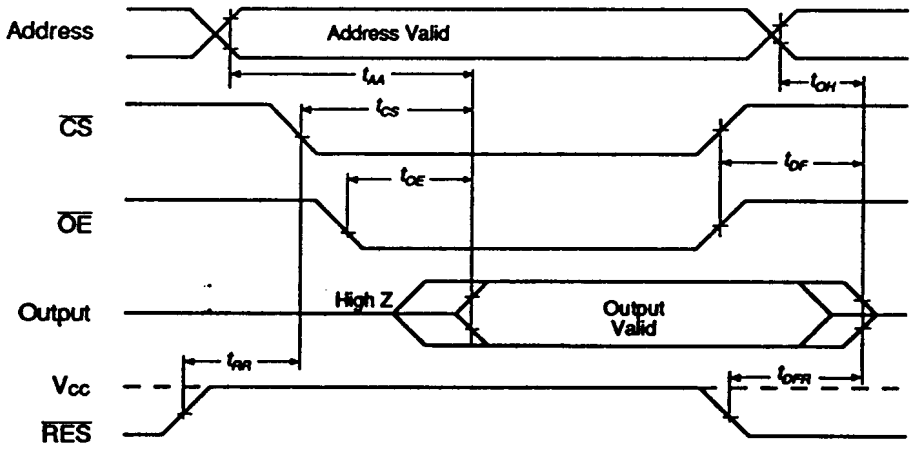
AC READ CHARACTERISTICS

Read Cycle

Parameter	Symbol	-15 min	-15 max	-20 min	-20 max	-25 min	-25 max	Unit	Notes
Address Access Time	t_{AA}	-	150	-	200	-	250	ns	
$\overline{CS}$ Access Time	t_{CS}	-	150	-	200	-	250	ns	
$\overline{OE}$ Access Time	t_{OE}	10	75	10	80	10	90	ns	
$\overline{OE}$ high to output float	t_{DF}	0	50	0	55	0	60	ns	(1)
	t_{DFR}	0	350	0	350	0	350	ns	(1)
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	ns	
$\overline{RES}$ to output delay	t_{RR}	0	600	0	600	0	600	ns	

Notes: (1) t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Cycle Timing Waveform



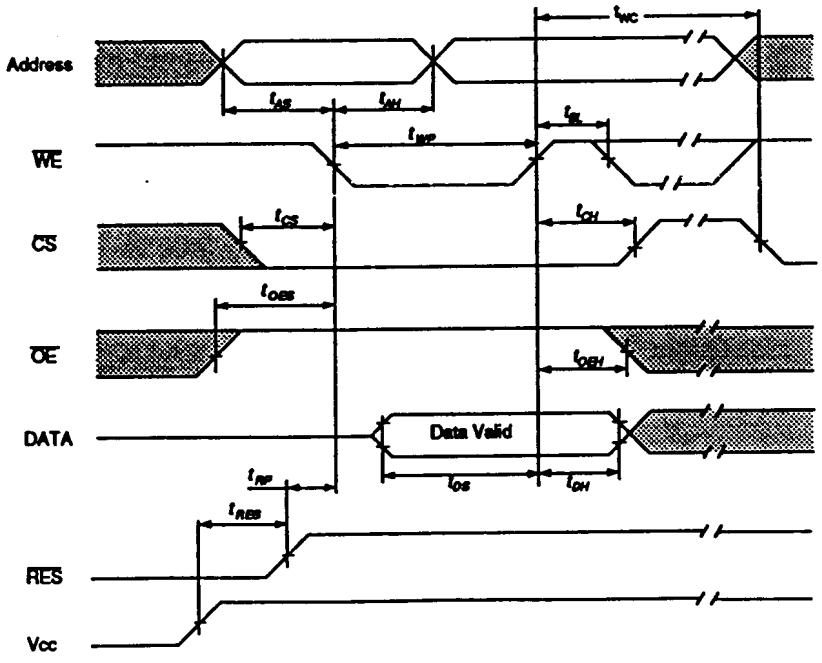
AC WRITE CHARACTERISTICS

Byte and Page Write Cycle

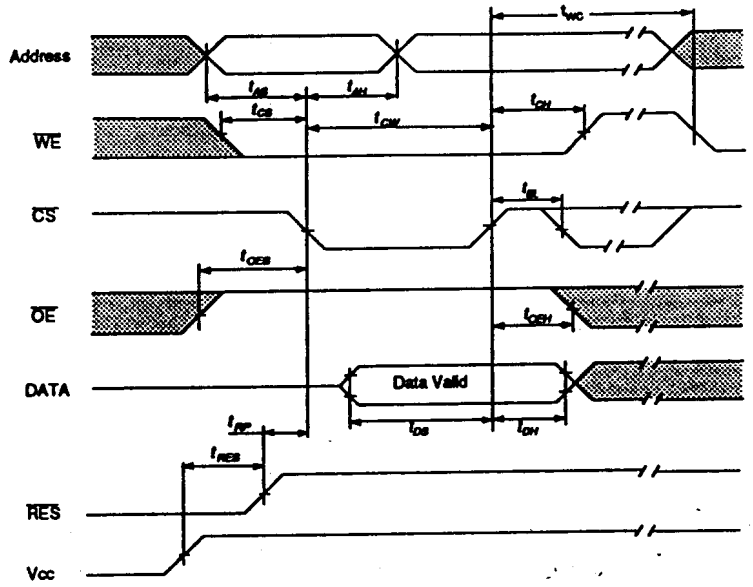
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Write Cycle Time	t_{WC}	15(1)	-	-	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	150	-	-	ns
$\overline{OE}$ Set-up Time	t_{OES}	0	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	-	-	ns
$\overline{OE}$ to Output Delay	t_{OE}	10	-	75	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
	t_{CS}(2)	-	-	150	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Chip Select Pulse Width	t_{CW}	250	-	-	ns
Write Pulse Width	t_{WP}	250	-	-	ns
Data Set-up Time	t_{DS}	100	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Delay to Next Write	t_{DW}	150	-	-	ns
Byte Load Cycle	t_{BLC}	0.55	-	30	µs
Byte Load Window	t_{BL}	100	-	-	µs
Data Latch Time	t_{DL}	300	-	-	ns
$\overline{RES}$ to Write setup time	t_{RP}	100	-	-	µs
V_{CC} to $\overline{RES}$ setup time	t_{RES}	1	-	-	µs

Note: (1) Use this device in longer cycle than this value.
(2) This parameter is for Data Polling Characteristics.
(3) Normal writing is not possible when the $\overline{RES}$ terminal becomes low during writing. The $\overline{RES}$ terminal should not be made low for at least 10ms after the last writing pulse is input.

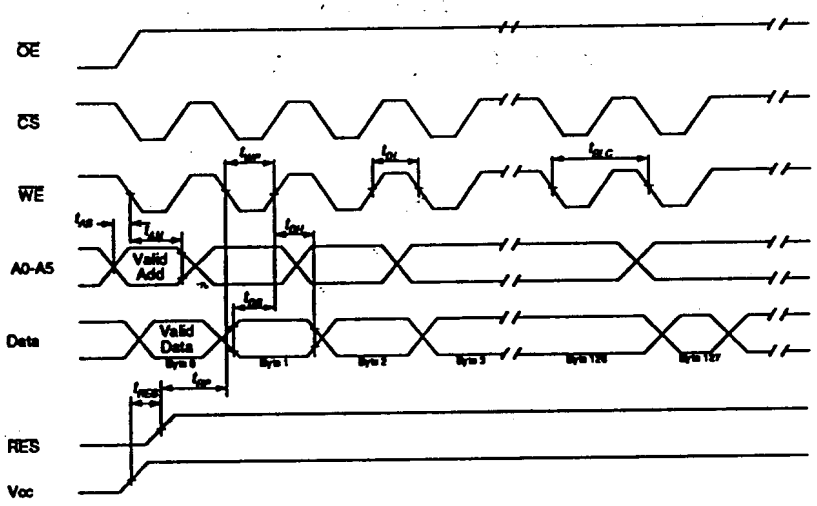
AC Write Waveform - $\overline{WE}$ Controlled



AC Write Waveform - $\overline{CS}$ Controlled

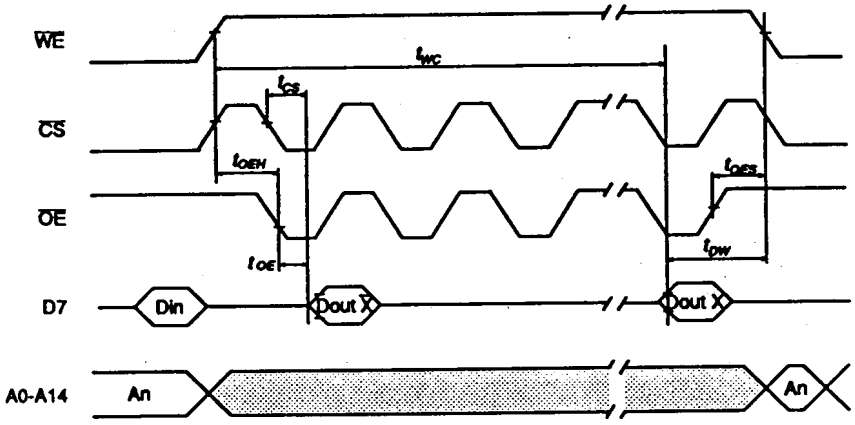


Page Mode Write Waveform



Note: A7 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

DATA Polling Waveform



DEVICE OPERATION

Read

The MEM8129 read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedence state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH.The MEM8129 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Mode Write

The page write feature of the MEM8129 allows the entire memory to be written. Page Write allows 128 bytes of data to be written prior to the commencement of internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A7 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write up to 128 bytes in the same manner as the first byte written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 30 µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence.

DATA Polling

The MEM8129 features DATA Polling to indicate if the write cycle is completed. During the internal programming cycle, any attempt to read the last byte written will produce the compliment of that data on D7. Once the programming is complete, D7 will reflect the true data. Note: If the the MEM8129 is in a protected state and an illegal write operation is attempted DATA Polling will not operate.

Hardware Data Protection

The MEM8129 provides hardware features to protect non-volatile data from inadvertent writes.

* Noise Protection - A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.

$\overline{RES}$ Data Protection

The $\overline{RES}$ singal disables the device, preventing read and write operations. This offers the greatest protection against inadvertant writes during system reset or power-up/down. A full description of this function can be found in "Write Protection for 1M EEPROM Device" available from Mosaic Semiconductor Inc. The $\overline{RES}$ pin should not be made low during t_{WC}.

Mode Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	DATA
Read	LOW	LOW	HIGH	HIGH	Dout
Standby	HIGH	X	X	X	High-Z
Write	LOW	HIGH	LOW	HIGH	Din
Deselect	LOW	HIGH	HIGH	HIGH	High-Z
Write Inhibit	X	X	HIGH	X	-
	X	LOW	X	X	-
Data Polling	LOW	LOW	HIGH	HIGH	Data out
Program	X	X	X	LOW	High-Z

X	Don't Care
Low	V_{IL}
High	V_{IH}

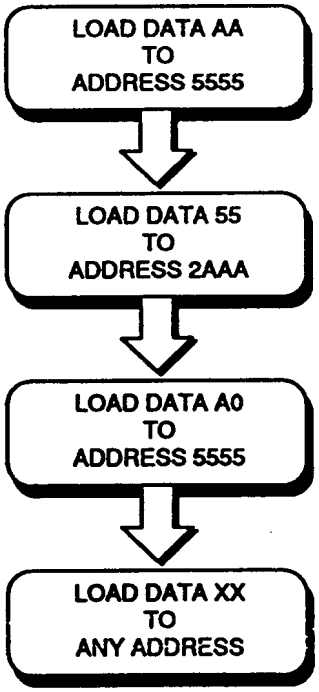
Software Algorithms

The MEM8129 offers the industry standard software algorithms for data protection.

Software Write Protection

The array can be protected against inadvertant writes during power up/ power down or illegal access to the system by employing the Software Write Protect Algorithm.
Selecting the software data protection mode requires the host system to precede the data write operations to three specific addresses. The three byte sequence opens the page write window enabling the host to write from 1 to 128 bytes of data.

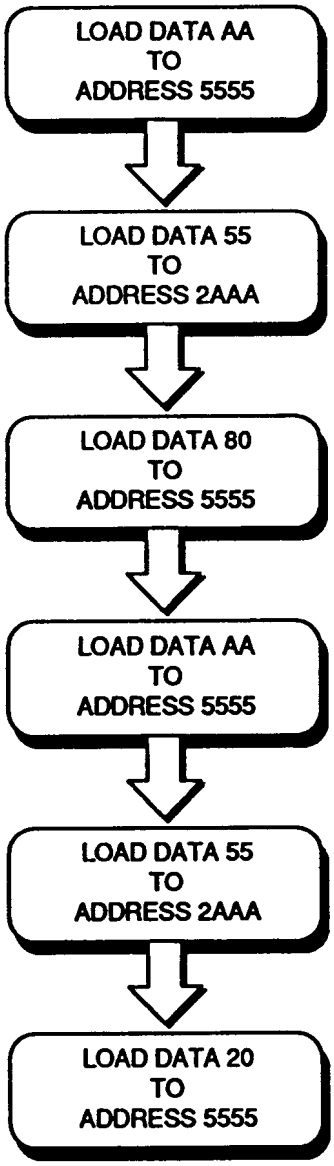
Software Write Protect Algorithm



Software Write Disable

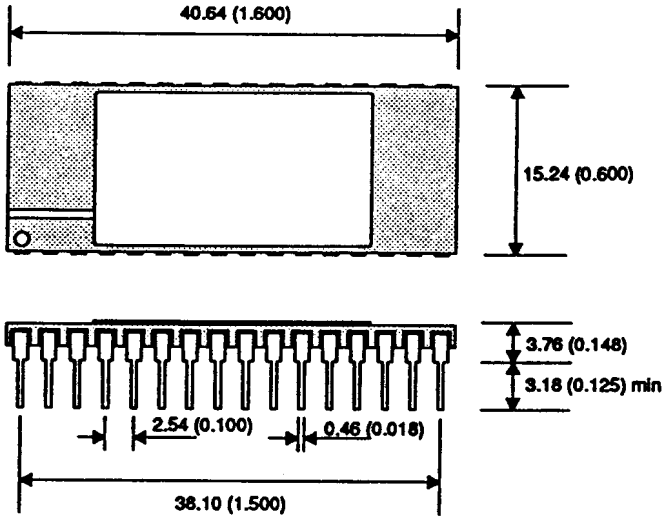
In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer.
The following six step algorithm will reset the internal protection circuit. After t_{WC}, the MEM8129 will be in standard operating mode.

Software Write Disable Algorithm

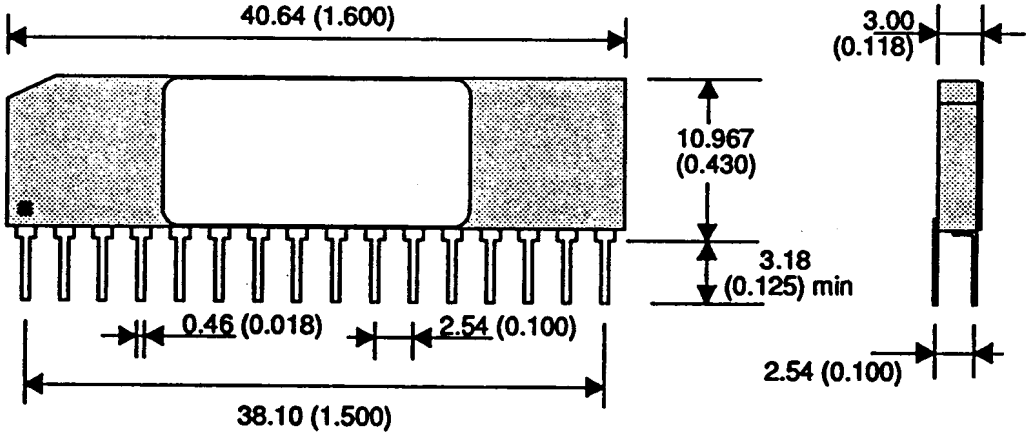


Package Details All dimensions in mm (inches). Tolerance on all dimensions ± 0.254 (0.010).

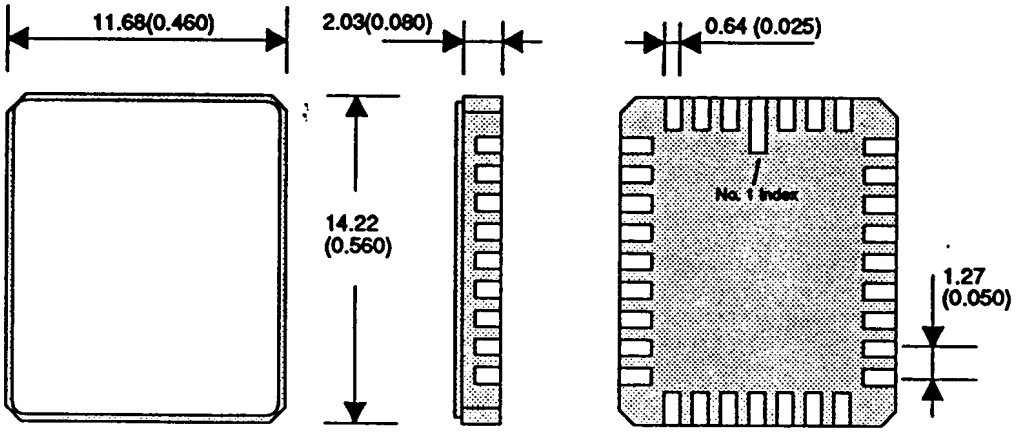
32 Pin 600 mil Dual-In Line (DIP) "S"- Package



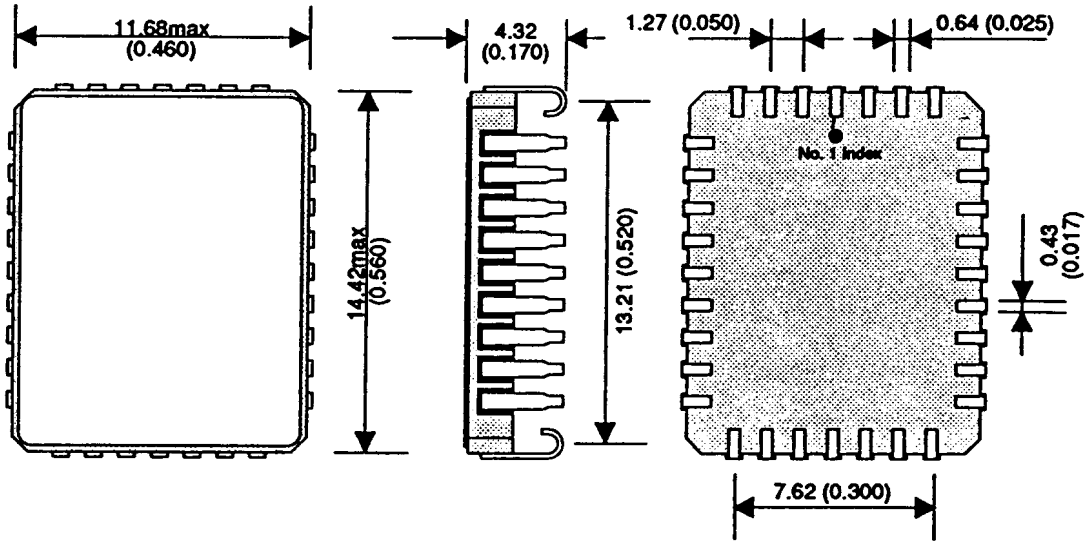
32 Pin 0.1" Vertical-In Line (VIL™) "V"- Package



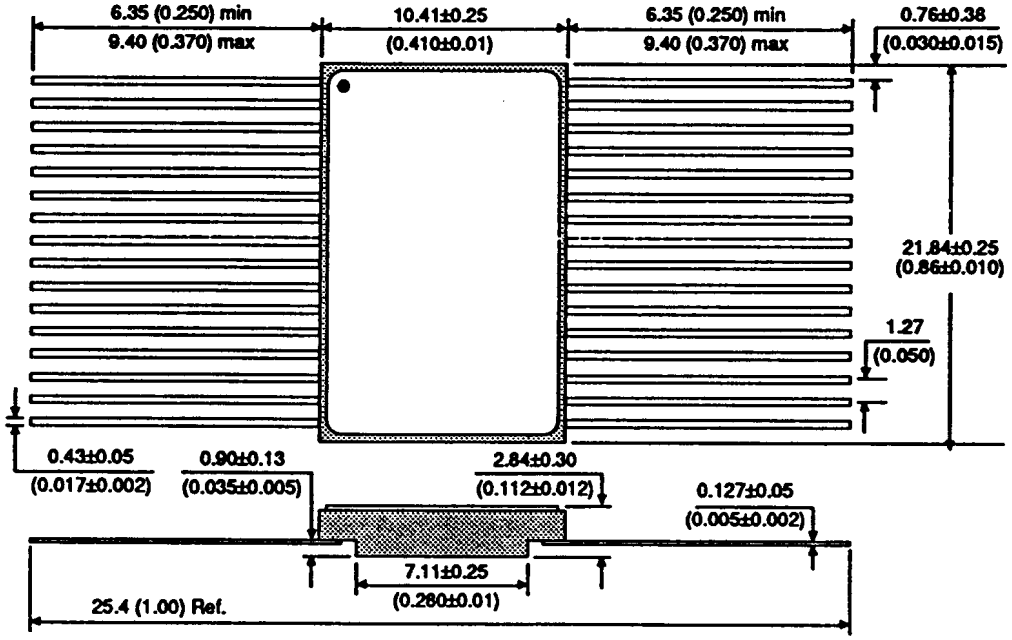
32 pad Leadless Chip Carrier (LCC) - 'W' Package



32 pad 'J' Leaded Chip Carrier (JLCC) - 'J' Package

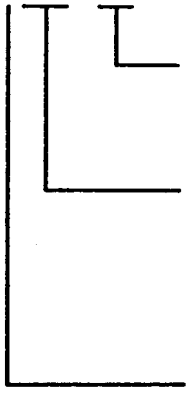


32 pin Ceramic Flatpack - 'G' Package



Ordering Information

MEM8129VMB-15



Speed	15	= 150 ns
	20	= 200 ns
	25	= 250 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL STD-883, Method 5004, non compliant.
Packages	S	= Ceramic 0.6" DIP
	V	= Ceramic 0.1" VIL™
	W	= Ceramic LCC
	J	= Ceramic JLCC
	G	= Ceramic Flatpack

Note: For more information regarding screening flows contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'

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