SERIES

(315) 701-6751

ULTRA HIGH SPEED/VOLTAGE NEGATIVE OUTPUT VIDEO AMPLIFIER

4707 Dev Road Liverpool, N.Y. 13088

FEATURES:

- · Low Cost Complete Amplifier System
- 100Vpp Output Signal Into 10pF

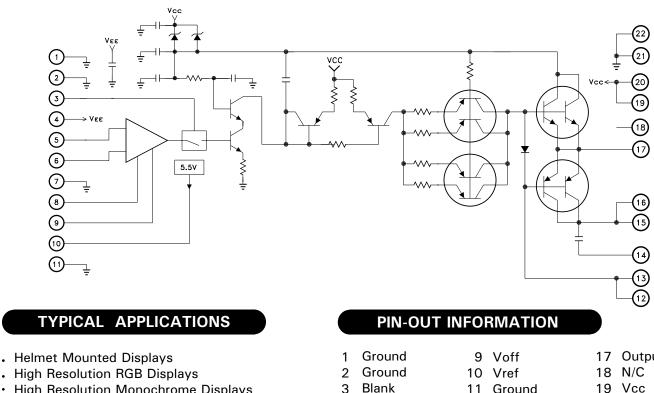
M.S.KENNEDY CORP.

- Ultra Fast Transition Times: 2.5nS @ 50Vpp
- User Adjustable Contrast and Brightness
- TTL Compatible Blanking
- On Board DC Reference Output
- · Customized Versions Readily Available
- Available with Three Lead Bend Options

DESCRIPTION:

The MSK 1933 Series of High Speed, High Voltage Video Amplifiers are designed to drive the grid of today's high performance CRTs. The MSK 1933 has user adjustable contrast and brightness levels and also comes with a blanking function. The MSK 1933 can be directly connected to many video sources including RS170, RS343 and high speed video D/A converters. The MSK 1933 is available in four versions for different applications. The MSK 1933-0 has no internal high voltage resistor or inductor allowing the user to dissipate much of the power externally. The MSK 1933-2, MSK 1933-4 and the MSK 1933-6 each have an internal resistor-inductor designed for optimum bandwidth. The MSK 1933-6 has slightly lower bandwidth but can be operated from up to -120V. Each version of the MSK 1933 is packaged in an isolated 22 pin insulated ceramic substrate that can be directly connected to a heat sink using standard mounting techniques. The leads are available straight out, bent up or bent down.

EQUIVALENT SCHEMATIC



- High Resolution Monochrome Displays
- Automatic Test Equipment
- Medical Monitors
- **CAE/CAD** Station Monitors
- **Projection Displays**
- Beam Index Displays



Ground	9	Voff
Ground	10	Vref
Blank	11	Ground
VEE	12	-VHV RES
-Input	13	-VHV RES
+ Input	14	Ground
Ground	15	-VHV
VGain	16	-VH∨

17	Output
18	N/C

- 19 Vcc
- 20 Vcc
- 21 Ground
- 22 Ground

1

4

5

6

7

8

ABSOLUTE MAXIMUM RATINGS

-VHV	High Voltage Supply (1933-0)	VBL
	(1933-2)	IREF
	(1933-4)75V	Tst
	(1933-6)120V	TLD
Vcc	Positive Supply Voltage+22V	
Vee	Negative Supply Voltage	ТJ
Vin	Differential Input Voltage	I RP
Vic	Common Mode Input Voltage ± 2V	Tc
V_{GAIN}	Gain Adjust Input Voltage0.6 to +6V	
Voff	Offset Adjust Input Voltage0.6 to +6V	

VBLANK	Blank Input Voltage
REF	Reference Output Current
Тsт	Storage Temperature Range -40°C to +150°C
Tld	Lead Temperature Range
	(10 Seconds)
ТJ	Junction Temperature
RP	Current Through Rp
Tc	Case Operating Temperature -25°C to +125°C
	(All Devices)

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions $\textcircled{1}$	MSK1933-0		MSK1933-2		MSK1933-4		MSK1933-6						
Farameter		Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
STATIC														
Quiacoant Current 68	VCM=0V @ +20V	-	75	100	-	75	100	-	75	100	-	75	100	mA
Quiescent Current	VCM=0V @ -10.5V	-	-75	-100	-	-75	-100	-	-75	-100	-	-75	-100	mA
High Voltage Supply 23		-30	-90	-95	-30	-90	-95	-30	-70	-75	-30	-100	-120	V
Thermal Resistance to Case	③ QOUT and QCAS	-	10	13	-	10	13	-	10	13	-	8	12	°C/W
INPUT														
Input Bias Current (6)	VCM=0V	-	± 1	±50	-	± 1	±50	-	± 1	±50	-	± 1	±50	μA
(6)	VBLANK = 0.4V	-	500	600	-	500	600	-	500	600	-	500	600	μA
Blank Input Current $^{(6)}$	VBLANK = 2.4V	-	300	400	-	300	400	-	300	400	-	300	400	μA
Offset Adjust Input Current	⑦ VOFF = 1V	-	2	10	-	2	10	-	2	10	-	2	10	μA
Gain Adjust Input Current (7) VGAIN=5V	-	2	10	-	2	10	-	2	10	-	2	10	μA
Blank Input Pulse Width ③	Normal Operation	30	-	-	30	-	-	30	-	-	30	-	-	nS
Common Mode Rejection Rat	tio (3) VCM = $\pm 0.5V$ F = 10Hz	-	40	-	-	40	-	-	40	-	-	40	-	dB
Input Impedance ③	Either Input F=DC	10K	20K	-	10K	20K	-	10K	20K	-	10K	20K	-	Ω
Input Capacitance (3)	Either Input	-	2	-	-	2	-	-	2	-	-	2	-	pF
Blank Mode Input	VBLANK = 2.4V VIN = 0.3V			1 Ov Dro			1 OvDro			1 OvDro			1 OvDra	m\/
Rejection $\Delta V (3) (4)$	$\Delta V = VHV-VOUT$	-	-	±2xRp	-	-	±2xRp	-	-	±2xRp	-	-	±2xRp	mV
Gain Adjust Rejection ΔV (3)		-	-	±10xRp	-	-	$\pm 10 x R p$	-	-	±10xRp	-	-	$\pm 10 x R p$	mV
Power Supply Rejection Ratio	$3 + VCC$ and $-VEE = Nom \pm 5\%$	25	30	-	25	30	-	25	30	-	25	30	-	dB
Internal Rp ③ ④		-	0	-	380	400	420	190	200	210	380	400	420	Ω
ουτρυτ														
Reference Output Voltage	5) IOUT<2mA	5.2	5.5	5.8	5.2	5.5	5.8	5.2	5.5	5.8	5.2	5.5	5.8	V
	$\Delta V = VHV-VOUT VOFF = 1V$	2D.+	Dra	2 D	2. D.	D	2D.#	2vDn	Dn	2. Do	2D.	D	0. D.	mV
ΔV Blank Mode $\overset{\textcircled{4}56}{56}$	VBLANK = 2.4V VGAIN = 5V	-3xRp	Rp	3xRp	-3xRp	Rp	3xRp	-3xRp	Rp	3xRp	-3xRp	Rp	3xRp	mv
ΔV Min Offset (5) (6) ΔV	V=VHV-VOUT VOFF=0V VGAIN=3V	0	3	6	0	3	6	0	3	6	0	3	10	V
ΔV Max Offset (5) (6)	$\Delta V = VHV-VOUT VOFF = 5V$	32	42	52	32	42	52	16	21	26	32	42	52	V
6	VIN = 0.6V F = 10KHz	70	110	100	70	110	100	26	FF	68	70	4.0.0	4.45	
Voltage Gain ⁶	VGAIN = 3V Both Inputs	72	110	138	72	110	138	36	55		72	120	145	V/V
Output Voltage High 🔞	VGAIN=3V F=10KHz	-85	-88	-	-85	-88	-	-65	-68	-	-95	-98	-	V
Output Voltage Low 6	VGAIN=3V F=10KHz	-	-1	-5	-	-1	-5	-	-1	-5	-	-1	-5	V
Transistion Times ⑦	VIN = 0.6V TR = TF < 0.5nS	-	3.5	6.0	-	3.0	5.0	-	2.5	4.0	-	6	8	nS
Linearity Error ③	/GAIN = 4V VOFF = 1V VCM = 0.5V	-	-	± 2	-	-	±2	-	-	±2	-	-	±2	%GS
Gain Linearity ③	VOFF = 1V VIN = 2.0V VCM = 0.5V	-	-	±2	-	-	±2	-	-	±2	-	-	±2	%
Thermal Distortion ③		-	-	±2	-	-	± 2	-	-	±2	-	-	± 2	%GS

NOTES:

(1) + Vcc = +20V, -VEE = -10.5V, VBLANK = VGAIN = VOFF = ±VIN = 0V, CL = 10pF, Tc = 25°C unless otherwise specified.
(2) VHv = Typical Value for each dash number for all parameters.
(3) This parameter is guaranteed by design but need not be tested. Typical parameters are representative of actual device performance but are for reference only.
(4) RP = Internal RP except MSK 1933-0. External value = 400Ω unless otherwise specified for the MSK 1933-0.
(5) ΔV is defined as the difference between -VHv and the output.
(6) Deventer is 1000 to the divide of a contained on the integral.

B Parameter is 100% tested on production devices.
Parameter is sample tested in accordance with MSK industrial grade quality devices.
When the output is amplifying a video signal, the output current will be present at +Vcc and -VHv since the output is referred to +Vcc internally.

POWER SUPPLIES

The input stage of the MSK 1933 requires power supplies of +20V and -10.5V for optimum operation. The negative power supply can be increased to -12V if -10.5V is not available, but additional power dissipation will cause the internal temperature to rise. Both low voltage power supplies should be effectively decoupled with tantalum capacitors (at least 4.7 μ F) connected as close to the amplifier's pins as possible. The MSK 1933 has internal 0.01 μ F capacitors that also improve high frequency performance. It is also recommended to put 0.1 μ F decoupling capacitors on the +20V and -10.5V supplies as well. Since the output stage is returned to +20V internally, all of the output current will flow through this supply pin.

The high voltage power supply (-VHV) is connected to the amplifier's output stage and must be kept as stable as possible. The internal or external Rp is connected to -VHV and as such, the amplifier's DC output is directly related to the high voltage value. The -VHV pins of the hybrid should be decoupled to ground with as large a capacitor as possible to improve output stability.

SUPPLY SEQUENCING

The power supply sequence is VHV, VCC, VEE followed by the other DC control inputs. If power supply sequencing is not possible, the time difference between each supply should be less than five milliseconds. If the DC control signals are being generated from a low impedance source other than the VREF output, reverse biased diodes should be connected from each input (VGAIN, VOFF) to the VCC pin. This will protect the inputs until VCC is turned on.

VIDEO OUTPUT

When power is first applied and VIN = VGAIN = VOFF = OV, the output will be practically at the -VHV rail voltage. The output voltage is a function of the value of Rp and also the VGAIN and VOFF DC inputs. The maximum output voltage swing for any of the MSK 1933 variants is determined by Vpp = (250mA) x (Rp). The bandwidth of the amplifier largely depends on both Rp and Lp.

Hybrid pins 12 and 13 are directly connected to Rp. Additional external resistance can be added to reduce power dissipation, but slower transition times will result. If an additional resistor is used, it must be low capacitive and the layout should minimize capacitive coupling to ground (ie: no ground plane under Rp).

The MSK 1933 Series is conservatively specified with low values for Lp which yield about 5% overshoot. Additional peaking can be obtained by using a high self-resonant frequency inductor in series with pins 12 & 13. Since this value of inductance can be very dependent on circuit layout, it is best to determine its value by experimentation. A good starting point is typically 0.47μ H for the MSK 1933-0 and 0.0047μ H for the remaining devices.

If external resistors or inductors are not used, be sure to connect high frequency bypass capacitors directly from pins 12 and 13 to ground for the devices that contain an internal Rp.

VIDEO INPUTS

The video input signals should be kept below $\pm 2 V \text{MAX}$ total, including both common mode offset and signal levels. The input structure of the MSK 1933 was designed for $\pm 0.714 V \text{pp}$ RS343 signals. If either input is not used it should be connected directly to the analog ground or through a 25Ω resistor to ground if input offset currents are to be minimized.

OUTPUT PROTECTION

The output pin of the MSK 1933 should be protected from transients by connecting reversed biased ultra-low capacitance diodes from the output pin to both -VHV and ground. The output can also be protected from arc voltages by inserting a small value (25-50 Ω) resistor in series with the amplifier. This resistor will reduce system bandwidth along with the load capacitance, but a series inductor can reduce the problem substantially.

VGAIN CONTROL INPUT

The VGAIN control (contrast) input is designed to allow the user to vary the video gain. By simply applying a DC voltage from OV to VREF, the video gain can be linearly adjusted from 0 to 195V/V (MSK 1933-2). The VGAIN input should be connected to the VREF pin through a 5K Ω pot to ground. For convenient stable gain adjustment, a 0.1 μ F bypass capacitor should be connected near the VGAIN input pin to prevent output instability due to noisy sources. Digital gain control can be accomplished by connecting a D/A converter to the VGAIN pin. However, some temperature tracking performance may be lost when using an external DC voltage source other than VREF for gain adjustment. The bandwidth of the VGAIN input is approximately 1MHz.

The overall video output of the MSK 1933 can be characterized using the following expression:

Here is a sample calculation for the MSK 1932-2: Given information

• $V_{IN} = 0.7V$ • $V_{GAIN} = 1VDC$ • $Rp = 400\Omega$ (internal) • $V_{HV} = -80VDC$ VHV-VOUT = (0.7V)(1V)(400\Omega)(0.09) VHV-VOUT = 25.2V Nominal

The expected video output would swing from approximately -80V to -54.8V assuming that VOFF = 0V. This calculation should be used as a nominal result because the overall gain may vary as much as $\pm 20\%$ due to internal high speed device variations. Changing ambient conditions can also effect the video gain of the amplifier by as much as 150 PPM/°C. It is wise to connect all video amplifiers to a common heat sink to maximize thermal tracking when multiple amplifiers are used in applications such as RGB systems. Additionally, only one of the VREF outputs should be shared by all three amplifiers. This voltage should be buffered with a suitable low drift op-amp for best tracking performance.

VOFF CONTROL INPUT

The brightness (output offset) can be linearly adjusted by applying a 0 to VREF DC voltage to the VOFF input pin. The output quiescent voltage range is from approximately (5 μ A)(Rp) to (100mA)(Rp) from -VHV. This control voltage is normally generated by connecting the VOFF control pin to a 5K potentiometer between VREF and ground. The VOFF input pin should be bypassed with a 0.1 μ F capacitor to ground placed as close as possible to the hybrid. This DC voltage can be any stable system source. The bandwidth of the VOFF pin is approximately 1MHz.

Keep hybrid power dissipation in mind when adjusting the output quiescent voltage. Practically all of the voltage is seen across Rp! This power must be taken into account when high Rp currents are used. If the quiescent level is set too close to -VHV, the power dissipation will be minimal but the rise time will suffer slightly. If the quiescent level is set too far from -VHV, the power dissipation will increase dramatically and the output fall time will be limited. The output black level is obviously dependent on system requirements but a little experimentation will strike the optimum balance between power dissipation and bandwidth. Total current through Rp should be limited to less than 290mA when operating from power supplies greater than 90V. The gain adjust alone can set the AC current to 250mA (ie: $250mApp = 100Vpp/400\Omega$). Typically, most applications use about 10V from -VHV for a black level.

BLANK INPUT

The video input can be electrically disconnected from the ampliifer by applying a TTL high input to the blank pin. When this occurs, the output will be set to approximately -VHV. The VGAIN and VOFF control pins have little or no effect on the output when it is in blank mode.

When the TTL compatible blank input is not used, the pin must be connected to ground to enable the amplifier. The blank input will float high when left unconnected which will disable the video.

VREF OUTPUT

The MSK 1933 has an on board buffered DC zener reference output. The VREF output is nominally 5.5V DC and has full temperature test limits of 5.2V to 5.8V DC. This output is provided for gain and offset adjustment and can source up to 4mA of current.

THERMAL MANAGEMENT

The MSK 1933 package has mounting holes that allow the user to connect the amplifier to a heat sink or chassis. Since the package is electrically isolated from the internal circuitry, mounting insulators are not required or desired for best thermal performance. Use 4 to 6 inch/pounds for mounting the device to the heat sink.

The power dissipation of the amplifier depends mainly on the load requirements, bandwidth, pixel size, black level and the value of Rp. The following table illustrates a few examples:

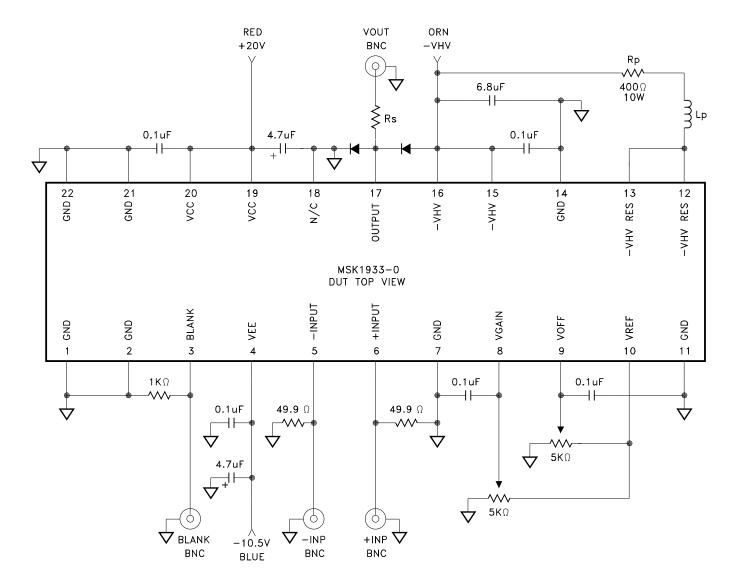
DEVICE	BLACK		WHITE	OUTPUT	PEF	CENT OF SIG	NAL	OUTPUT	TOTAL
ТҮРЕ	-VHV	LEVEL	LEVEL	VOLTAGE	BLANK	BLACK	WHITE	AVE. Pd	AVE. Pd
1933-6	-120V	-110V	-20V	0V	100%	0%	0%	OW	2.5W
1933-6	-120V	-110V	-20V	-90V	20%	40%	40%	13.3W	15.7W
1933-4	-70V	-65V	-15V	0V	100%	0%	0%	OW	2.5W
1933-4	-70V	-65V	-15V	-50V	20%	40%	40%	8.4W	10.6W

This table does not include power dissipation due to output switching since this is dependent on individual load requirements. The input stage power dissipation is typically 2.5 watts and is essentially independent of output levels.

Display Resolution	Maximun Pixel Time	Minimum Pixel Clock Frequency	Required Rise Time at CRT	Required System Bandwidth (F-3dB)
320 x 200	182nS	5MHz	60nS	6MHz
640 x 350	52nS	19MHz	17nS	20MHz
640 x 480	38nS	26MHz	12.5nS	28MHz
800 x 560	26nS	38MHz	8.6nS	41MHz
1024 x 900	12.6nS	80MHz	4.2nS	84MHz
1024 x 1024	11nS	90MHz	3.7nS	95MHz
1280 x 1024	8.9nS	112MHz	2.9nS	120MHz
1664 x 1200	5.8nS	170MHz	1.9nS	180MHz
2048 x 2048	2.8nS	360MHz	1nS	380MHz
4096 x 3300	860pS	1.2GHz	280pS	1.23GHz

All data assumes retrace time equal to 30% of frame time and a 60Hz refresh rate.

TYPICAL CONNECTION CIRCUIT

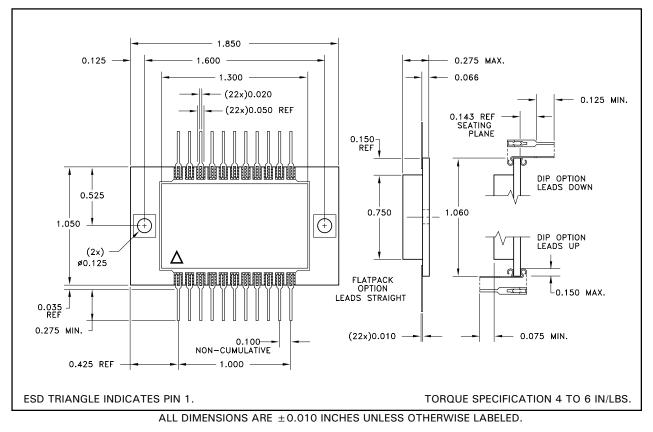


The connection circuit shown above is for the MSK 1933-0 evaluation board. The Rp and Lp are external components and must not be located near ground planes if possible. A high quality resistor such as Bradford Electronics P/ N FP10-400 is required for optimum response times. Use an inductor with a high self-resonant frequency that can withstand the currents required for the application.

When using the other variants of the MSK 1933, place an additional bypass capacitor on pins 12 and 13 if series (Rp and Lp) components are not utilized. The pin should connect to -VHV with a short low impedance path.

For additional applications information, please contact the factory. Evaluation amplifiers with test boards are readily available for MSK.

NOTES:



ORDERING INFORMATION

PART NUMBER	LEAD OPTION	-VHV MAX	INTERNAL RP	TYPICAL RISE TIME	SCREENING LEVEL
MSK 1933S-0	STRAIGHT				
MSK 1933D-0	DOWN	-95V	NONE	3.5nS	Industrial
MSK 1933U-0	UP				
MSK 1933S-2	STRAIGHT				
MSK 1933D-2	DOWN	-95V	400Ω	3.0nS	Industrial
MSK 1933U-2	UP				
MSK 1933S-4	STRAIGHT				
MSK 1933D-4	DOWN	-75V	200Ω	2.5nS	Industrial
MSK 1933U-4	UP				
MSK 1933S-6	STRAIGHT				
MSK 1933D-6	DOWN	-120V	400Ω	6.0nS	Industrial
MSK 1933U-6	UP				

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