H-BRIDGE MOSFET POWER MODULE 3020

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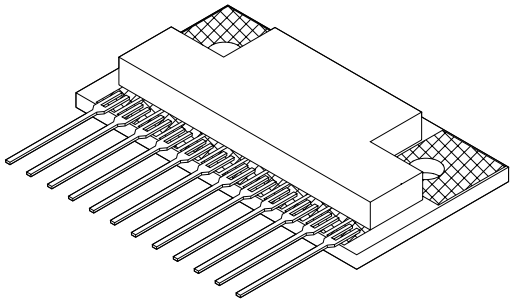
FEATURES:

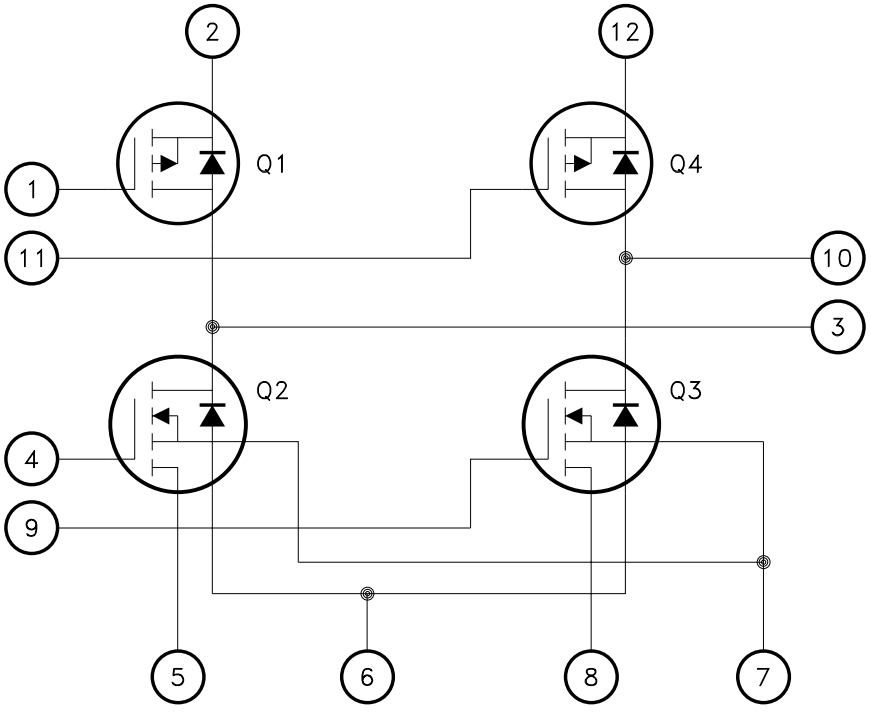
- Pin Compatible with MPM3002 and MPM3012
- P and N Channel MOSFETs for Ease of Drive
- N Channel Current Sensing MOSFET for Lossless Sensing
- Isolated Package for Direct Heat Sinking, Excellent Thermal Conductivity
- Avalanche Rated Devices
- 100 Volt, 10 Amp Full H-Bridge



DESCRIPTION:

The MSK 3020 is an H-bridge power circuit packaged in a space efficient isolated ceramic tab power SIP package. The MSK 3020 consists of P-Channel MOSFETs for the top transistors and N-Channel MOSFETs for the bottom transistors. The N Channel MOSFETS are current sensing to allow lossless current sensing for current controlled applications. The MSK 3020 uses M.S. Kennedy's proven power hybrid technology to bring a cost effective high performance circuit for use in today's sophisticated servo motor and disk drive systems. The MSK 3020 is pin compatible with the MPM3002 and MPM3012 with some differences in specifications.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- Stepper Motor Servo Control
- Disk Drive Head Control
- X-Y Table Control
- Az-El Antenna Control

PIN-OUT INFORMATION

1	Gate Q1	7	Source 2, 3
2	Source Q1	8	Sense Q3
3	Drain 1, 2	9	Gate Q3
4	Gate Q2	10	Drain 3, 4
5	Sense Q2	11	Gate Q4
6	Kelvin Source 2, 3	12	Source 4

ABSOLUTE MAXIMUM RATINGS

V_{DSS}	Drain to Source Voltage	100V	MAX
V_{DGDR}	Drain to Gate Voltage (RGS = 1 MW)	100V	MAX
V_{GS}	Gate to Source Voltage (Continuous)	±20V	MAX
I_D	Continuous Current	10A	MAX
I_{DM}	Pulsed Current	25A	MAX
R_{TH-JC}	Thermal Resistance (Junction to Case)	4.0°C/W	
I_M	Sense Current - Continuous	13 mA	MAX
I_{MM}	Sense Current Peak	33 mA	

	Single Pulse Avalanche Energy	
	(Q1, Q4)	7.9 mJ
	(Q2, Q3)	69 mJ
T_J	Junction Temperature	+175°C MAX
T_{ST}	Storage Temperature	-55°C to +150°C
T_C	Case Operating Temperature Range	-55°C to +125°C
T_{LD}	Lead Temperature Range (10 Seconds)	300°C MAX

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions 4◯	MSK 3020 Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage	V_{GS} = 0 I_D = 0.25 mA (All Transistors)	100	-	-	V
Drain-Mirror Breakdown Voltage	V_{GS} = 0 V_{DS} = 100V, (Q2, Q3)	100	-	-	V
Drain-Source Leakage Current	V_{DS} = 100V V_{GS} = 0V, (Q2, Q3)	-	-	25	µA
	V_{DS} = -100V V_{GS} = 0V, (Q1, Q4)	-	-	-25	µA
Gate-Source Leakage Current	V_{GS} = ±20V V_{DS} = 0V (All Transistors)	-	-	±100	nA
Gate-Source Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA (Q2, Q3)	2.0	-	4.0	V
	V_{DS} = V_{GS} I_D = 250 µA (Q1, Q4)	-2.0	-	-4.0	V
Drain-Source on Resistance ②	V_{GS} = 10V I_D = 8.4A (Q2, Q3)	-	-	0.26	W
	V_{GS} = -10V I_D = -8.4A (Q1, Q4)	-	-	0.31	W
Drain-Source on Resistance ③	V_{GS} = 10V I_D = 8.4A (Q2, Q3)	-	-	0.16	W
	V_{GS} = -10V I_D = -8.4A (Q1, Q4)	-	-	0.20	W
Forward Transconductance ①	V_{DS} = 50V I_D = 8.4A (Q2, Q3)	4.7	-	-	S
	V_{DS} = -50V I_D = -8.4A (Q1, Q4)	3.2	-	-	S
N-CHANNEL (Q2, Q3)					
Total Gate Charge ①	I_D = 14A	-	-	26	nC
Gate-Source Charge ①	V_{DS} = 80V	-	-	5.5	nC
Gate-Drain Charge ①	V_{GS} = 10V	-	-	11	nC
Turn-On Delay Time ①	V_{DD} = 50V	-	9.5	-	nS
Rise Time ①	I_D = 14A	-	42	-	nS
Turn-Off Delay Time ①	R_G = 12W	-	22	-	nS
Fall Time ①	R_D = 3.5W	-	25	-	nS
Input Capacitance ①	V_{GS} = 0V	-	700	-	pF
Output Capacitance ①	V_{DS} = 25V	-	320	-	pF
Reverse Transfer Capacitance ①	f = 1 MHz	-	83	-	pF
Output Capacitance of Sensing Cells ❍		-	9	-	pF
Current Sensing Ratio ①	V_{GS} = 10V I_D = 14A	1390	-	1540	r
P-CHANNEL (Q1, Q4)					
Total Gate Charge ①	I_D = -8.4A	-	-	58	nC
Gate-Source Charge ①	V_{DS} = -80V	-	-	8.3	nC
Gate-Drain Charge ①	V_{GS} = -10V	-	-	32	nC
Turn-On Delay Time ①	V_{DD} = -50V	-	15	-	nS
Rise Time ①	I_D = -8.4A	-	58	-	nS
Turn-Off Delay Time ①	R_G = 9.1W	-	45	-	nS
Fall Time ①	R_D = 6.2W	-	46	-	nS
Input Capacitance ①	V_{GS} = 0V	-	760	-	pF
Output Capacitance ①	V_{DS} = -25V	-	260	-	pF
Reverse Transfer Capacitance ①	f = 1 MHz	-	170	-	pF
BODY DIODE					
Forward on Voltage ①	I_S = 14A V_{GS} = 0V (Q2, Q3)	-	2.5	-	V
	I_S = -14A V_{GS} = 0V (Q1, Q4)	-	-1.6	-	V
Reverse Recovery Time ①	I_S = 14A di/dt = 100A/µS (Q2, Q3)	-	150	310	nS
	I_S = -8.4A di/dt = 100A/µS (Q1, Q4)	-	47	71	nS
Reverse Recovery Charge ①	I_S = 14A di/dt = 100A/µS (Q2, Q3)	-	0.85	1.2	µC
	I_S = -8.4A di/dt = 100A/µS (Q1, Q4)	-	650	970	nC

NOTES:

① This parameter is guaranteed by design but need not be tested. Typical parameters are representative of actual device performance but are for reference only.

② Resistance as seen at package pins.

③ Resistance for die only; use for thermal calculations.

④ T_A = 25°C unless otherwise specified.

APPLICATION NOTES

N-CHANNEL GATES (Q2, Q3):

For driving the N-Channel gates, it is important to keep in mind that it is essentially like driving a capacitance to a sufficient voltage to get the channel fully on. Driving the gates to +15 volts with respect to their sources assures that the transistors are on. This will keep the dissipation down to a minimum level. How quickly the gate gets turned ON and OFF will determine the dissipation of the transistor while it is transitioning from OFF to ON and vice-versa. Turning the gate ON and OFF too slow will cause excessive dissipation, while turning it ON and OFF too fast will cause excessive switching noise in the system. It is important to have as low a driving impedance as practical for the size of the transistor. Many motor drive IC's have sufficient gate drive capability for the MSK 3020. If not, paralleled CMOS standard gates will usually be sufficient. A series resistor in the gate circuit slows it down, but also suppresses any ringing caused by stray iductances in the MOSFET circuit. The selection of the resistor is determined by how fast the MOSFET wants to be switched. See Figure 1 for circuit details.

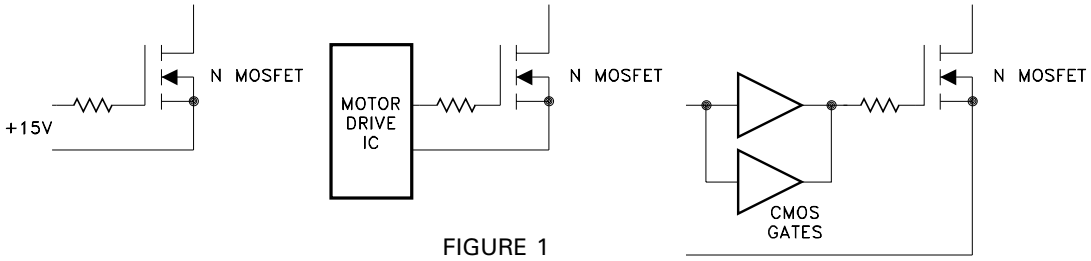


FIGURE 1

P-CHANNEL GATES (Q1, Q4):

Most everything applies to driving the P-Channel gates as the N-Channel gates. The only difference is that the P-Channel gate to source voltage needs to be negative. Most motor drive IC's are set up with an open collector or drain output for directly interfacing with the P-Channel gates. If not, an external common emitter switching transistor configuration (see Figure 2) will turn the P-Channel MOSFET on. All the other rules of MOSFET gate drive apply here. For high supply voltages, additional circuitry must be used to protect the P-Channel gate from excessive voltages.

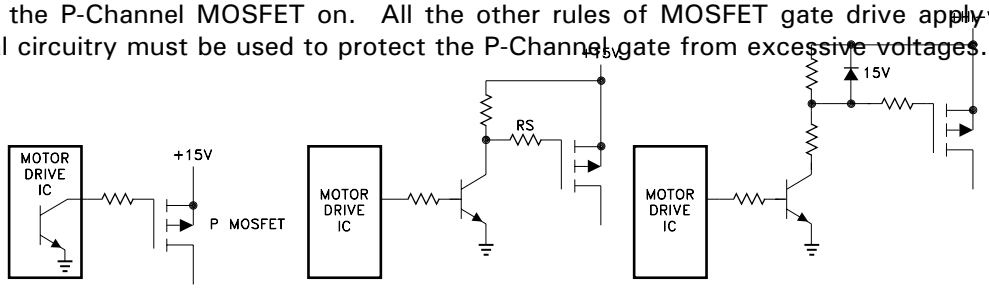


FIGURE 2

BRIDGE DRIVE CONSIDERATIONS:

It is important that the logic used to turn ON and OFF the various transistors allow sufficient "dead time" between a high side transistor and its low side transistor to make sure that at no time are they both ON. When they are, this is called "shoot-through" and it places a momentary short across the power supply. This overly stresses the transistors and causes excessive noise as well. See Figure 3.

FIGURE 3

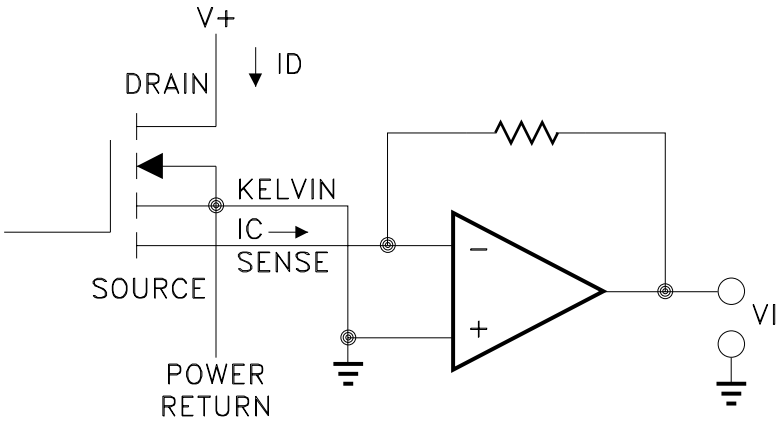
This deadtime should allow for the turn on and turn off time of the transistors, especially when slowing them down with gate resistors. This situation will be present when switching motor direction, or when sophisticated timing schemes are used for servo systems such as locked antiphase PWM'ing for high bandwidth operation.

USING CURRENT SENSING MOSFETS:

A MOSFET transistor is constructed of many individual MOSFET cells connected in parallel. They share the current total very evenly. If one of these cells are brought out to a pin, that cell will pass an accurate proportional amount of the total current. This current can be used as a low power sense of the whole current without passing that whole current through a sensing device like a resistor. This small current multiplied by the ratio specified on the data sheet equals the whole current.

There are several methods of working with the sense function to obtain the actual current.

1. Virtual Earth Sensing

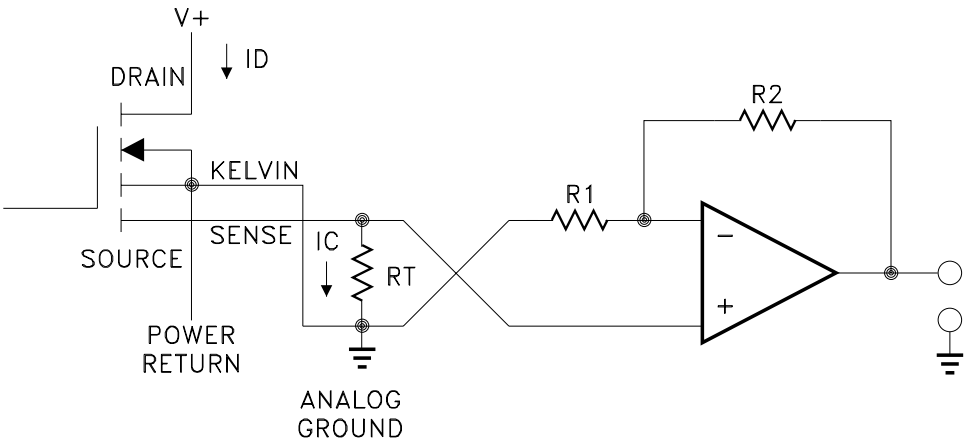


$$VI = -RIC = \frac{-RID}{r + 1}$$

WHERE r = CURRENT SENSE RATIO, ISOURCE ÷ ISENSE

The disadvantage is amplifying a current swing of 10 amps in 100 nSec to produce a 5V output means the op amp has to slew 50V/μSec. This is beyond the capabilities of a lot of op amps.

2. Resistor Sensing



$$VS = \frac{R2}{R1} \times RT \times \frac{ID}{r + 1}$$

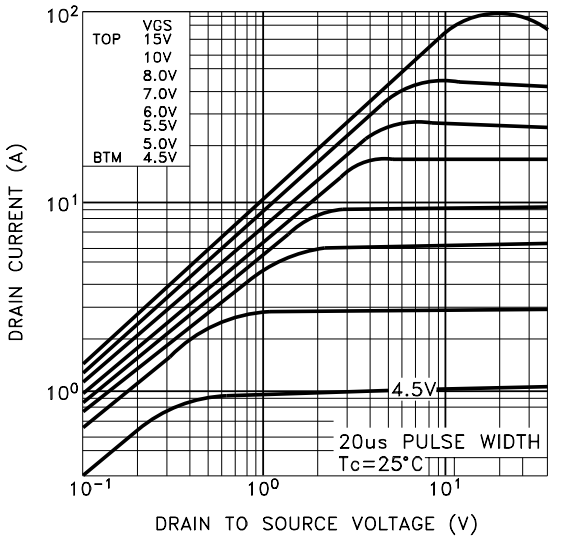
IF RT<10% OF RDS(ON) x r

The disadvantage is R_T voltage must be above the offset voltage of the op amp and R_T must be much less than $R_{DS(ON)}$ of the sensing cell or temperature shifts will affect accuracy.

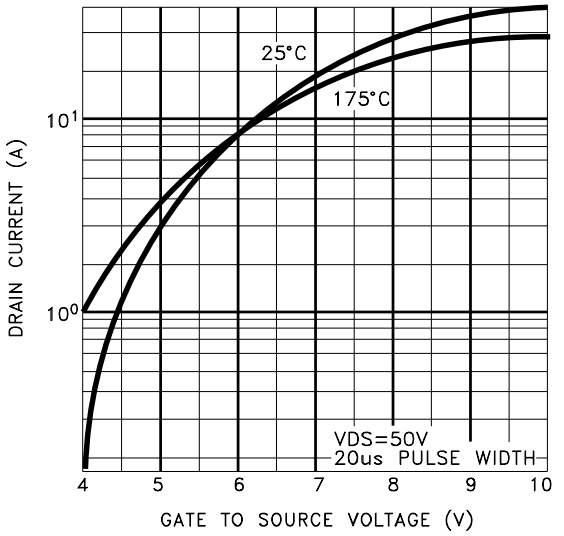
TYPICAL PERFORMANCE CURVES

N-CHANNEL DEVICES (Q2,Q3)

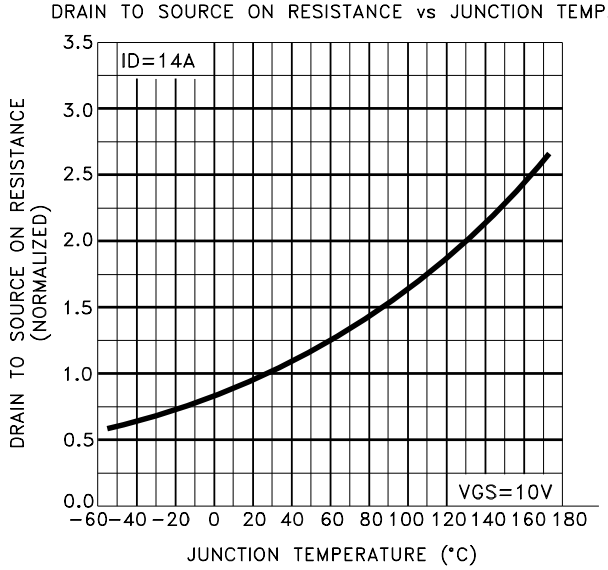
DRAIN CURRENT vs DRAIN TO SOURCE VOLTAGE



DRAIN CURRENT vs GATE TO SOURCE VOLTAGE

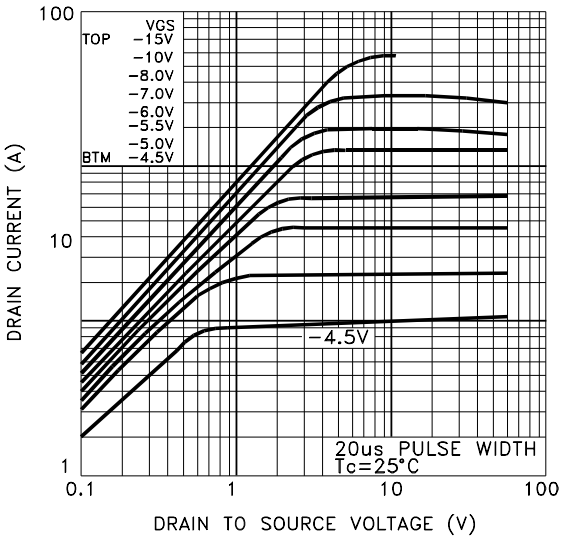


DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMP.

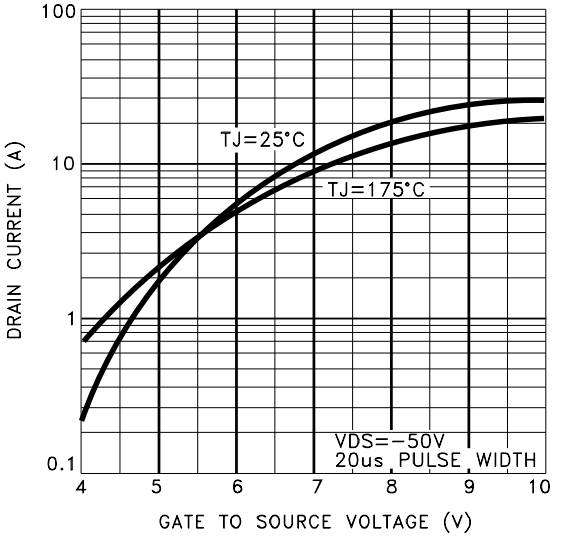


P-CHANNEL DEVICES (Q1,Q4)

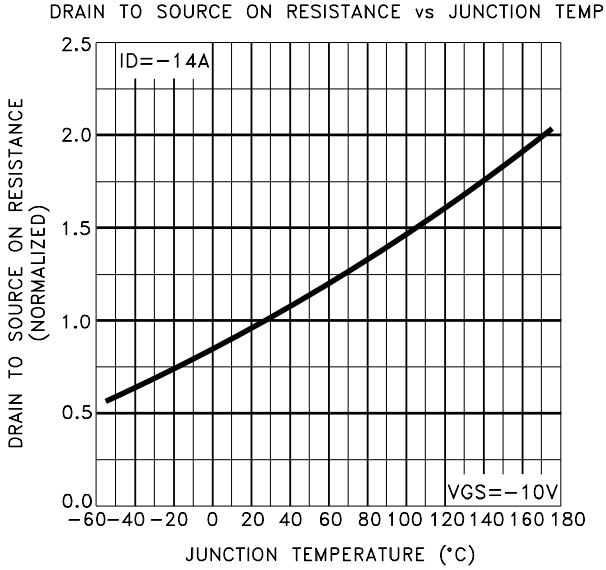
DRAIN CURRENT vs DRAIN TO SOURCE VOLTAGE

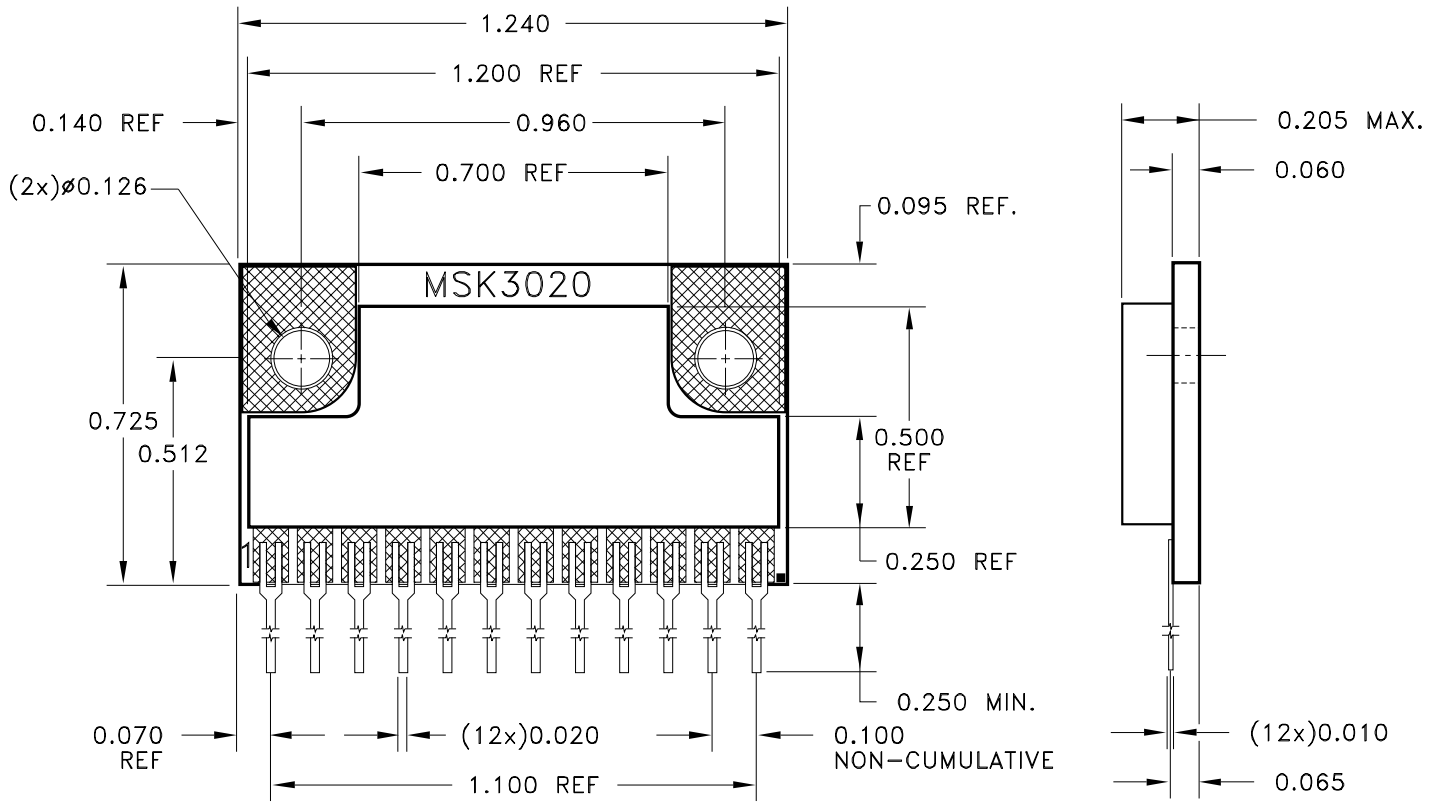


DRAIN CURRENT vs GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMP.





TORQUE SPECIFICATION 3 TO 5 IN/LBS. TEFLON SCREWS OR WASHERS ARE RECOMMENDED.

ALL DIMENSIONS ARE ±0.010 INCHES UNLESS OTHERWISE SPECIFIED.

ORDERING INFORMATION

PART NUMBER	SCREENING LEVEL
MSK 3020	Industrial

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