HIGH PERFORMANCE, HIGH VOLTAGE VIDEO DISPLAY DRIVER

645

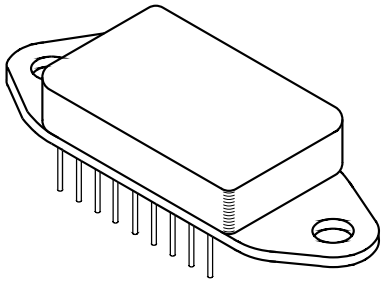
M.S.KENNEDY CORP.

4707 Dey Road Liverpool, N.Y. 13088 (315) 701-6751

MIL-PRF-38534 CERTIFIED

FEATURES:

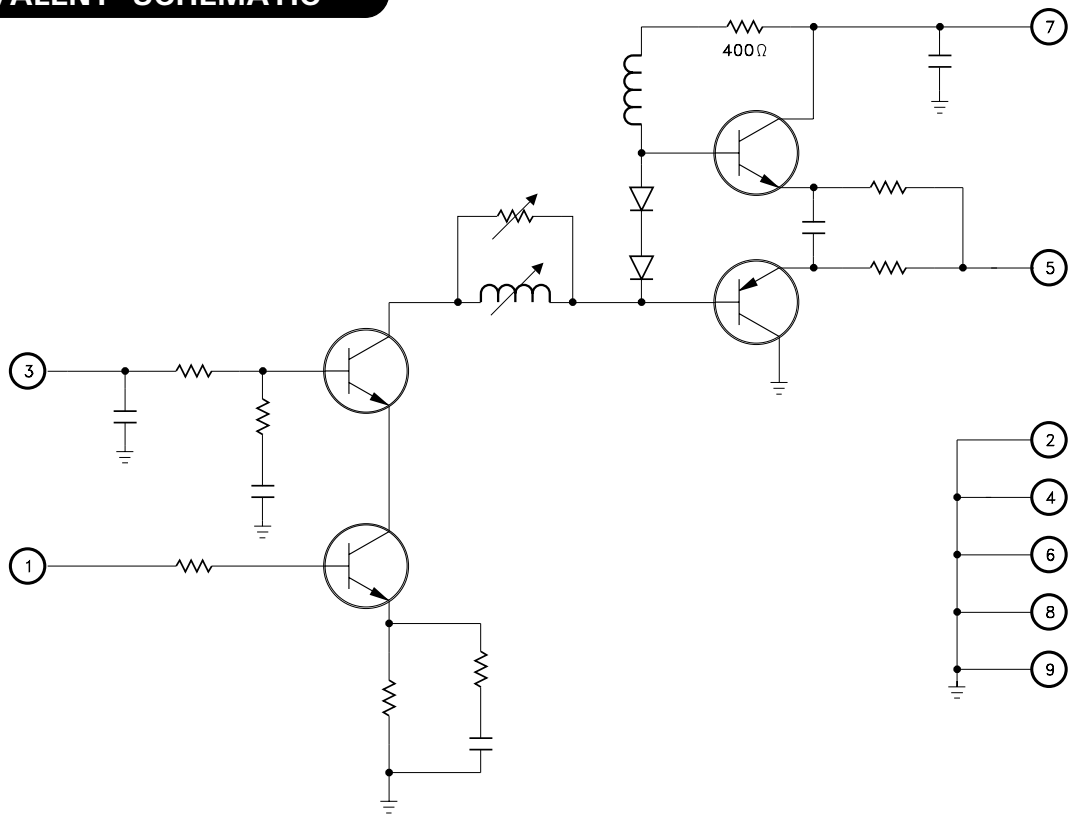
- 70 Vpp Output Voltage
- 150 MHz Typical Bandwidth
- Transition Times Typically <3.0 nS
- Cost and Space Efficient Package
- Electrically Isolated Case
- Gain Fixed Internally



DESCRIPTION:

The MSK 645 is an amplifier designed specifically to suit the needs of todays high resolution CRT display monitors. With a typical bandwidth of 150 MHz and transition times typically under 3.0nS the MSK 645 can easily drive monitors with resolutions of up to 1280 x 1024. The output can swing up to 70 Vpp and gain is internally set to minimize external component count. The MSK 645(B) is available screened to MIL-PRF-38534 and comes in a space efficient package that is electrically isolated from the internal circuitry and can be attached directly to a heat sink for efficient thermal dissipation.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- CRT Driver for SVGA
- Display Driver for Systems with up to 1280 x 1024 Display Resolution
- High Voltage Fixed Gain Amplifier

PIN-OUT INFORMATION

1	Video Input	6	Ground
2	Ground	7	$+V_{HV}$
3	V_{BIAS}	8	Ground
4	Ground	9	Ground
5	Video Output		

ABSOLUTE MAXIMUM RATINGS

$+V_{HV}$ High Voltage Supply . . . . . +90V
$+V_{IN}$ Input Voltage . . . . . ±5V
$+V_{BIAS}$ Bias Input Voltage . . . . . +10V
I_{OUT} Peak Output Current 200mA

T_{ST} Storage Temperature Range -65°C to +150°C
T_{LD} Lead Temperature Range . . . . . +300°C
(Solder 10 Seconds)
T_J Junction Temperature . . . . . +175°C
T_C Case Operating Temperature
MSK645 . . . . . -40°C to +85°C
MSK645(B) . . . . . -55°C to +125°C

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions ①	Group A Subgroup	MSK 645(B)			MSK 645			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS									
Quiescent Current (V_{HV})	V_{IN} = No Connect $R_L = \infty$	1,2,3	-	0.6	2.0	-	0.6	2.0	mA
Quiescent Current ($+V_{BIAS}$)	V_{IN} = No Connect $R_L = \infty$	1,2,3	-	0.01	0.5	-	0.01	0.5	mA
V_{HV} Power Supply Range		-	20	60	90	20	60	90	V
V_{BIAS} Power Supply Range		-	4	5	10	4	5	10	V
Video Input Voltage	V_{OUT} = +50VDC	1,2,3	0.5	0.85	1.2	0.4	0.85	1.3	V
Thermal Resistance (junction-to-case) ②	Output Stage	-	-	25	27	-	25	27	°C/W
DYNAMIC CHARACTERISTICS									
Video Output Voltage ⑥	High Level	4	50	59	-	50	59	-	V
	Low Level	4	-	5	10	-	5	10	V
Video Gain	F = 1MHz; V_{OUT} = +15Vto+45V	4	45	62	80	45	60	80	V/V
Video Gain Flatness ②	F = 10Hz to 60MHz; V_{OUT} = 30V_{PP}	-	-	±1.0	±2.0	-	±1.0	±3.0	dB
Video Output Rise/Fall Time	V_{OUT} = +15Vto+45V	4	-	3.0	4.0	-	3.0	5.0	nS
Video Output Overshoot ②	V_{OUT} = 10V_{PP} $V_{IN}T_R$ = 10nS	-	-	-	10	-	-	12	%
Bandwidth -3dB	C_L = 6.5pF	4	100	150	-	100	150	-	MHz

NOTES:

① $+V_{HV}$ = 60V; $+V_{BIAS}$ = 5V; R_L = 10KΩ; unless otherwise specified.
② Parameter is guaranteed by design but not tested. Typical specifications are representative of actual device performance at 25°C but are for reference only.
③ Military grade devices ('B' suffix) shall be 100% tested to subgroups 1,2,3 and 4.
④ Subgroup 5 and 6 testing available upon request.
⑤ Subgroup 1,4 $T_A = T_C = +25°C$
Subgroup 2,5 $T_A = T_C = +125°C$
Subgroup 3,6 $T_A = T_C = -55°C$
⑥ Refer to the video clip point curve on the Typical Performance Curves page.

APPLICATION NOTES

BLACK LEVEL CONTROL

Unlike many currently available video amplifiers, the MSK 645 is a D.C. coupled device. D.C. coupling affords the user direct black level control. A video input voltage of approximately 0.85 volts will set the output voltage to 50VDC (black level for $+V_{HV}$ = 60VDC). Black level control grants the user flexibility in the application of the amplifier. For example, the user could apply a 0.85VDC level to the video input to bias the output at the black level (approximately 50V for V_{HV} = 60V) and have input video information swing from 0.85 to 1.5V causing the output to swing from the black level towards white (zero). This configuration would dissipate the least amount of power and is most common. Another possible circuit configuration could be to D.C. bias the video input pin so that the output is at 1/2V_{HV}. The output video signal could then swing linearly from ($+V_{HV}$-10V) to (ground + 10V). Careful consideration must be paid to device power dissipation in this configuration since it will be very high.

VBIAS INPUT

The V_{BIAS} pin is connected to the base of the cascode transistor in the equivalent schematic. The purpose of the cascode transistor is to isolate the input transistor from the high voltage supply. The input transistor must have a very high transition frequency specification and this is difficult to find in high voltage transistors. By using the cascode transistor to relieve the input transistor of its high BVceo requirement, high speed, low breakdown transistors can be used. The voltage applied to pin three minus a base to emitter voltage drop of approximately 0.6 volts is the voltage present at the collector of the input transistor that acts as the voltage to current convertor. The voltage applied to the V_{BIAS} pin has a practical upper limit of 10.0 volts. Above 10.0 volts the device may not be able to reach white level without going into cutoff. The practical lower limit for this pin is approximately 2.0 volts. Below 2.0 volts the input transistor will be dangerously close to cutoff. The MSK 645 functions best with V_{BIAS} set to 5.0 volts ±1.0 volt.

OUTPUT CONSIDERATIONS

The output of the MSK 645 is driven by a complimentary push-pull buffer. The output stage isolates the capacitive load from the amplifier thereby making rising and falling edges relatively load independent. The bandwidth of the MSK 645 is limited by the RC time constant made up of the resistance from $+V_{HV}$ to the base of the NPN buffer and the capacitance from the NPN buffer base to ground. The coils in the equivalent schematic are chosen at the factory to moderately peak the amplifiers response (10%). For application specific user adjustable peaking, see the Typical Connection Circuit page.

OUTPUT PROTECTION

High voltage arcing can occur in the CRT being driven and cause severe damage to the MSK 645 output unless certain precautions are taken. The clamp diodes D1 and D2 (see figure 1) will keep the voltage at the output at a safe level. These diodes should have a low series resistance and shunt capacitance as well as a high surge rating (FDH400 is recommended). In the event of an arcover, Rb limits the current flowing through the clamp diode and Ra limits the current into the MSK 645 output. The recommended values shown in figure 1 should not be deviated from without checking the monitor performance since increasing these values will adversely affect transistion times.

POWER DISSIPATION

The most efficient method to reduce device power dissipation when using the MSK 645 is to fix the black level at a point as close to $+V_{HV}$ as possible and maintain the peak to peak video output voltage to as small an excursion as possible. The case of the MSK 645 is electrically isolated from internal circuitry and therefore the user should attach the heat sink directly to the case of the device.

HEAT SINK SELECTION

To calculate what size heat sink is needed for a particular application, the following formula must be used:

$$T_j = P_d (R_{\theta jc} + R_{\theta sa}) + T_a$$

where:
T_j = junction temperature = 150°C max.
$R_{\theta jc}$ = 27°C/W max.
T_a is the ambient temperature and P_d is the device power dissipation. $R_{\theta sa}$ is the heat sink thermal resistance.

EXAMPLE:
In an application an MSK 645 is dissipating 4 watts of power and the ambient temperature is +25°C. Plugging in all the known variables and rearranging the equation it can be seen that:

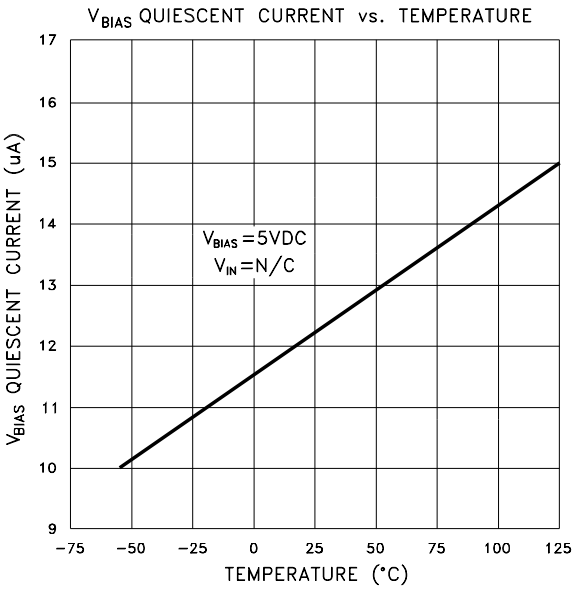
$$R_{\theta sa} = ((150°C - 25°C)/4W) - 27°C/W$$
$$= 4.2°C/W$$

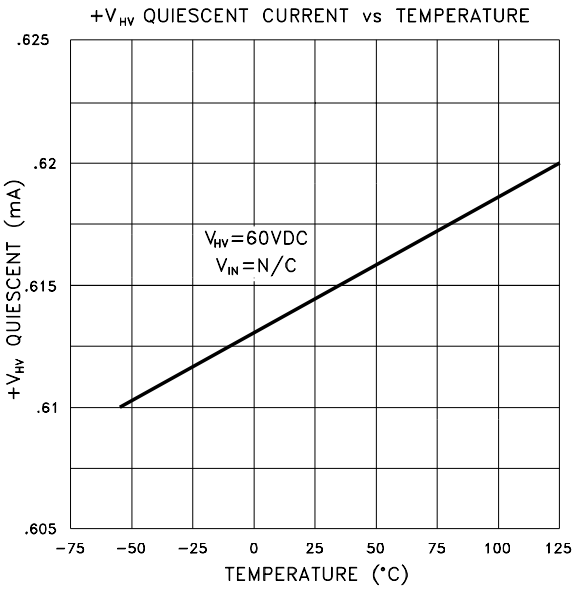
A heat sink with a thermal resistance of no more than 4.2°C/W must be used to maintain a junction temperature of 150°C max.

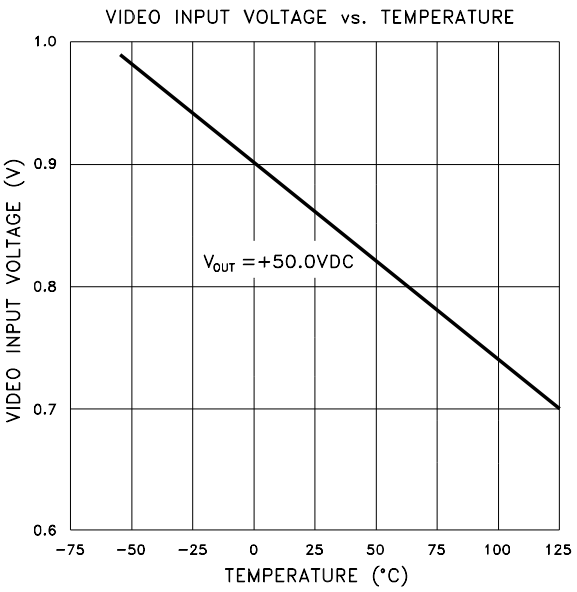
POWER SUPPLY DECOUPLING

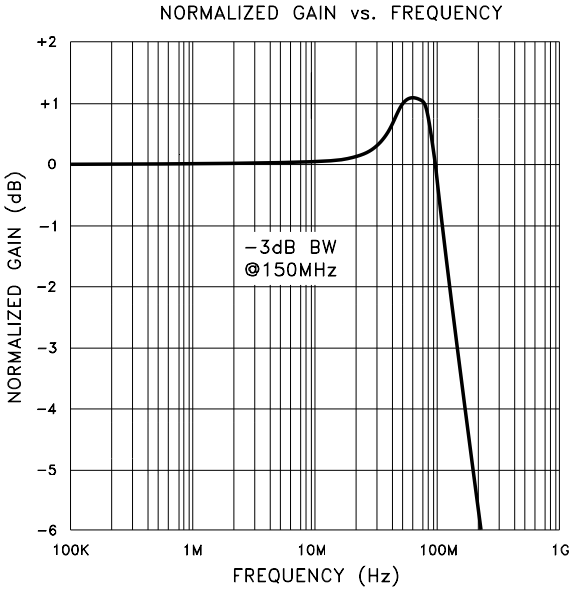
Both the $+V_{HV}$ and the V_{BIAS} input pins are decoupled internally with 0.1μF capacitors to contain line noise. However it is good practice to decouple the MSK 645 externally with at least a 4.7μF electrolytic capacitor placed as close as possible to the associated device pins.

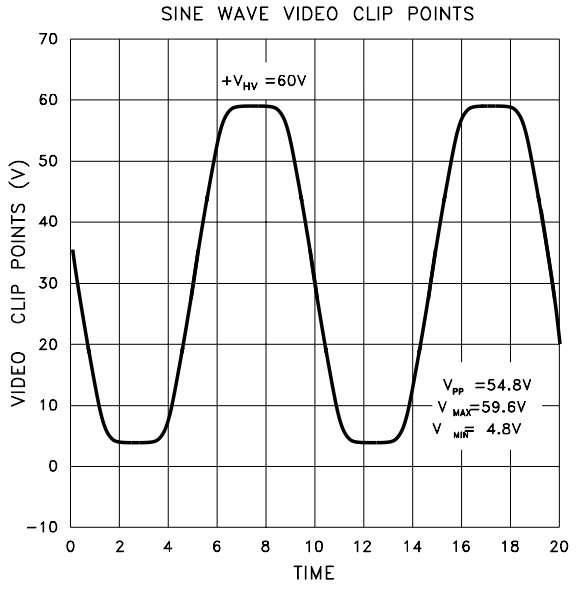
TYPICAL PERFORMANCE CURVES

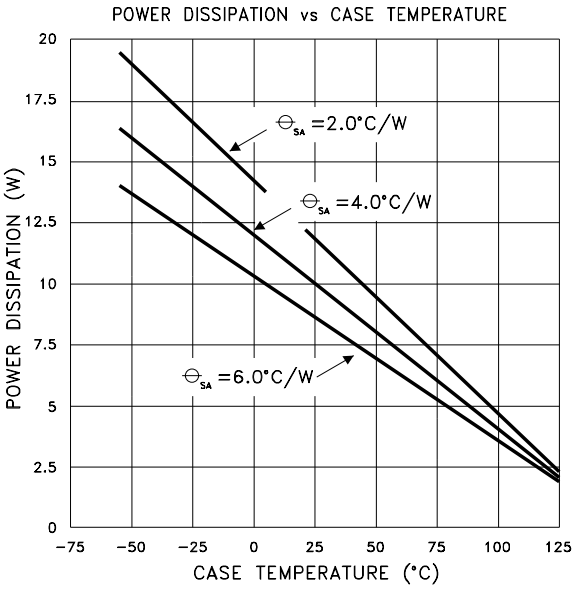












TYPICAL CONNECTION CIRCUIT

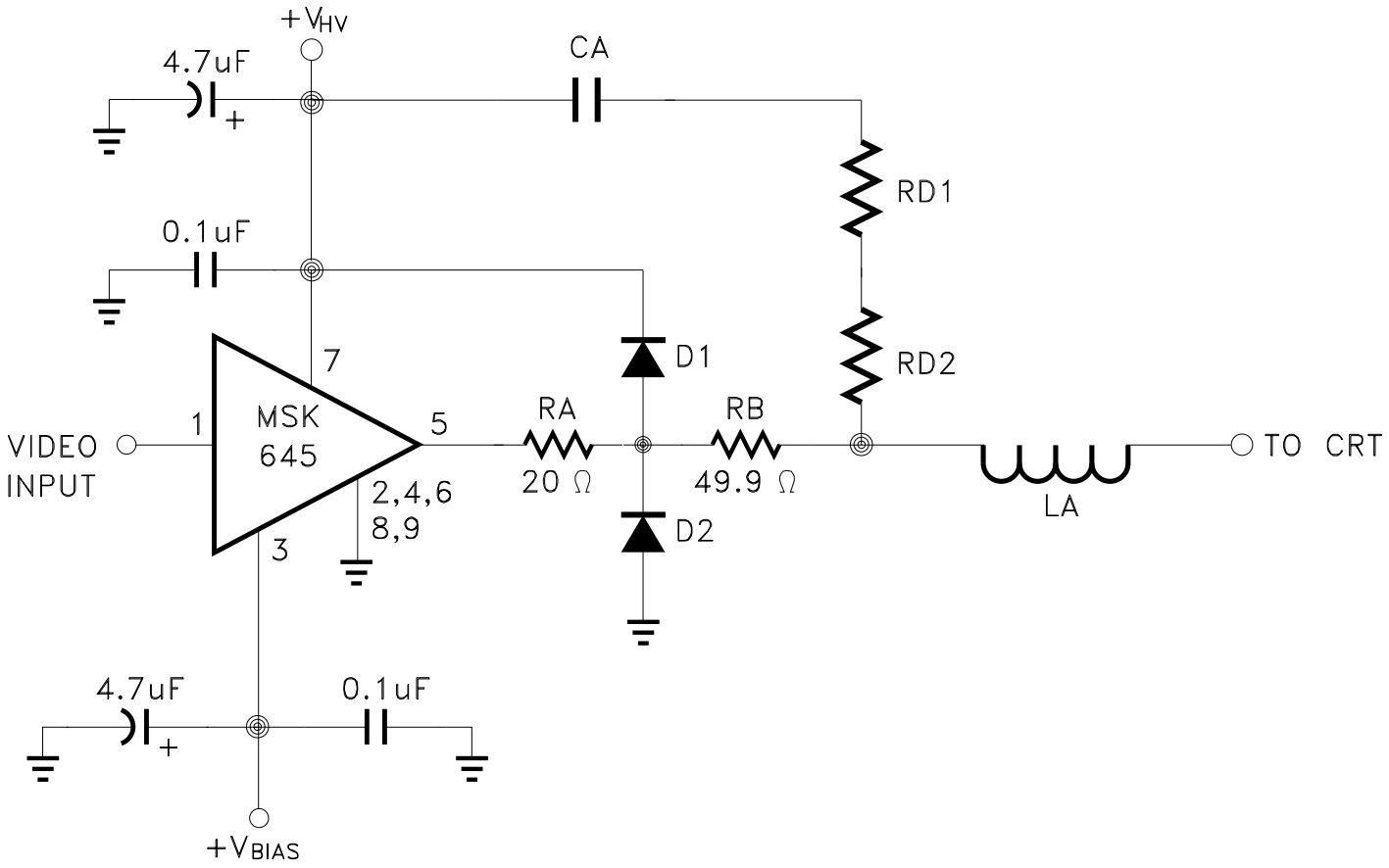
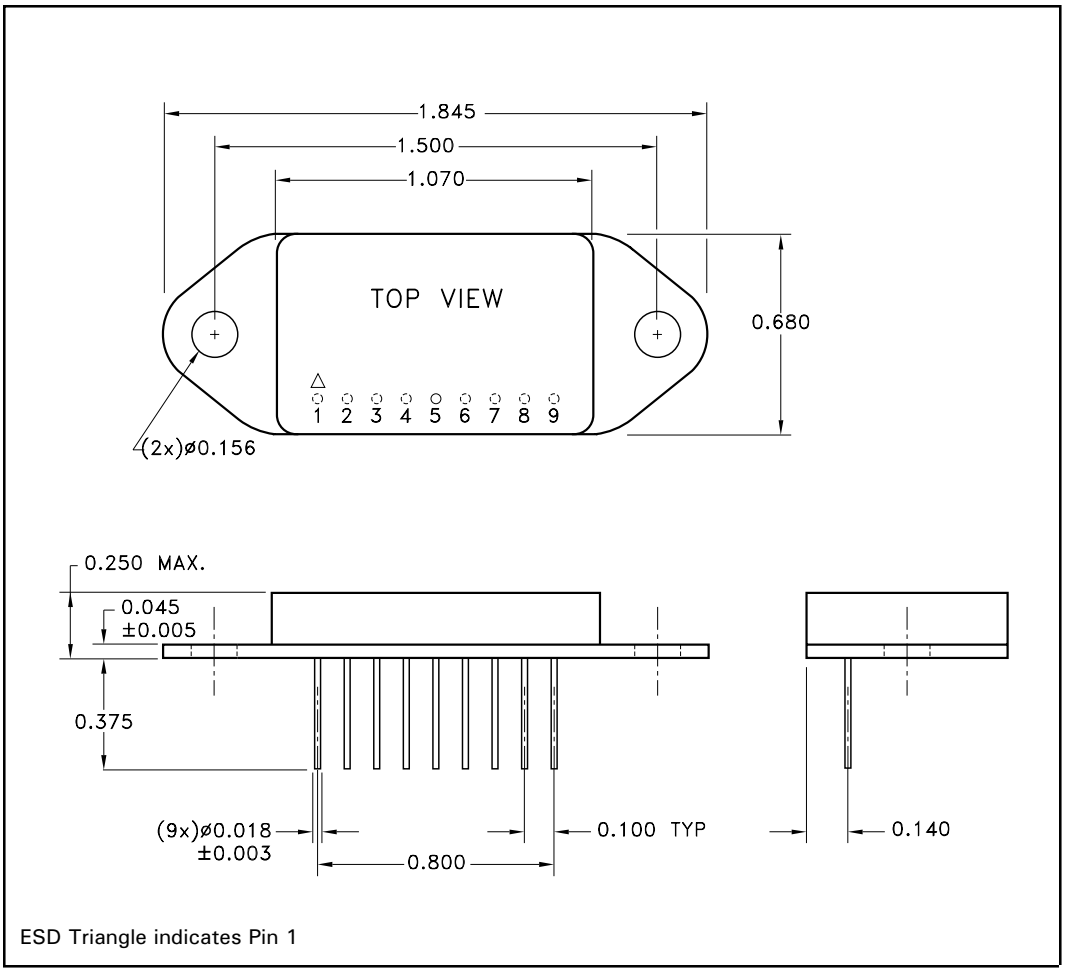


FIGURE 1

Transition time and overshoot adjustment is made possible using the circuit of Figure 1. LA peaks the amplifiers frequency response at the cathode yielding optimum rise and fall times. A good starting point value for this inductor is 0.1μH. The tradeoff that must be dealt with when peaking an amplifiers' response is increased overshoot. Once the rise and fall times have been adjusted with LA, the overshoot can be damped by adjusting CA, RD1 and RD2 in Figure 1. Keep in mind that as the value of load capacitance increases, so will the overshoot. Starting with 499Ω resistors for RD1 and RD2 and 150pF for CA, the overshoot can be minimized by adjusting RD1 and RD2 up or down.

NOTES:

MECHANICAL SPECIFICATIONS



ALL DIMENSIONS ARE ±0.010 INCHES UNLESS OTHERWISE LABELED

ORDERING INFORMATION

Part Number	Screening Level
MSK645	Industrial
MSK645(B)	Mil-PRF-38534

M.S. Kennedy Corp.
4707 Dey Road, Liverpool, New York 13088
Phone (315) 701-6751
FAX (315) 701-6752
www.mskennedy.com