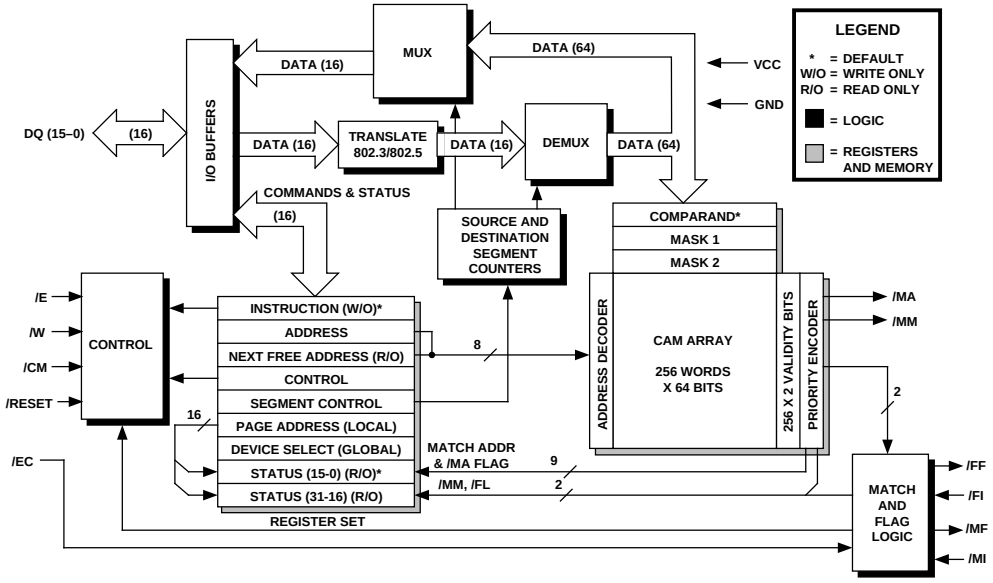
MU9C3480A
LANCAM®

PRELIMINARY DATA SHEET DRAFT

DISTINCTIVE CHARACTERISTICS

- **256 x 64-bit CMOS Content-addressable Memory (CAM) with 16-bit I/O for compatibility with the MU9C5480**
- **New faster compare speed of 70 ns.**
- **Dual configuration register set (Control, Segment Control, Mask Register 1, Address Register, and Persistent Source and Destination) for rapid context switching**
- **Shiftable Comparand and Mask Register 2 to assist in proximate matching algorithms**
- **Increased flexibility of the patented CAM/RAM partitioning**
- **Added /MA and /MM output flags to enable faster system performance**
- **Readable Device ID**
- **Selectable faster operating mode with no wait states after a no-match**
- **Validity bits of entries are stored in the Status register after a read or move from memory operation**
- **Single cycle reset for Segment Control register**
- **External Reset pin works in parallel to internal Power On Reset circuitry**
- **Packaged in an industry-standard 44-pin PLCC package to be socket compatible with the MU9C5480A, MU9C1480A and MU9C2480A.**
- **Low power off a 5 volt supply**

BLOCK DIAGRAM



GENERAL DESCRIPTION

The MU9C3480A LANCAM is a 256 x 64-bit Content-addressable Memory (CAM), designed for address filtering applications in Local-area Network (LAN) bridges and routers. The architecture of the LANCAM allows a network station list of any length to be searched in a single memory transaction. This device is also well-suited for other high-speed data search applications such as virtual memories, optical and magnetic disk caches, data base accelerators, data compressors, and image processors.

Content-addressable Memories, also known as Associative Memories, operate in the converse way to Random Access Memories. In a RAM, the input to the device is an address, and the output is the data stored at that address. In a CAM, the input is a data sample and the output is a flag to indicate a match and the address of the matching data. As a result, a CAM searches large data bases for matching data in a short, constant time period, no matter how many entries are in the data base. The ability to search data words up to 64 bits wide allows large address spaces to be searched rapidly and efficiently. A patented architecture links each CAM entry to associated data and makes this data available for use after a successful compare operation.

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MUSIC is a trademark of MUSIC Semiconductors. Certain features of this device are patented under US Patent 5,383,146.

MU9C3480A
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OPERATIONAL OVERVIEW

To use the LANCAM, the user loads the data into the Comparand register, which is automatically compared to all valid CAM locations. The device then indicates whether or not one or more of the valid CAM locations contains data that matches the target data. The status of each CAM location is determined by two validity bits at each memory location. The two bits are encoded to render four validity conditions: Valid, Skip, Empty, and Random Access. The memory can be partitioned into CAM and associated RAM segments on 16-bit boundaries. By using one of the two available mask registers, the CAM/RAM partitioning can effectively be set at any arbitrary size between zero and 64 bits.

The MU9C3480A LANCAM's internal data path is 64 bits wide for rapid internal comparison and data movement. A data translation facility converts between IEEE 802.3 (CSMA/CD "Ethernet") and 802.5 (Token Ring) address formats. Vertical cascading of additional LANCAMs in a daisy-chain fashion extends the CAM memory depth for large data bases. Cascading requires no external logic. Loading data to the Control, Comparand a mask registers automatically triggers a compare, and compares may also be initiated by a command to the device. Associated RAM data is available immediately after a successful compare operation. The Status register reports the results of compares including all flags and addresses. Two mask registers are available and can be used in two different ways: to mask comparisons or to mask data writes. The random access validity flag allows additional masks to be stored in the CAM array where they may be retrieved rapidly.

The device is controlled by a simple four-wire control interface and commands loaded into the Instruction decoder. A powerful instruction set increases the control flexibility and minimizes software overhead. Additionally, dedicated pins for match and multiple-match flags enhance performance when the device is controlled by a state machine. These and other features make the LANCAM a powerful associative memory that drastically reduces search delays.

Skip Bit	Empty Bit	Entry Type
0	0	Valid
0	1	Empty
1	0	Skip
1	1	RAM

Table 1: Entry Types vs. Validity Bits

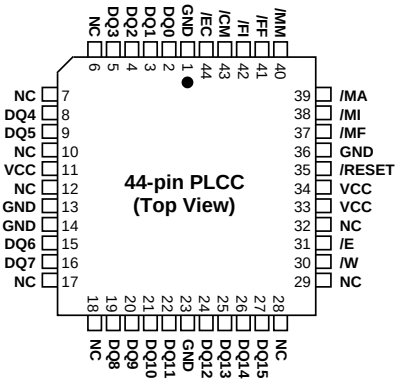


Figure 1: Pinout Diagram

PIN DESCRIPTIONS

All signals are implemented in CMOS technology with TTL levels. Signal names that start with a slash ("/") are active LOW. Inputs (except for the RESET pin) should never be left floating. The CAM architecture draws large currents during compare operations, mandating the use of good layout and bypassing techniques. Refer to the Electrical Characteristics section for more information.

DQ15-DQ0 (Data Bus, I/O, Three-state TTL)

The DQ15-DQ0 lines convey data, commands and status to and from the MU9C3480A. The direction and nature of the information that flows to or from the device is controlled by the states of /W and /CM, respectively. When /E is HIGH, DQ15-DQ0 go to Hi-Z.

/E (Chip Enable, Input, TTL)

The /E input enables the device while LOW. The falling edge registers the control signals /W, /CM, /EC. The rising edge locks the daisy chain, turns off the DQ pins, and clocks the Destination and Source Segment counters. The four cycle types enabled by /E are shown in Table 2.

PIN DESCRIPTIONS (CONT'D)

/W (Write Enable, Input, TTL)

The /W input selects the direction of data flow during a device cycle. /W LOW selects a Write cycle, and /W HIGH selects a Read cycle.

/CM (Data/Command Select, Input, TTL)

The /CM input selects whether the input signals on DQ15-DQ0 are data or commands. /CM LOW selects Command cycles, and /CM HIGH selects Data cycles.

/EC (Enable Daisy Chain, Input, TTL)

The /EC signal performs two functions. The /EC input enables the /MF output to show the results of a comparison. If /EC is LOW at the falling edge of /E in a given cycle, the /MF output is enabled. Otherwise, the /MF output is held HIGH. The /EC signal also enables the /MF-/MI daisy-chain, which serves to select the device with the highest-priority match in a string of LANCAMs. Tables 8a and 8b explain the effect of the /EC signal on a device with and without a match in both the 1480 and 2480 modes. /EC must be HIGH during initialization.

/MF (Match Flag, Output, TTL)

The /MF output goes LOW when one or more valid matches occur during a compare cycle. /MF becomes valid after /E goes HIGH on the cycle that enables the daisy chain (the first cycle that /EC is registered LOW by the previous falling edge of /E; see Figure 6). In a daisy-chain, valid match(es) in higher priority devices are passed from the /MI input to /MF. If the daisy chain is enabled but the match flag is disabled in the control register, the /MF output only depends on the /MI input of the device (/MF=/MI). /MF is HIGH if there is no match or when the daisy chain is disabled (/E goes HIGH when /EC was HIGH on the previous falling edge of /E). The System Match flag is the /MF pin of the last device in the daisy-chain. /MF will be reset when the active configuration register set is changed.

/MI (Match Input, Input, TTL)

The /MI input prioritizes devices in vertically cascaded systems. It is connected to the /MF output of the previous (next higher-priority) device in the daisy chain. The /MI pin on the highest priority device must be tied HIGH.

/W	/CM	Cycle Type
LOW	LOW	Command Write Cycle
LOW	HIGH	Data Write Cycle
HIGH	LOW	Command Read Cycle
HIGH	HIGH	Data Read Cycle

Table 2: I/O Cycles

/MA (Device Match Flag, Output, TTL)

The /MA output is LOW when one or more valid matches occur during the current or the last previous compare cycle. The /MA output is not qualified by /EC or /MI, and reflects the match flag from that specific device's Status register. /MA will be reset when the active register set is changed.

/MM (Device Multiple Match Flag, Output, TTL)

The /MM output is LOW when more than one valid match occurs during the current or the last previous compare cycle. The /MM output is not qualified by /EC or /MI, and reflects the multiple match flag from that specific device's Status register. /MM will be reset when the active register set is changed.

/FF (Full Flag, Output, TTL)

If enabled in the control register, the /FF output goes LOW when no empty memory locations exist within the device (and in the daisy-chain above the device as indicated by the /FI pin). The System Full flag is the /FF pin of the last device in the daisy chain, and the Next Free address resides in the device with /FI LOW and /FF HIGH. If disabled in the control register, the /FF output only depends on the /FI input (/FF = /FI).

/FI (Full Input, Input, TTL)

The /FI input generates a CAM-Memory-System-Full indication in vertically cascaded systems. It is connected to the /FF output of the previous (next-higher priority) device in the daisy chain. The /FI pin on the highest priority device must be tied LOW.

/RESET (Reset, Input, TTL)

Driving the /RESET pin LOW resets the device to the conditions shown in Table 5. The hardware reset operates in parallel with the internal Power-on-reset circuitry, which sets the device to the same conditions. For compatibility with the MU9C5480, the /RESET pin has an internal pull-up resistor and may be left unconnected. The /RESET pin should be driven by TTL levels, not directly by an RC timeout. /E must be kept HIGH during /RESET.

VCC, GND (Positive Power Supply, Ground)

These pins are the power supply connections to the MU9C3480A. VCC must meet the requirements in the Operating Conditions section relative to the GND pins, which are at 0 Volts (system reference potential), for correct operation of the device. The ground connections on pins 1 and 23 are connected to the internal ground system and may be left unconnected for compatibility with existing MU9C5480 layouts; however, they must be connected to the ground plane for 70ns performance.

FUNCTIONAL DESCRIPTION

The MU9C3480A LANCAM is a 256 x 64-bit Content-addressable Memory (CAM) for network address filtering, virtual memory, data compression, cache, and table look-up applications. The MU9C3480A contains 16,384 (16K) usable bits of static CAM, organized as 256 64-bit Data fields. Each Data field can be partitioned into a CAM and a RAM subfield on 16-bit boundaries. The contents of the memory can be randomly accessed or associatively accessed by the use of a compare. During automatic Comparison cycles, data in the Comparand register is automatically compared with the "Valid" CAM section of the memory array. The device ID of 341H can be read using a TCO PS instruction.

The data inputs and outputs of the MU9C3480A LANCAM are multiplexed for data and instructions over a 16-bit I/O bus. Internally, data is handled on a 64-bit basis, since the Comparand register, the Mask registers, and each memory entry is 64 bits wide. Memory entries are globally configurable into CAM and RAM segments on 16-bit boundaries, as described in US Patent 5,383,146 assigned to MUSIC Semiconductors. Seven different CAM/RAM splits are possible, with the CAM width going from one to four segments, and the remaining RAM width going from three to zero segments. Finer resolution on compare width is possible by invoking a Mask register during a compare, which does global masking on a bit basis. The CAM subfield contains the Associative data which enters into Compares, while the RAM subfield contains the Associated data which is not compared. In LAN Bridges, the RAM subfield could hold, for example, port-address and aging information related to the destination or source address information held in the CAM subfield of a given location. In a translation application, the CAM field could hold the dictionary entries, while the RAM field holds the translations, with almost instantaneous response.

Each entry has two validity bits (known as Skip bit and Empty bit) associated with it to define its particular type: Empty, Valid, Skip, or RAM. When data is written to the active Comparand register and the active Segment Control register reaches its terminal count, the contents of the Comparand register are automatically compared with the CAM portion of all the Valid entries in the memory array. For added versatility, the Comparand register can be barrel-shifted right or left one bit at a time. A Compare instruction can then be used to force another compare between the Comparand register and the CAM portion of memory entries of any one of the four validity types. After a Read or Move from Memory operation, the validity bits of the location read or moved will be copied into the Status register, where they can be read from the Status register using Command Read cycles.

Data can be moved from one of the data registers (CR, MR1, or MR2) to a memory location that is based on the results of the last comparison (Highest Priority Match or Next free), or to an absolute address, or to the location pointed to by the active Address register. Data can also be written directly to the memory from the DQ bus using any of the above addressing modes, with the Address register directly loaded or set to increment or decrement, allowing DMA-type reading or writing from memory.

Two sets of configuration registers (Control, Segment Control, Address, Mask Register 1, and the Persistent Source and Destination) are provided to permit rapid context switching between foreground and background activities. Writes, reads, moves and compares are controlled by the currently active set of configuration registers. The foreground set would typically be pre-loaded with values useful for comparing input data, often called filtering, while the background set would be pre-loaded with values useful for housekeeping activities such as purging old entries. Moving from the foreground task of filtering to the background task of purging can be done by issuing a single instruction to change the current set of configuration registers. The match condition of the device is reset whenever the active register set is changed.

The active Control register determines the operating conditions within the device. Conditions set by this register's contents are Reset, enable or disable Match flag, enable or disable Full flag, default data translation, CAM/RAM partitioning, disable or select masking conditions, disable or select auto-incrementing or -decrementing the Address register, and to set 1480-compatible or 2480-enhanced modes. The active Segment Control register contains separate counters to control the writing of 16-bit data segments to the selected persistent destination, and to control the reading of 16-bit data segments from the selected persistent source.

There are two active Mask registers at any one time, which can be selected to mask comparisons or data writes. Mask Register 1 has both a foreground and background mode to support rapid context switching. Mask Register 2 does not have this mode, but can be shifted left or right one bit at a time. For masking comparisons, data stored in the active selected Mask register determines which bits of the Comparand are compared against the valid contents of the Memory. If a bit is set HIGH in the Mask register, the same bit position in the Comparand register becomes a "don't care" for the purpose of the comparison with all the memory locations. During a Write cycle, data in the selected active Mask register can also determine which bits in the destination will be updated. If a bit is HIGH in the Mask register, the corresponding bit of the destination is unchanged during the Write cycle.

The Match line associated with each memory address is fed into a Priority encoder where multiple responses

FUNCTIONAL DESCRIPTION (CONT'D)

are resolved, and the address of the highest-priority responder (the lowest numerical match address) is generated. In the LAN Bridge application, a multiple response might indicate an error. In other applications the existence of multiple responders may be valid.

Control of these devices is via four input control signals and by commands loaded into an Instruction decoder. Two of the four input control signals determine the cycle type. The control signals tell the device whether the data on the I/O bus represents Data or a Command, and is Input or Output. Commands are decoded by Instruction logic and control moves, forced compares, validity bit manipulations, and the data path within the device. Registers (Control, Segment Control, Address, Next Free Address, etc.) are accessed using Temporary Command Override instructions. The data path from the DQ bus to/from data resources (Comparand, Masks, and Memory) within the device are set until changed by Select Persistent Source and Destination instructions.

After a Compare cycle caused by either a Data Write to the Comparand or Mask registers or a forced Compare, the Status register contains the address of the Highest Priority Matching location in that device, concatenated with its Page Address, along with flags indicating internal Match, Multiple Match, and Full. When the Status register is read with a Command Read cycle, the device with the Highest Priority match will respond, outputting the System Match Address to the DQ bus. The internal Match (/MA) and Multiple match (/MM) flags are also output on pins. Another set of flags (/MF and /FF) that are qualified by the match and full flags of previous devices in the system are also available directly on output pins, and are independently daisy-chained to provide System Match and Full flags in vertically cascaded LANCAM arrays. In such arrays, if no match occurs during a comparison, read access to the memory, and all the registers except the Next Free Register, is denied to prevent device contention. In a daisy chain, all devices will respond to Command and Data Writes, depending on the conditions shown in Tables 8a and 8b, unless the operation involves the Highest Priority Match address or the Next Free Address; in which case, only the specific device having the Highest Priority Match or the Next Free Address will respond.

A Page Address register in each device simplifies vertical expansion in systems using more than one LANCAM. This register is loaded with a specific device address during system initialization, which then serves as the higher-order address bits. A Device Select register allows the user to target a specific device within a vertically cascaded system by setting it equal to the Page Address register value, or to address all the devices in a string at the same time by setting the Device Select value to FFFFH.

Figure 2a shows expansion using a daisy-chain. Note that system flags are generated without the need for external logic. The Page Address register allows each device in the vertically cascaded chain to supply its own address in the event of a match eliminating the need for an external Priority encoder to calculate the complete Match address at the expense of the ripple-through time to resolve the Highest-priority match. The Full flag daisy-chaining allows Associative writes using a Move to Next Free Address instruction which does not need a supplied address.

Figure 2b shows an external PLD implementation of a simple priority encoder to resolve the Highest-priority match and gate the /E signal to each device for systems requiring maximum performance.

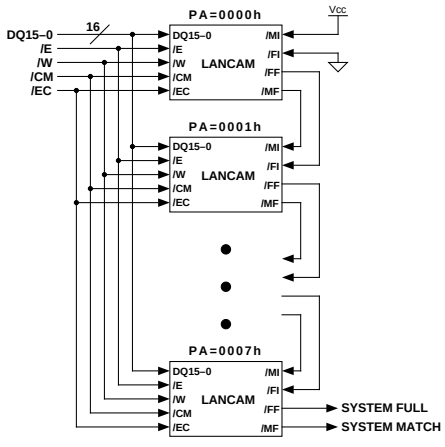


Figure 2a: Vertical Cascading

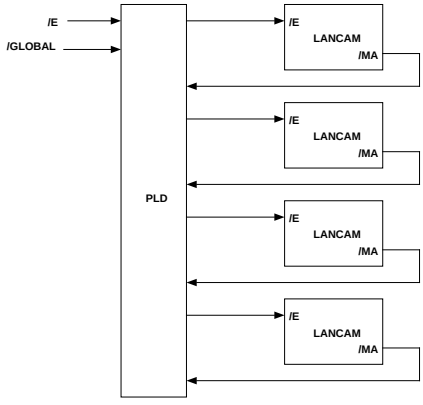


Figure 2b: External Prioritizing

OPERATIONAL CHARACTERISTICS

Throughout the following, "aaaH" represents a three-digit hexadecimal number "aaa," while "bbB" represents a two-digit binary number "bb." All memory locations are broken into 16-bit segments. Segment 0 corresponds with the lowest order bits (bits 15-0) while the higher segments, labeled 1, 2, and 3, contain bits 31-16, 47-32 and 63-48, respectively.

THE CONTROL BUS

Refer to the Block Diagram for the following discussion. The primary control mechanism for the MU9C3480A are the input signals Chip Enable (/E), Write Enable (/W), Command Enable (/CM), and Enable Daisy Chain (/EC). The /EC input of the Control bus is responsible for enabling the /MF Match flag output when LOW, and controlling the daisy-chain operation. The secondary control mechanism of the MU9C3480A is by instructions which are decoded by the Instruction decoder. Logical combinations of the Control Bus inputs, coupled with the execution of Select Persistent Source (SPS), Select Persistent Destination (SPD), and Temporary Command Override (TCO) instructions, allow the I/O operations to and from the DQ15-DQ0 lines to the internal resources, as shown in Table 3.

The default source and destination for Data Read and Write cycles is the Comparand register. This default state can be overridden independently by executing a Select Persistent Source or Select Persistent Destination instruction, selecting a different source or destination for data. Subsequent Data Read or Data Write cycles will access that source or destination until another SPS or SPD instruction is executed. The currently selected persistent source or destination can be read back via a TCO PS or PD instruction. The sources and destinations available for persistent access are those resources on the 64-bit bus: Comparand register, Mask Register 1, Mask Register 2, and the Memory array.

The default destination for Command Write cycles is the Instruction decoder, while the default source for Command Read cycles is the Status register.

Access to the Control register, the Page Address register, the Segment Control register, the Address register, the Next Free Address register, and Device Select register is by Temporary Command Override (TCO) instructions which are only active for one Command Read or Write cycle after being loaded into the Instruction decoder.

The data and control interfaces to the MU9C3480A are synchronous. During a Write cycle, the Control and Data inputs are registered by the falling edge of /E. When writing to the persistently selected data destination, the Destination Segment counter is clocked by the rising edge of /E. During a Read cycle, the Control inputs are registered by the falling edge of /E, and the Data outputs are enabled while /E is LOW. When reading from the persistently selected data source, the Source Segment counter is clocked by the rising edge of /E.

THE REGISTER SET

The Control, Segment Control, Address, Mask Register 1, and the Persistent Source and Destination registers are duplicated, with one set termed the Foreground set, and the other the Background set. The active set is chosen by issuing Set Foreground Active or Set Background Active instructions. By default, the Foreground set is active after a power-up or Reset. Having two alternate sets of registers that determine the device configuration allows for a rapid return to a foreground network filtering task from a background housekeeping task.

Writing a value to the Control register or writing data to the last segment of the Comparand or either Mask register will cause an automatic comparison to occur between the contents of the Comparand register and the words in the CAM segments of the memory marked valid, masked by MR1 or MR2 if selected in the Control register.

Instruction Decoder

The Instruction decoder is the write-only decode logic for instructions and is the default destination for Command Write cycles. The lower-order 12 bits comprise the instruction, as shown in the Instruction Set Description. Bit 11 is a flag that notifies the LANCAM that the instruction is a two-cycle instruction and requires an absolute address to be loaded into the Address register on the next cycle. If the Address flag is not set, the memory access occurs at the address currently contained in the Address register.

Control Register (CT)

The Control register is composed of a number of switches that configure the LANCAM, as shown in Table 4, and is written to or read from using a TCO CT instruction. If bit 15 of the value written following the TCO CT is a "0", the device is Reset (and all other bits are ignored.) See Table 5 for the reset state. A write to the Control register causes an automatic compare to occur (except in case of a Reset.) Either the Foreground or Background Control register will be active, depending on which has been selected, and only the active Control register will be written to or read.

If the Match Flag is disabled via bits 14 and 13, the internal match condition, /MA(int), used to determine a daisy-chained device's response, is forced HIGH as shown in Tables 8a and 8b, so that Case 6 is not possible, effectively removing the device from the

OPERATIONAL CHARACTERISTICS (CONT'D)

CycleType	/E	/CM	/W	I/O Status	SPS	SPD	TCO	Operation	Notes
Com Write	L	L	L	IN				Load Instruction decoder	1
				IN			√	Load Address register	2, 3
				IN			√	Load Control register	3
				IN			√	Load Page Address register	3
				IN			√	Load Segment Control register	3
				IN			√	Load Device Select register	3
				IN				Deselected	10
Com Read	L	L	H	OUT			√	Read Next Free Address register	3
				OUT			√	Read Address register	3
				OUT				Read Status Register bits 15-0	4
				OUT				Read Status Register bits 31-16	5
				OUT			√	Read Control Register	3
				OUT			√	Read Page Address Register	3
				OUT			√	Read Segment Control Register	3
				OUT			√	Read Device Select Register	3
				OUT			√	Read Current Persistent Source or Destination	3,11
				HIGH-Z				Deselected	10
Data Write	L	H	L	IN		√		Load Comparand Register	6, 9
				IN		√		Load Mask Register 1	7, 9
				IN		√		Load Mask Register 2	7, 9
				IN		√		Write Memory Array at Address	7,9
				IN		√		Write Memory Array at Next Free Address	7, 9
				IN		√		Write Memory Array at Highest-priority Match	7, 9
				IN				Deselected	10
Data Read	L	H	H	OUT	√			Read Comparand Register	6, 9
				OUT	√			Read Mask Register 1	8,9
				OUT	√			Read Mask Register 2	8,9
				OUT	√			Read Memory Array at Address	8,9
				OUT	√			Read Memory Array at Highest-priority Match	8,9
				HIGH-Z				Deselected	10
	H	X	X	HIGH-Z				Deselected	

Notes

1. Default Command Write cycle destination (does not require a TCO instruction).
2. Default Command Write Cycle destination (no TCO instruction required) if Address flag was set in bit IR11 of the instruction loaded in the previous cycle.
3. Loaded or read on the consecutive Command Write or Read cycle after a TCO instruction has been loaded. Active for one Command Write or Read cycle only. NFA register cannot be loaded this way.
4. Default Command Read cycle source (does not require a TCO instruction).
5. Default Command read cycle source (no //tco instruction required) if the previous cycle was a Command /read of status register bits 15-0. If next cycle is not a Command Read cycle, any subsequent Command Read cycle will access the Status register bits 15-0.
6. Default persistent source and destination on power-up and after Reset. If other resources were sources or destinations, SPD CR or SPS CR restores the Comparand register as the destination or source.
7. Selected by executing a Select Persistent Destination Instruction.
8. Selected by executing a Select Persistent Source Instruction.
9. Access may require multiple 16-bit Read or Write cycles. The Segment Control register is used to control the selection of the desired 16-bit segment(s) by establishing the Segment counters' limits and start values.
10. Device is deselected if Device Select register setting does not equal Page Address register setting, unless the Device Select register is set to FFFFH which allows only write access to the device. (Writes to the Device Select register are always active.) Device may also be deselected under locked daisy-chain conditions as shown in Tables 8a and 8b.
11. A Command Read cycle after a TCO PS or TCO PD read back the Instruction decoder bits that were last set to select a persistant source or destination.

Table 3: Input/Output Operations

OPERATIONAL CHARACTERISTICS (CONT'D)

15	14 13	12 11	10 9	8 7 6	5 4	3 2	1 0
RST	Match Flag	Full Flag	Translation	CAM/RAM Part.	Comp. Mask	AR Inc/Dec	Mode
R E S E T = "0"	Enable = "00" Disable = "01" No Change = "11"	Enable = "00" Disable = "01" No Change = "11"	Input Not Translated = "00" Input Translated = "01" No Change = "11"	64 CAM/0 RAM = "000" 48 CAM/16 RAM = "001" 32 CAM/32 RAM = "010" 16 CAM/48 RAM = "011" 48 RAM/16 CAM = "100" 32 RAM/32 CAM = "101" 16 RAM/48 CAM = "110" No Change = "111"	None = "00" MR1 = "01" MR2 = "10" No Change = "11"	Increment = "00" Decrement = "01" Disable = "10" No Change = "11"	1480 Mode = "00" 2480 Mode = "01" Reserved = "10" No Change = "11"

Table 4: Control Register Bit Assignments

CAM Status	After /RESET or POR	Software Reset
Validity bits at all memory locations	Skip = 0, Empty = 1	Same
Match and Full Flag outputs	Enabled	Same
IEEE 802.3-802.5 Input Translation	Not Translated	Same
CAM/RAM Partitioning	64 bits CAM, 0 bits RAM	Same
Comparison Masking	Disabled	Same
Address register auto-increment or -decrement	Disabled	Same
Source and Destination Segment Counters Count Ranges	00B to 11B; loaded with 00B	Same
Address register and Next Free Address register	Contains all "0"s	Same
Page Address and Device Select registers	Contain all "0"s	Unchanged
Control register after reset (Including CT15)	Contains 0008H	Same
Persistent Destination for Command Writes	Instruction decoder	Same
Persistent Source for Command Reads	Status register	Same
Persistent Source and Destination for Data Reads and Writes	Comparand register	Same
Operating Mode	1480	Same
Configuration Register Set	Foreground	Same

Table 5: Device Control State after Reset

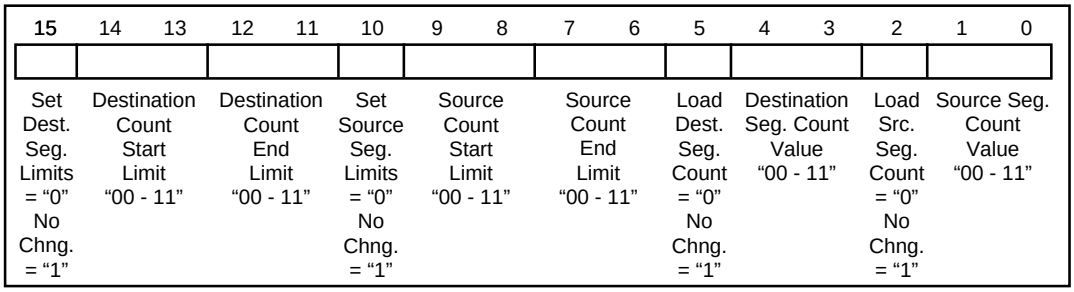
daisy-chain. With the Match Flag disabled, /MF=/MI, and operations directed to Highest-priority Match locations are ignored. Normal operation of the device is with the /MF enabled. The Match Flag Enable field has no effect on the /MA or /MM bits in the Status register. These bits always reflect the true state of the device.

If the Full Flag is disabled via bits 12 and 11, the device behaves as if it is full and ignores instructions to Next Free Address. Additionally, writes to the Page Address register will be disabled. All other instructions operate normally. Additionally, with the /FF disabled, /FF=/FI. Normal operation of the device is with the /FF enabled. The Full Flag Enable field has no effect on the /FL Status register bit. This bit always reflects the true state of the device.

The IEEE Translation control at bits 10 and 9 can be used to enable the translation hardware for writes to 64-bit resources in the device. When translation is enabled, the bits are reordered as shown in Figure 7. The CAM/RAM partitioning is controlled at bits 8-6, and may be set in 16-bit increments. The CAM portion of each word may be sized from a full 64 bits down to 16 bits. The RAM portion can be at either end of the 64-bit word.

Compare masks may be selected by bits 5 and 4. Mask Register 1, Mask Register 2, or neither may be selected to mask compare operations. The address register behavior is controlled by bits 3 and 2, and may be set to increment, decrement or neither after a memory access. Bits 1 and 0 set the operating mode: 1480-compatible as shown in Table 8a, or 2480-compatible as shown in Table 8b. The device powers up in the 1480 mode, following the 1480 operating responses in Table 8a. When switched to the 2480 mode, a NOP is not required to unlock the daisy chain after a non-matching compare, as in the 1480 mode.

OPERATIONAL CHARACTERISTICS (CONT'D)



Note: D15, D10, D5, and D2 read back as "0"s.

Table 6: Segment Control Register Bit Assignments

Segment Control Register (SC)

The Segment Control register contains dual independent incrementing counters with limits; one for data reads and one for data writes. These counters control which 16-bit segment of the 64-bit internal resource is accessed during a particular data cycle on the 16-bit data bus. The actual destination for data writes and source for data reads (called the persistent destination and source) are set independently with SPD and SPS instructions, respectively. Either the Foreground or Background Segment Control Register will be active, depending on which has been selected, and only the active Segment Control Register can be written to or read from.

Each of the two counters consists of a start segment, the end segment, and the current segment pointer. The current segment pointer can be set to any segment even if its a segment outside the range set by the start and end segments. If a sequence of data writes or reads is interrupted, the Segment Control register can be reset to its inital start limits values using an RSC instruction. A TCO SC instruction writes a configuration value to the Segment Control register, as shown in Table 6. After a Reset, both Source and Destination counters are set to count from Segment 0 to Segment 3 with an initial value of 0. D15, D10, D5 and D2 always read back as "0"s.

Page Address Register (PA)

The Page Address register is loaded by the user during initialization with a TCO PA instruction followed by a 16-bit value (not FFFFH) which gives a unique address to the different devices in a daisy-chain. In a daisy-chain, the PA value of each device is loaded followed by an SFF instruction to advance to the next device as shown in the "Setting Page Address Register Values" section. The Page Address register can be read from the Status register. The lower five bits also appear in the Next Free Address register. A software Reset (TCO CT, OXXXH) does not affect the Page Address register.

Device Select Register (DS)

The Device Select register is used to select a specific (target) device using the TCO DS instruction by setting the 16-bit DS value equal to the target's PA value. In a daisy-chain, setting DS = FFFFH will select all devices. However, in this case, the ability to read information out of the device is restricted as shown in Tables 8a and 8b. A software Reset (using the Control register) does not affect the Device Select register.

Address Register (AR)

The Address register points to the CAM Memory location to be operated upon with a M@[AR] or M@aaaH instruction. It can be loaded directly by using a TCO AR instruction or indirectly by using an instruction requiring an absolute address, such as MOV aaaH,CR,V. After being loaded, the Address register value will then be used for the next memory access referencing the Address register. After this access, the Address register will automatically increment or decrement from that value according to the setting of CT3 and CT2 of the Control register. A Reset sets the Address register to zero.

Either the Foreground or Background Address register will be active, depending on which has been selected, and only the active Address register will be written to or read from.

Next Free Address Register (NF)

The Next Free Address in a system of MU9C3480A's can be read using a TCO NF instruction. Only the device with /FI LOW and /FF HIGH will respond with its contents of the Next Free Register, as shown in Table 7. The MU9C3480A automatically stores the address of the first empty memory location in the Next Free Address register, which is then used as a memory address pointer for M@NF operations. The Full Flag daisy chain causes only the device whose /FI input is LOW and /FF output HIGH to respond to an instruction using the Next Free address. After a Reset, the Next Free Address register is set to zero.

OPERATIONAL CHARACTERISTICS (CONT'D)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Page Address, PA5–0						**0**	**0**	Next Free Address, NF7–0							

Table 7: Next Free Address Register

Case	Internal /EC	Internal /MA(int)	External /MI	Device Select Reg.	Command Write*	Data Write*	Command Read*	Data Read*
1	1	X	X	DS = FFFFH	YES	YES	NO	NO
2	1	X	X	DS = PA	YES	YES	YES#	YES
3	1	X	X	DS ≠ FFFFH and DS ≠ PA	NO	NO	NO	NO
4	0	X	0	X	NO	NO	NO	NO
5	0	1	1	X	NO	NO	NO	NO
6	0	0	1	X	YES	YES	YES#	YES

*Note: Exceptions are 1) Write to Device Select register is always active in all devices, 2) Write to Page Address register is active in the device with /FI LOW and /FF HIGH; 3) the Set Full Flag (SFF) instruction is active in the device with /FI LOW and /FF HIGH; 4) a Command Read as the second cycle of a TCO NF instruction will always return the contents of the NFA register of the device with /FI LOW and /FF HIGH; and, 5) if /MF is disabled in the Control Register, /MA (Internal) is forced HIGH preventing a Case 6 response. # This is a NO for a TCO Read of the NFA if this device does not contain the first empty location in a daisy chain, or the daisy chain is FULL.

Table 8a: Device Select Response (1480 Mode)

Case	Internal /EC	Internal /MA(int)	External /MI	Device Select Reg.	Command Write*	Data Write*	Command Read*	Data Read*
1	1	X	X	DS = FFFFH	YES	YES	NO	NO
2	1	X	X	DS = PA	YES	YES	YES#	YES
3	1	X	X	DS ≠ FFFFH and DS ≠ PA	NO	NO	NO	NO
4	0	0	0	X	YES†	YES**	NO	NO
5	0	1	X	X	YES†	YES**	NO	NO
6	0	0	1	X	YES	YES	YES#	YES

*Note: Exceptions are 1) Write to Device Select register is always active in all devices, 2) Write to Page Address register is active in the device with /FI LOW and /FF HIGH; 3) the Set Full Flag (SFF) instruction is active in the device with /FI LOW and /FF HIGH; 4) a Command Read as the second cycle of a TCO NF instruction will always return the contents of the NFA register of the device with /FI LOW and /FF HIGH; and, 5) if /MF is disabled in the Control Register, /MA (Internal) is forced HIGH preventing a Case 6 response. † This is NO if it's a MOV or VBC instruction involving Memory at Highest Priority Match. ** This is NO if the Persistent Destination is Memory at Highest Priority Match. # This is a NO for a TCO Read of the NFA if this device does not contain the first empty location in a daisy chain, or the daisy chain is FULL.

Table 8b: Device Select Response (2480 Mode)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
/FL	/MM	Skip	Empty	**0**	Page Address Bits, PA15–PA5										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA4–PA0					**0**	**0**	Match Address, AM7–AM0								/MA

Note: The Status register is read by performing Command Read cycles. On the first cycle, bits 15–0 will be output, and if a second Command Read cycle is issued immediately after the first Command Read cycle, bits 31–16 will be output.

Table 9: Status Register Bit Assignments

OPERATIONAL CHARACTERISTICS (CONT'D)

Status Register

The 32-bit Status register, shown in Table 9, is the default source for Command Read cycles. Bit 31 is the internal Full flag, which will go LOW if the particular device has no empty memory locations. Bit 30 is the internal Multiple Match flag, which will go LOW if a Multiple match was detected. After a read or move from memory, bits 29-28 reflect the Skip and Empty validity bits of the last memory location read. In the MU9C5480, these bits always read back "00", but in the MU9C3480A, a "00" indicates the last Memory location read had its Validity bits set to "Valid". If no read or move from memory has occured, the Skip and Empty bits will read "11". Bits 26–11 give the Page Address of the device. Bits 8–1 give the match address of the Highest-priority match. After power-on or after a no-match condition, the match address will be all "1"s. Bit 0 is the internal Match flag, which will go LOW if a match was found in this particular device.

Comparand Register (CR)

The 64-bit Comparand register is the default destination for Data Writes and Reads, using the Segment Control register to select the segment of the Comparand register to be loaded or read out. The Persistent Source and Destination for Data Writes and Reads can be changed to the Mask registers or Memory by SPS and SPD instructions. During an automatic or forced compare, the Comparand register is compared against the CAM portion of all memory locations with the correct validity condition simultaneously. Automatic compares always compare against Valid Memory locations, while forced compares, using CMP instructions, can compare against Memory locations tagged with any specific validity condition.

The Comparand register may be shifted one bit at a time to the right or left by issuing a Shift Right or Shift Left instruction, with the right and left limits for the wrap-around determined by the CAM/RAM partitioning set in the Control register. During shift rights, bits shifted off the LSB of the CAM partition will reappear at the MSB of the CAM partition. Likewise, bits shifted off the MSB of the CAM partition will reappear at the LSB during shift lefts.

Mask Registers (MR1, MR2)

The Mask registers can be used in two different ways, either to mask compares or to mask data writes and moves. Either Mask register can be selected in the Control register to mask every compare, or selected by instructions to participate in data writes or moves to and from Memory. If a bit in a 64-bit Mask register is set to a "0", the corresponding bit in the Comparand register will enter into a masked compare operation. If a Mask bit is a "1", the corresponding bit in the Comparand register will not enter into a masked compare operation. Bits set to "0" in the Mask register cause corresponding bits in the destination register or memory location to be updated when masking data writes or moves, while a bit set to "1" will prevent that bit in the destination from being changed.

Either the Foreground or Background MR1 can be set active, but after a reset, the Foreground MR1 is active by default. MR2 incorporates a sliding mask, where the data can be replicated one bit at a time to the right or left with no wrap-around by issuing a Shift Right or Shift Left instruction. The right and left limits are determined by the CAM/RAM partitioning set in the Control register. For a Shift Right the upper limit bit is replicated to the next lower bit, while for a Shift Left the lower limit bit is replicated to the next higher bit.

THE MEMORY ARRAY

Memory Organization

The Memory array is organized as 256 64-bit locations, each having two Validity bits, the Skip bit and Empty bit. By default all locations are configured to be 64 CAM cells. However, the array can be reconfigured in the Control register to divide each location into a CAM field and a RAM field. The CAM/RAM partitioning is allowed on 16-bit boundaries, permitting selections of 64 CAM bits, 0 RAM bits; 48 CAM bits, 16 RAM bits; 32 CAM bits, 32 RAM bits; 16 CAM bits, 48 RAM bits;16 RAM bits, 48 CAM bits; 32 RAM bits/32 CAM bits; and, 48 RAM bits/16 CAM bits. Memory Array bits designated to be RAM bits can be used to store and retrieve Associated data (data associated with a CAM content).

Memory Access

There are two general ways to get data into and out of the memory array, directly or by moving the data via the Comparand or Mask registers.

The first way, through direct reads or writes, is set up by issuing a Set Persistent Destination (SPD) or Set Persistent Source (SPS) command. The addresses for the direct access can be directly supplied, supplied from the address register, supplied from the Next Free Address Register, or supplied as the Highest-priority Match address. Additionally, all the direct writes can be masked by either mask register.

The second way is to move data via the Comparand or Mask registers. This is accomplished by issuing Data Move commands (MOV). Moves using the Comparand register can also be masked by either of the Mask registers.

OPERATIONAL CHARACTERISTICS (CONT'D)

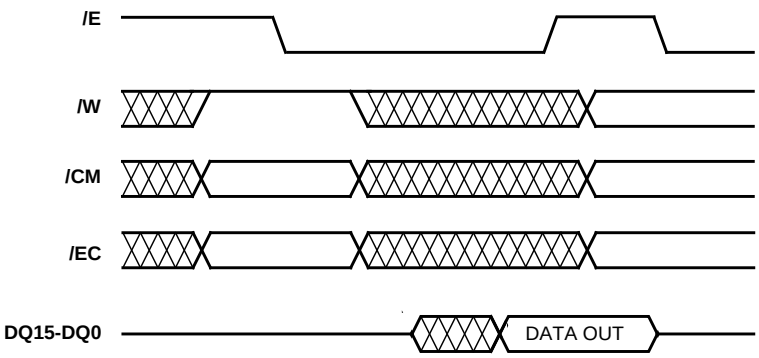


Figure 3: Read Cycle

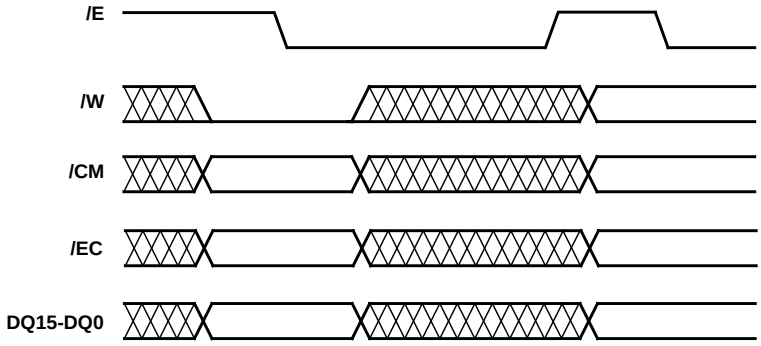
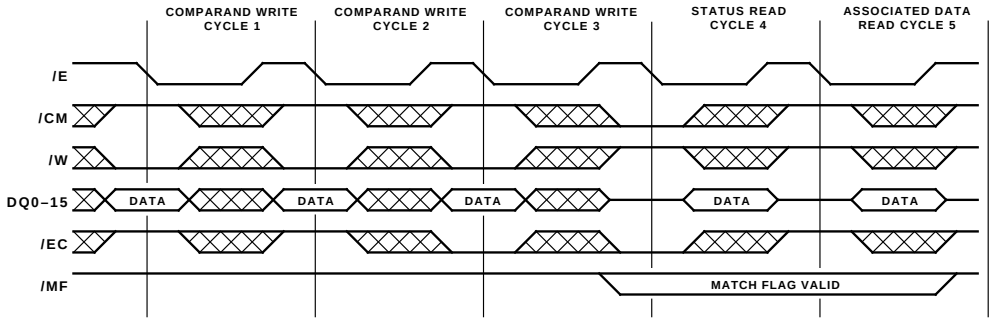


Figure 4: Write Cycle



Note: In this example, the Segment Control register is set such that the Destination Count runs from 01B to 11B. As such, an automatic compare cycle is generated by the third comparand write.

Figure 5: Example Cycle to Cycle Timing

OPERATIONAL CHARACTERISTICS (CONT'D)

I/O CYCLES

The MU9C3480A supports four basic I/O cycles: Data Read, Data Write, Command Read, and Command Write as shown in Table 2. The type of cycle is determined by the states of the /W and /CM control inputs. These signals are registered at the beginning of a cycle by the falling edge of /E.

During Read cycles, the DQ15-DQ0 outputs are enabled after /E goes LOW. During Write cycles, the data or command to be written is captured from DQ15-DQ0 at the beginning of the cycle by the falling edge of /E. Figures 3 and 4 show Read and Write cycles respectively. Figure 5 shows typical cycle-to-cycle timing with the Match flag valid at the end of the third comparand write cycle, assuming /EC is LOW at the start of this cycle. The Compare operation automatically occurs when the segment counter reaches the end count set in the Segment Control register (for Data writes to the Comparand or Mask registers). If there was a match, the next cycle reads status or associated data, depending on the state of /CM. For cascaded devices, /EC needs to be held LOW in the cycle prior to any cycle which requires a locked daisy-chain, such as a Status register or associated data read after a match. When set to 1480 mode, if there was not a match, the output buffers stay Hi-Z, and the daisy-chain must be unlocked by taking /EC HIGH during a NOP or other non-functioning cycle, as shown in Table 8a. Figure 6 shows how the internal /EC timing holds the daisy-chain locking effect over into the next cycle. In the 2480 mode, this NOP is not needed before data or command writes following a non-matching compare, as shown in Table 8b. A single-chip system does not require daisy-chained match flag operation, hence /EC could be tied high and the /MA pin or flag in the Status register used instead of /MF, allowing access to the device regardless of the match condition.

The minimum timings for the /E control signal are given in the Electrical Characteristics section. Note that at minimum timings the /E signal is non-symmetrical, and that different cycle types have different timing requirements as given in Table 11.

COMPARE OPERATIONS

All compare operations available in the LANCAM are similar in that the data in the Comparand register is compared to all locations in the Memory array simultaneously, including the Validity bits. There are two ways compares are initiated: Automatic and Forced compares. The mask register to be used for compares is selected in the Control register.

Automatic compares perform a compare of the contents of the Comparand register against Memory locations that are tagged as "Valid", and occur whenever the following happens:

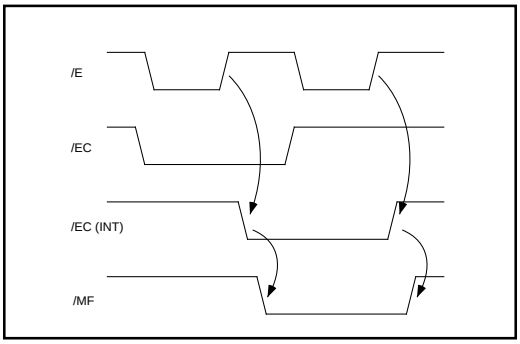


Figure 6: /EC(Int) Timing Diagram

1. The Destination Segment counter in the Segment Control register reaches its end limit during writes to the Comparand or Mask registers.

2. After the Control register is loaded with a new value, an automatic compare occurs using the new Control register settings.

Forced compares are initiated by CMP instructions using one of the four validity conditions. The forced compare against "Empty" locations automatically masks all 64 bits of data to find all locations with the validity bits set to "Empty", while the other forced compares are only masked as selected in the Control register.

VERTICAL CASCADING

The MU9C3480A can be vertically cascaded to increase system depth. Through the use of flag daisy-chaining, multiple LANCAMs will respond as an integrated system. The daisy-chain of flags allows all commands to operate globally. For example, operations at the Next Free address or at the Highest-priority Match address will only operate in the device in a string that actually has the first empty location or the first matching location, respectively. When connected in a daisy-chain, the last device's Full flag and Match flag accurately report the condition for the whole string. By setting the Page Address and Device Select registers to the same value, individual devices in a daisy-chain can be addressed. The ripple delay of the flags when connected in a daisy-chain requires the extension of the /E HIGH time until the logic in all devices has settled out. In a string of "n" devices, the /E HIGH time should be greater than t_{EHMFV} + (n-1) • t_{MIVMFV}. A system in which MU9C3480As are vertically cascaded using daisy-chaining of the flags is shown in Figure 2a.

OPERATIONAL CHARACTERISTICS (CONT'D)

LOCKED DAISY-CHAIN

In a locked daisy chain, the highest priority device is the one with /MI HIGH and /MF LOW. In the 1480 mode, only this device will respond to command and data reads and writes, until the daisy chain has been unlocked by taking /EC HIGH. This allows reading only from the associated data field of the Highest-priority Match location anywhere in a string of devices, or the Match address from the Status register of the device with the match. It also permits updating the entry stored at the Highest-priority Match location. In the 2480 mode, devices are enabled to respond to command and data writes, with some exceptions, but not command and data reads.

Table 8a (1480 mode) and Table 8b (2480 mode) shows when a device will respond to reads or writes and when it won't based on the state of /EC(int), the internal match condition, and other control inputs. /EC is latched by the falling edge of /E. /EC(int) is registered from the latched /EC signal off the rising edge of /E, so it controls what happens in the next cycle, as shown in Figure 6. When /EC is first taken LOW in a string of LANCAM devices (and assuming the Device Select registers are set to FFFFH), all devices will respond to that command write or data write.

In the 1480 mode, from then on, the daisy-chain will remain locked in each subsequent cycle as long as /EC is held LOW on the falling edge of /E in the current cycle. When the daisy-chain is locked, only the Highest-priority Match device will respond (See Case 6 of Table 8a). If, for example, all of the CAM memory locations were empty, there would be no match, and /MF would stay HIGH. Since none of the devices could then be the Highest-priority Match device, none will respond to reads or writes until the daisy chain is unlocked by taking /EC HIGH and asserting /E for a cycle.

If there is a match between the data in the Comparand register and a location or locations in memory, then only the Highest-priority Match device will respond to any cycle, such as an associated data or Status register read. If there isn't a match, then a NOP with /EC HIGH needs to be inserted before issuing any new instructions, such as Write to Next Free Address instruction to learn the data. Since Next Free operations are controlled by the /FI-/FF daisy-chain, only the device with the first empty location will respond. If an instruction is used to unlock the daisy-chain it will work only on the Highest-priority Match device, if one exists. If none exists, the instruction will have no effect except to unlock the daisy-chain. To read the Status registers of specific devices when there is no match requires the use of the TCO DS command to set DS=PA of each device. Single chip systems can tie /EC HIGH and just use the status register to monitor match conditions, as the daisy chain lock-out feature is not needed in this configuration. This will alleviate the need for inserting an additional NOP in the case of a no-match condition.

When the Control register is set to the 2480 mode, you can continue to write data to the Comparand register or issue a Move to Next Free Address instruction without first having to issue a NOP with /EC HIGH to unlock the daisy-chain after a Compare cycle with no match, as shown in Cases 4 and 5 of Table 8b. In the 2480 mode, data write cycles as well as command write cycles are enabled even when /EC is LOW, except in the cases of Moves to HM or VBC at HM instructions. The 2480 mode speeds up system performance by eliminating the need to unlock the daisy-chain.

Full Flag Cascading

The Full Flag daisy-chain cascading is used for three purposes: First, to allow instructions that address Next Free locations to operate globally, second, to provide a system wide Full flag, and third, to allow the loading of the Page Address registers during initialization using the SFF instruction. The full flag logic causes only the device containing the first empty location to respond to Next Free instructions such as "MOV NF,CR,V", which will move the contents of the Comparand register to the first empty location in a string of devices and set that location Valid, so it will be available for the next automatic compare. With devices connected as in Figure 2a, the /FF output of the last device in a string provides a full indication for the entire string.

Match Flag Cascading

The Match Flag daisy-chain cascading is used for three purposes: First, to allow operations on Highest Priority Match addresses to operate globally over the whole string, second, to provide a system wide match flag, and third, to lock out all devices except the one with the Highest-priority match for instructions such as Status reads after a match. The Match flag logic causes only the highest priority device to operate on its Highest-priority Match location and lower priority devices to ignore operations on Highest-priority Match locations. With devices connected as in Figure 2a, the /MF output of the last device provides a system match indication for the entire string. The lock-out feature is enabled by the match flag cascading and the use of the /EC control signal as shown in Tables 8a and 8b.

Global vs. Local Access for Cascaded Systems

The Device Select register controls access to devices in the daisy-chain once the Page Address registers have been initialized. Local access into a daisy-chained system works by sending a Device Select value to all Device Select registers which equals the Page Address

OPERATIONAL CHARACTERISTICS (CONT'D)

Cycle Type	Opcode or Data on DQ Bus	Control Bus /E	/CM	/W	/EC	Comments	Notes
Command Write	0000H	L	L	L	H	Accounts for Power-up anomalies	
Command Write	TCO DS	L	L	L	H	Target Device Select register to disable local device selection	
Command Write	FFFFH	L	L	L	H	Disables Device Select feature	
Command Write	TCO CT	L	L	L	H	Target Control register for reset	1
Command Write	0000H	L	L	L	H	Causes reset	1
Command Write	TCO PA	L	L	L	H	Target Page Address register to set page for cascaded operation	2
Command Write	nnnnH	L	L	L	H	Page Address value	2
Command Write	SFF •	L	L	L	H	Set Full flag; allows access to next device (repeat previous 2 cycles plus this one for each device in chain)	2, 3
Command Write	TCO CT	L	L	L	H	Target Control register for reset of Full flags, but not Page Address.	1
Command Write	0000H	L	L	L	H	Causes Reset	1
Command Write	TCO CT	L	L	L	H	Target Control register for initial values	4
Command Write	8040H	L	L	L	H	Control register value	4
Command Write	TCO SC	L	L	L	H	Target Segment Counter Control register	
Command Write	3808H	L	L	L	H	Set both Segment Counters to write to Segment 1, 2 and 3, and read from Segment 0.	4
Command Write	SPS M@HM	L	L	L	H	Sets Data Reads from Segment 0	

Notes

1. A software Reset using a TCO CT followed by 0000H puts the device in a known state shown in Table 5. Good programming practice dictates a software reset for initialization to account for all possible conditions.
2. This instruction may be omitted for a single LANCAM application.
3. The last SFF will cause the /MF pin in the last chip in a daisy chain to go LOW. In a daisy chain, DS needs to be set equal to PA to read out of a particular chip prior to a match condition.
4. A typical LANCAM control environment: Enable match flag; Enable full flag; 48 CAM bits, 16 RAM bits; Disable comparison masking; Enable address increment. See Table 4 for Control register bit assignments.

Table 10: Example Initialization Routine

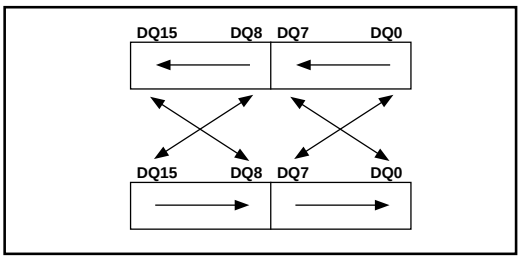


Figure 7: IEEE 802.3/802.5 Format Mapping

of the target device, using the TCO DS instruction. Once this is done, only the device which has a match between its Page Address register and its Device Select register will respond to Read or Write cycles.

Loading the value “FFFFH” into the Device Select registers of a string will restore global access as shown in Tables 8a and 8b, with Read cycles being restricted to devices with the Highest-priority Match to eliminate bus contention.

IEEE 802.3/802.5 Format Mapping

To support the symmetrical mapping between the address formats of IEEE 802.3 and IEEE 802.5, the MU9C3480A provides a bit translation facility. Formally expressed, the nth input bit, D(n), maps to the xth output bit, Q(x), through the following expressions:

$$D(n) = Q(7-n) \text{ for } 0 \le n \le 7,$$
$$D(n) = Q(23-n) \text{ for } 8 \le n \le 15$$

Setting Control register bits 10 and 9 selects whether to persistently translate, or persistently not to translate, the data written onto the 64-bit internal bus. The default condition after a Reset command is not to translate the incoming data. Figure 7 shows the bit mapping between the two formats.

INITIALIZING THE MU9C3480A LANCAM

Initialization of the MU9C3480A is required to configure the various registers on the device. Since a Control register reset establishes the operating conditions shown in Table 5, restoration of normal operating conditions better suited for the application is usually required after a Reset.

Setting Page Address Register Values

In a vertically cascaded system, the user must set the individual Page Address registers to unique values by using the Page Address initialization mechanism. Each Page Address register must contain a unique value to prevent bus contention. This process allows individual device selection. The Page Address register initialization works as follows: Writes to Page Address registers are only active for devices with /FI LOW and /FF HIGH. At initialization, all devices are empty, thus the top device in the string will respond to a TCO PA instruction, and load its PA register. To advance to the next device in the string, a Set Full Flag (SFF) instruction is used, which is also only active for the device with /FI LOW and /FF HIGH. The SFF instruction changes the first device’s /FF to LOW, although the device really is empty, which allows the next device in the string to respond to the TCO PA instruction and load its PA register. The initialization proceeds through the chain in a similar manner filling all the PA registers in turn. Each device must have a unique Page Address value stored in its PA register, or contention will result. After all the PA registers are filled, the entire string is reset through the Control register, which does not change the values stored in the individual PA registers. After the reset, the Device Select registers are usually set to FFFFH to enable operation as shown in Case 1 of Tables 8a and 8b. The Control registers and the Segment Control registers are now also set to their normal operating values for the application.

Vertically Cascaded System Initialization

Table 10 shows an example of code that initializes a daisy-chained string of LANCAM devices. The Initialization example shows how to set the Page Address registers of each of the devices in the chain through the use of the Set Full Flag instruction, and how the Control registers and Segment counters of all the LANCAM devices are set for a typical application. Each Page Address register must contain a unique value (not FFFFH) to prevent bus contention. The first Command Write of all zeroes is provided to take care of the situation of an anomalous power-up state caused by a too slow rise of the voltage on /E relative to VCC. For typical daisy-chain operation, data is loaded into the Comparand registers of all the devices in a string simultaneously by setting DS=FFFFH. Since reading is prohibited when DS=FFFFH except for the device with a match, for a diagnostic operation you need to select a specific device by setting DS=PA for the desired device to be able to read from it. Tables 8a and 8b show the pre-conditions for reading and writing.

Initialization for a single LANCAM is simpler. The Device Select register in this case is usually set to equal the Page Address register for normal operations. If the hardware match flag, /MF, is not needed by this single device application, the compare results can be read out of the Status register or from the /MA pin. Because /MF isn’t monitored, the /EC signal is also not needed and can be kept HIGH, which will eliminate the need to insert a NOP after a no-match, often speeding up the application.

INSTRUCTION SET DESCRIPTION*

Instruction: Select Persistent Source (SPS)

Binary Op-Code:	**0000 f000 0000 0sss**
f	**Address Field Flag†**
sss	**Selected Source**

This instruction selects a persistent source for Data Reads, until another SPS instruction changes it or a Reset occurs. The default source for Data Read cycles is the Comparand register after power-up or Reset. Setting the persistent source to M@aaaH loads the Address register with 'aaaH', and the first access to that persistent source will be at aaaH, after which the AR value increments or decrements as set in the Control register. The SPS M@[AR] instruction does the same except the current Address register value is used.

Instruction: Select Persistent Destination (SPD)

Binary Op-Code:	**0000 f001 mmdd dvvv**
f	**Address Field Flag†**
mm	**Mask Register Select**
ddd	**Selected Destination**
vvv	**Validity Setting for memory location destinations**

This instruction selects a persistent destination for Data Writes, which remains until another SPD instruction changes it or a Reset occurs. The default destination for Data Write cycles is the Comparand register after power-up or Reset. When the destination is the Comparand register or the Memory array, the data written may be masked by either Mask Register 1 or 2, so that only destination bits corresponding to bits in the Mask register set to "0" will be modified. An automatic compare will occur after writing the last segment of the Comparand or Mask registers, but not after writing to Memory. Setting the persistent destination to M@aaaH loads the Address register with 'aaaH', and the first access to that persistent destination will be at aaaH, after which the AR value increments or decrements as set in the Control register. The SPD M@[AR] instruction does the same except the current Address register value is used.

Instruction: Temporary Command Override (TCO)

Binary Op-Code:	**0000 0010 00dd d000**
ddd	**Register selected as source or destination for only the next Command Read or Write cycle.**

The TCO instruction selects a register as the source or destination for only the next Command Read or Write cycle, so a value can be loaded or read out of the register. Subsequent Command Read or Write cycles revert to reading the Status register and writing to the Instruction decoder. All registers but the NF, PS and PD can be written to, and all can be read from. The Status register is only available via non-TCO Command Read cycles. Reading the PS register also outputs the Device ID of 341H in bits 15–4.

Instruction: Data Move (MOV)

Binary Op-Code:	**0000 f011 mmdd dsss or 0000 f011 mmdd dvss**
f	**Address Field Flag†**
mm	**Mask Register select**
ddd	**Destination of Data**
sss	**Source of Data**
v	**Validity setting if destination is a memory location**

The MOV instruction performs a 64-bit move of the data in the selected source to the selected destination. If the source or destination is M@aaaH, the Address register is set to 'aaaH', and will increment or decrement as set in the Control register from that value after the move completes, as it will after a MOV with respect to [AR]. Data transfers between the Memory array and the Comparand register may be masked by either Mask Register 1 or Mask Register 2, in which case, only those bits in the destination which correspond to bits in the selected Mask register set to "0" will be changed. A Memory location used as a destination for a MOV instruction may be set to Valid or left unchanged. If the source and destination are the same register, no net change occurs (a NOP).

Instruction: Validity Bit Control (VBC)

Binary Op-Code:	**0000 f100 00dd dvvv**
f	**Address Field Flag†**
ddd	**Destination of data**
vvv	**Validity setting for Memory location**

The VBC instruction sets the Validity bits at the selected memory locations to the selected state. This feature can be used in finding all valid entries, by using a repetitive sequence of CMP V through a Mask of all "1s", followed by a VBC HM, S. If the VBC target is M@aaaH, the Address register is set to 'aaaH', and will increment or decrement as set in the Control register from that value after the operation completes, as it will after a VBC [AR] instruction.

Instruction: Compare (CMP)

Binary Op-Code:	**0000 0101 0000 0vvv**
vvv	**Validity condition**

A CMP V, S, or R instruction forces a Comparison of Valid, Skipped, or Random entries against the Comparand register through a Mask register, if one is selected. During a CMP E instruction, the compare is only done on the Validity bits, and all data bits are automatically masked.

Instruction: Special Instructions

Binary Op-Code:	**0000 0110 00dd drrr**
ddd	**Target Resource**
rrr	**Operation**

These instructions are a special set for the MU9C3480A to accommodate the added features over the MU9C5480. Two alternate sets of configuration registers can be

selected by using the Set Foreground and Set Background Register Set instructions. These registers are the Control, Segment Control, Address, Mask Register 1, and the PS and PD registers. An RSC instruction will reset the Segment Control register count values for both Destination and Source to the original Start Limits. The Shift instructions will shift the designated register one bit right or left. The right and left limits for shifting are determined by the CAM/RAM partitioning set in the Control register. The Comparand register is a barrel-shifter, and for the example of a device set to 64 bits of CAM, bit 0 is moved to bit 63, bit 1 is moved to bit 0, and bit 63 is moved to bit 62 for a Shift Comparand Right instruction. For a Shift Comparand Left instruction, bit 63 is moved to bit 0, bit 0 is moved to bit 1 and bit 62 is moved to bit 63. MR2 acts as a sliding mask, where for a Shift Right instruction bit 1 is replicated to bit 0, while bit 0 "falls off the end", and bit 63 is replicated to bit 62. For a Shift Mask Left instruction, bit 0 is replicated to bit 1, bit 62 is replicated to bit 63, and bit 63 "falls off the end". With shorter width CAM fields, the bit limits on the right or left move to match the width of CAM field.

Instruction: Set Full Flag (SFF)
Binary Op-Code: 0000 0111 0000 0000

The SFF instruction is a special instruction used to force the Full flag LOW to permit setting the Page Address register in vertically cascaded systems.

Instruction: No Operation (NOP)
Binary Op-Code: 0000 0011 0000 0000

The NOP(No-Op) belongs to the MOV instructions, where a register is moved to itself. No change occurs within the device. This instruction is useful in unlocking the daisy chain in 1480 mode.

Notes:
** Instruction cycle lengths given in Table 11.*
† If f=1, the instruction requires an absolute address to be supplied, which updates the Address register to the "aaaH" value supplied in the second cycle of the instruction. After instructions involving M@[AR] or M@aaaH, the Address register will be incremented or decremented depending on the setting in the Control register.

INSTRUCTION SET SUMMARY

MNEMONIC FORMAT

INS dst,src[msk],val

INS: Instruction mnemonic.
dst: Destination of the data.
src: Source of the data.
msk: Mask register used.
val: Validity condition set at the location written.

Instruction: Select Persistent Source

Operation	Mnemonic	Op-Code
Comparand Register	SPS CR	0000H
Mask Register 1	SPS MR1	0001H
Mask Register 2	SPS MR2	0002H
Memory Array at Address Reg	SPS M@[AR]	0004H
Memory Array at Address	SPS M@aaaH	0804H
Memory at Highest-priority Match	SPS M@HM	0005H

Instruction: Select Persistent Destination

Operation	Mnemonic	Op-Code
Comparand Register	SPD CR	0100H
Masked by MR1	SPD CR[MR1]	0140H
Masked by MR2	SPD CR[MR2]	0180H
Mask Register 1	SPD MR1	0108H
MaskRegister 2	SPD MR2	0110H
Memory at Address Reg set Valid	SPD M@[AR],V	0124H
Masked by MR1	SPD M@[AR][MR1],V	0164H
Masked by MR2	SPD M@[AR][MR2],V	01A4H
Memory at Address Reg set Empty	SPD M@[AR],E	0125H
Masked by MR1	SPD M@[AR][MR1],E	0165H
Masked by MR2	SPD M@[AR][MR2],E	01A5H
Memory at Address Reg set Skip	SPD M@[AR],S	0126H
Masked by MR1	SPD M@[AR][MR1],S	0166H
Masked by MR2	SPD M@[AR][MR2],S	01A6H
Memory at Address Reg set Random	SPD M@[AR],R	0127H
Masked by MR1	SPD M@[AR][MR1],R	0167H
Masked by MR2	SPD M@[AR][MR2],R	01A7H
Memory at Address set Valid	SPD M@aaaH,V	0924H
Masked by MR1	SPD M@aaaH[MR1],V	0964H
Masked by MR2	SPD M@aaaH[MR2],V	09A4H
Memory at Address set Empty	SPD M@aaaH,E	0925H
Masked by MR1	SPD M@aaaH[MR1],E	0965H
Masked by MR2	SPD M@aaaH[MR2],E	09A5H
Memory at Address set Skip	SPD M@aaaH,S	0926H
Masked by MR1	SPD M@aaaH[MR1],S	0966H
Masked by MR2	SPD M@aaaH[MR2],S	09A6H
Memory at Address set Random	SPD M@aaaH,R	0927H
Masked by MR1	SPD M@aaaH[MR1],R	0967H
Masked by MR2	SPD M@aaaH[MR2],R	09A7H
Memory at Highest-prio. Match,Valid	SPD M@HM,V	012CH
Masked by MR1	SPD M@HM[MR1],V	016CH
Masked by MR2	SPD M@HM[MR2],V	01ACH
Memory at Highest-prio. Match,Emp.	SPD M@HM,E	012DH
Masked by MR1	SPD M@HM[MR1],E	016DH
Masked by MR2	SPD M@HM[MR2],E	01ADH
Memory at Highest-prio. Match, Skip	SPD M@HM,S	012EH
Masked by MR1	SPD M@HM[MR1],S	016EH
Masked by MR2	SPD M@HM[MR2],S	01AEH
Memory at High-prio. Match, Random	SPD M@HM,R	012FH
Masked by MR1	SPD M@HM[MR1],R	016FH
Masked by MR2	SPD M@HM[MR2],R	01AFH
Memory at Next Free Addr., Valid	SPD M@NF,V	0134H
Masked by MR1	SPD M@NF[MR1],V	0174H
Masked by MR2	SPD M@NF[MR2],V	01B4H
Memory at Next Free Addr.,Empty	SPD M@NF,E	0135H
Masked by MR1	SPD M@NF[MR1],E	0175H
Masked by MR2	SPD M@NF[MR2],E	01B5H
Memory at Next Free Addr., Skip	SPD M@NF,S	0136H
Masked by MR1	SPD M@NF[MR1],S	0176H
Masked by MR2	SPD M@NF[MR2],S	01B6H
Memory at Next Free Addr., Random	SPD M@NF,R	0137H
Masked by MR1	SPD M@NF[MR1],R	0177H
Masked by MR2	SPD M@NF[MR2],R	01B7H

INSTRUCTION SET SUMMARY (CONT'D)

Instruction: Temporary Command Override

Operation	Mnemonic	Op-Code
Control Register	TCO CT	0200H
Page Address Register	TCO PA	0208H
Segment Control Register	TCO SC	0210H
Read Next Free Address	TCO NF	0218H
Address Register	TCO AR	0220H
Device Select Register	TCO DS	0228H
Read Persistent Source	TCO PS	0230H
Read Persistent Destination	TCO PD	0238H

Instruction: Data Move

Operation	Mnemonic	Op-Code
Comparand Register from:		
No Operation	NOP	0300H
Mask Register 1	MOV CR,MR1	0301H
Mask Register 2	MOV CR,MR2	0302H
Memory at Address Reg	MOV CR,[AR]	0304H
Masked by MR1	MOV CR,[AR][MR1]	0344H
Masked by MR2	MOV CR,[AR][MR2]	0384H
Memory at Address	MOV CR,aaaH	0B04H
Masked by MR1	MOV CR,aaaH[MR1]	0B44H
Masked by MR2	MOV CR,aaaH[MR2]	0B84H
Memory at Highest-prio Match	MOV CR,HM	0305H
Masked by MR1	MOV CR,HM[MR1]	0345H
Masked by MR2	MOV CR,HM[MR2]	0385H
Mask Register 1 from:		
Comparand Register	MOV MR1,CR	0308H
No Operation	NOP	0309H
Mask Register 2	MOV MR1,MR2	030AH
Memory at Address Reg	MOV MR1,[AR]	030CH
Memory at Address	MOV MR1,aaaH	0B0CH
Memory at Highest-prio Match	MOV MR1,HM	030DH
Mask Register 2 from:		
Comparand Register	MOV MR2,CR	0310H
Mask Register 1	MOV MR2,MR1	0311H
No Operation	NOP	0312H
Memory at Address Reg	MOV MR2,[AR]	0314H
Memory at Address	MOV MR2,aaaH	0B14H
Memory at Highest-prio Match	MOV MR2,HM	0315H
Memory at Address Register, No Change to Validity bits, from:		
Comparand Register	MOV [AR],CR	0320H
Masked by MR1	MOV [AR],CR[MR1]	0360H
Masked by MR2	MOV [AR],CR[MR2]	03A0H
Mask Register 1	MOV [AR],MR1	0321H
Mask Register 2	MOV [AR],MR2	0322H
Memory at Address Register, Location set Valid, from:		
Comparand Register	MOV [AR],CR,V	0324H
Masked by MR1	MOV [AR],CR[MR1],V	0364H
Masked by MR2	MOV [AR],CR[MR2],V	03A4H
Mask Register 1	MOV [AR],MR1,V	0325H
Mask Register 2	MOV [AR],MR2,V	0326H
Memory at Address, No Change to Validity bits, from:		
Comparand Register	MOV aaaH,CR	0B20H
Masked by MR1	MOV aaaH,CR[MR1]	0B60H
Masked by MR2	MOV aaaH,CR[MR2]	0BA0H
Mask Register 1	MOV aaaH,MR1	0B21H
Mask Register 2	MOV aaaH,MR2	0B22H
Memory at Address, Location set Valid, from:		
Comparand Register	MOV aaaH,CR,V	0B24H
Masked by MR1	MOV aaaH,CR[MR1],V	0B64H
Masked by MR2	MOV aaaH,CR[MR2],V	0BA4H
Mask Register 1	MOV aaaH,MR1,V	0B25H
Mask Register 2	MOV aaaH,MR2,V	0B26H
Memory at Highest-priority Match, No Change to Validity bits, from:		
Comparand Register	MOV HM,CR	0328H
Masked by MR1	MOV HM,CR[MR1]	0368H
Masked by MR2	MOV HM,CR[MR2]	03A8H
Mask Register 1	MOV HM,MR1	0329H
Mask Register 2	MOV HM,MR2	032AH
Memory at Highest-priority Match, Location set Valid, from:		
Comparand Register	MOV HM,CR,V	032CH
Masked by MR1	MOV HM,CR[MR1],V	036CH
Masked by MR2	MOV HM,CR[MR2],V	03ACH
Mask Register 1	MOV HM,MR1,V	032DH
Mask Register 2	MOV HM,MR2,V	032EH
Memory at Next Free Address, No Change to Validity bits, from:		
Comparand Register	MOV NF,CR	0330H
Masked by MR1	MOV NF,CR[MR1]	0370H
Masked by MR2	MOV NF,CR[MR2]	03B0H
Mask Register 1	MOV NF,MR1	0331H
Mask Register 2	MOV NF,MR2	0332H
Memory at Next Free Address, Location set Valid, from:		
Comparand Register	MOV NF,CR,V	0334H
Masked by MR1	MOV NF,CR[MR1],V	0374H
Masked by MR2	MOV NF,CR[MR2],V	03B4H
Mask Register 1	MOV NF,MR1,V	0335H
Mask Register 2	MOV NF,MR2,V	0336H

Instruction: Validity Bit Control

Operation	Mnemonic	Op-Code
Set Validity bits at Address Register		
Set Valid	VBC [AR],V	0424H
Set Empty	VBC [AR],E	0425H
Set Skip	VBC [AR],S	0426H
Set Random Access	VBC [AR],R	0427H
Set Validity bits at Address		
Set Valid	VBC aaaH,V	0C24H
Set Empty	VBC aaaH,E	0C25H
Set Skip	VBC aaaH,S	0C26H
Set Random Access	VBC aaaH,R	0C27H
Set Validity bits at Highest-priority Match		
Set Valid	VBC HM,V	042CH
Set Empty	VBC HM,E	042DH
Set Skip	VBC HM,S	042EH
Set Random Access	VBC HM,R	042FH
Set Validity bits at All Matching Locations		
Set Valid	VBC ALM,V	043CH
Set Empty	VBC ALM,E	043DH
Set Skip	VBC ALM,S	043EH
Set Random Access	VBC ALM,R	043FH

Instruction: Compare

Operation	Mnemonic	Op-Code
Compare Valid Locations	CMP V	0504H
Compare Empty Locations	CMP E	0505H
Compare Skipped Locations	CMP S	0506H
Compare Random Access Locations	CMP R	0507H

Instruction: Special Instructions

Operation	Mnemonic	Op-Code
Shift Comparand Right	SFT CR, R	0600H
Shift Comparand Left	SFT CR, L	0601H
Shift Mask Register 2 Right	SFT MR2, R	0610H
Shift Mask Register 2 Left	SFT MR2, L	0611H
Select Foreground Register Set	SFR	0618H
Select Background Register Set	SBR	0619H
Reset Seg. Cont. Reg. to Initial Values	RSC	061AH

Instruction: Miscellaneous Instructions

Operation	Mnemonic	Op-Code
No-operation	NOP	0300H
Set Full Flag	SFF	0700H

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 Volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature Under Bias	-40°C to +85°C
Storage Temperature	-55°C to +125°C
DC Output Current	20 mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to GND.

OPERATING CONDITIONS (voltages referenced to GND at the device pin)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage	4.75	5.0	5.25	Volts	
V_{IH}	Input Voltage Logic "1"	2.2		V_{CC}+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	1, 2
T_A	Ambient Operating Temperature	0		70	°C	Still Air

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typical	Max	Units	Notes
I_{CC}	Average Power Supply Current		35	55	mA	tELEL=tELEL(min.), 9
$I_{CC(SB)}$	Stand-by Power Supply Current			7	mA	/E = HIGH
V_{OH}	Output Voltage Logic "1"	2.4			Volts	I_{OH} = -2.0 mA
V_{OL}	Output Voltage Logic "0"			0.4	Volts	I_{OL} = 4.0 mA
I_{IZ}	Input Leakage Current	-2		2	µA	$V_{SS} \le V_{IN} \le V_{CC}$, 10
I_{OZ}	Output Leakage Current	-10		10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$; DQ_n = High Impedance

CAPACITANCE

Symbol	Parameter	Max	Units	Notes
C_{IN}	Input Capacitance	6	pF	f=1MHz, V_{IN}=0 V.
C_{OUT}	Output Capacitance	7	pF	f=1MHz, V_{OUT}=0 V.

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 volts
Output Timing Reference Level	1.5 volts

SWITCHING TEST FIGURES

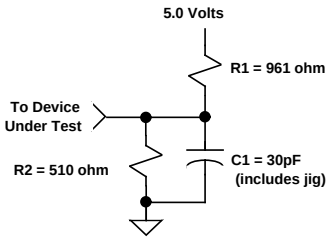


Figure 8: AC Test Load A

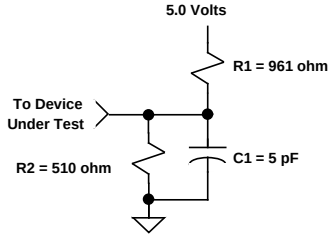


Figure 9: AC Test Load B

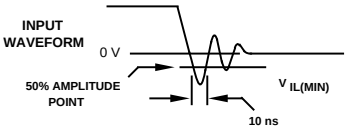


Figure 10: Input Signal Waveform

SWITCHING CHARACTERISTICS (see Note 3)

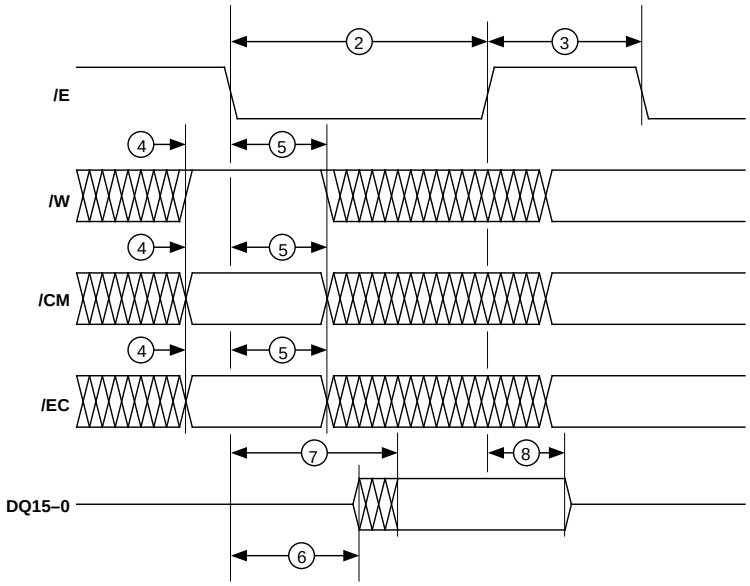
No	Symbol	Parameter (all times in nanoseconds)	-70		-90		-12		Notes
			Min	Max	Min	Max	Min	Max	
1	t_{ELEL}	Chip Enable Compare Cycle Time	70		90		120		
2	t_{ELEH}	Chip Enable LOW Pulse Width — Short Cycle:	15		25		35		4
		Medium Cycle:	35		50		75		4
		Long Cycle:	55		75		100		4
3	t_{EHEL}	Chip Enable HIGH Pulse Width	15		15		20		
4	t_{CVEL}	Control Input to Chip Enable LOW Set-up Time	0		0		0		5
5	t_{ELCX}	Control Input from Chip Enable LOW Hold Time	10		10		15		5
6	t_{ELQX}	Chip Enable LOW to Outputs Active	3		3		3		6
7	t_{ELQV}	Chip Enable LOW to Outputs Valid		30		50		70	4,6
				52		75		85	4,6
8	t_{EHQZ}	Chip Enable HIGH to Outputs High-Z	3	10	3	15	3	20	7
9	t_{DVEL}	Data to Chip Enable LOW Set-up Time	0		0		0		
10	t_{ELDX}	Data from Chip Enable LOW Hold Time	10		10		15		
11	t_{FIVEL}	Full In Valid to Chip Enable LOW Set-up Time	0		0		0		
12	t_{FIVFFV}	Full In Valid to Full Flag Valid		5		7		8	
13	t_{ELFFV}	Chip Enable LOW to Full Flag Valid		50		75		90	
14	t_{MIVEL}	Match In Valid to Chip Enable LOW Set-up Time	0		0		0		
15	t_{EHMFX}	Chip Enable HIGH to /MF, /MA, /MM Invalid	0		0		0		
16	t_{MIVMFV}	Match In Valid to /MF Valid, /MA, /MM		5		7		8	
17	t_{EHMFV}	Chip Enable HIGH to /MF Valid		16		25		30	
18	tEHMXV	Chip Enable HIGH to /MA and /MM Valid		18		25		30	
19	tRLRH	Reset LOW Pulse Width	100		100		100		8

NOTES

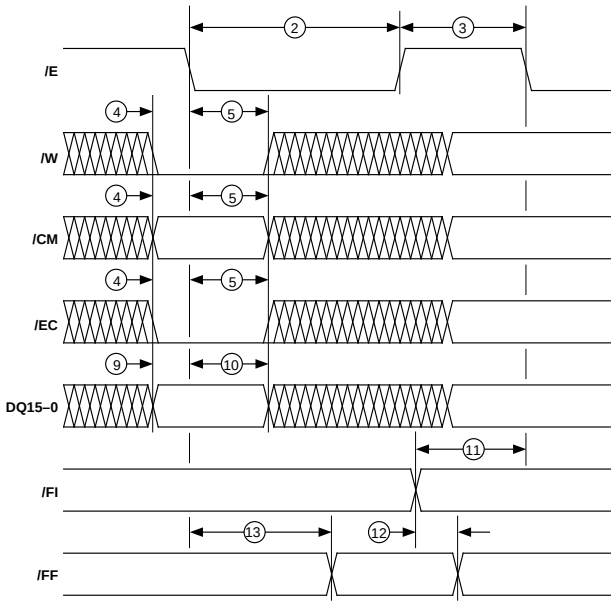
1. -1.0V for a duration of 10 ns measured at the 50% amplitude points for Input-only lines (Figure 10).
2. Common I/O lines are clamped, so that signal transients cannot fall below -0.5V.
3. At 0-70°C and 5.0V ± 0.25V.
4. See Table 11.
5. Control signals are /W, /CM and /EC.
6. With load specified in Figure 8.
7. With load specified in Figure 9.
8. /E must be HIGH during this period to ensure accurate default values in the configuration registers.
9. With output and I/O pins unloaded.
10. The /Reset pin has an internal pull-up registor of 6-12 Kohms.

TIMING DIAGRAMS

READ CYCLE

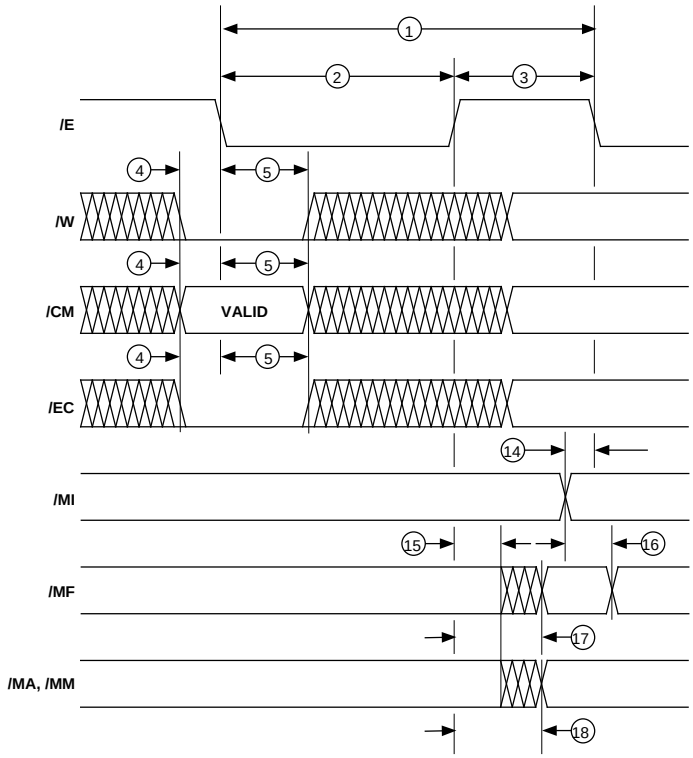


WRITE CYCLE



TIMING DIAGRAMS (CONT'D)

COMPARE CYCLE



CYCLE LENGTH	CYCLE TYPE			
	Command Write	**Command Read**	**Data Write**	**Data Read**
Short	MOV reg, reg TCO reg (except CT) SPS, SPD, SFT, SFR, SBR, RSC, NOP		Comparand register (not last segment) Mask register (not last segment)	
Medium	MOV reg, mem TCO CT (reset) VBC (NF Address invalid)	Status register or 16-bit register	Memory array (NF Address invalid)	Comparand register Mask register
Long	MOV mem, reg TCO CT (non-reset) CMP SFF VBC (NF Address valid)		Memory array (NF Address valid) Comparand register (last segment) Mask register (last segment)	Memory array

Note: The specific timing requirements for Short, Medium and Long cycles are given in the Switching Characteristics Section under the tELEH parameter. For two cycle Command Writes (TCO reg or any instruction requiring an immediate address) the first cycle is a short, and the second cycle will be the length given.

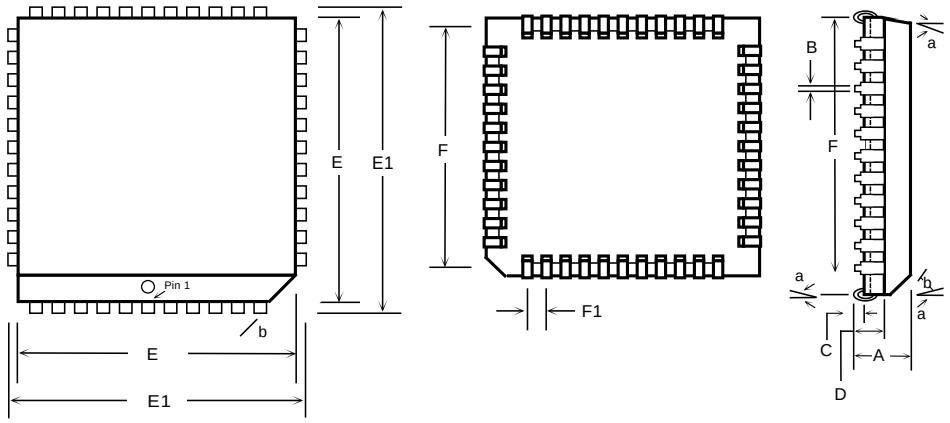
Table 11: Instruction Cycle Lengths

MU9C3480A
LANCAM®

ORDERING INFORMATION

PART NUMBER	CYCLE TIME	PACKAGE	TEMPERATURE	VOLTAGE
MU9C3480A-70DC	70ns	44-PIN PLCC	0-70°C	5.0 ± 0.25
MU9C3480A-90DC	90ns	44-PIN PLCC	0-70°C	5.0 ± 0.25
MU9C3480A-12DC	120ns	44-PIN PLCC	0-70°C	5.0 ± 0.25

PACKAGE OUTLINE



Dimensions are in inches.

44-pin PLCC	Dim. A	Dim. B	Dim. C	Dim. D	Dim. E	Dim. E1	Dim. F	Dim. F1	Dim. a	Dim. b	
(in.)	.170 .180	.017 TYP	.018 .032	.100 TYP	.650 .656	.685 .695	.590 .630	.050 TYP	3° 6°	.045±.002 x 45°±2°	

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