Preliminary Data Sheet

MU9C8328A Ethernet Interface

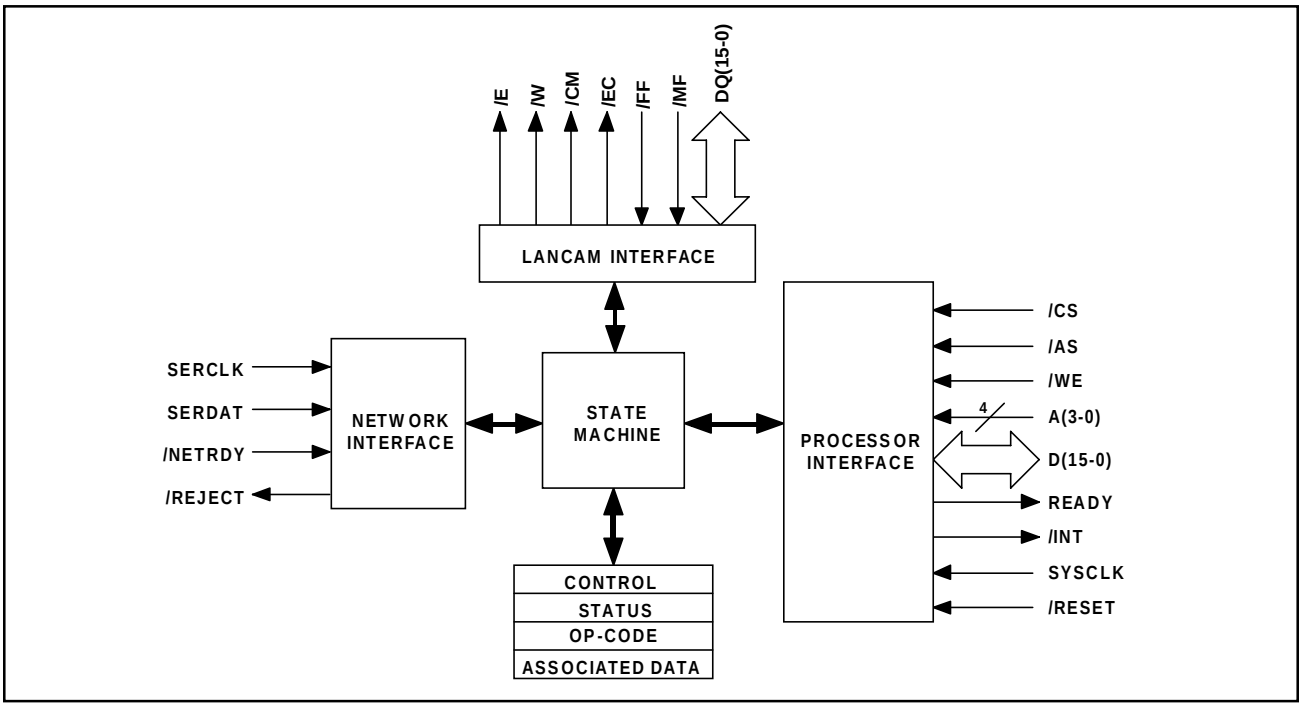
APPLICATION BENEFITS

- **Single port 10 MHz Ethernet address parsing, filtering, and learning at wire speed**
- **Glue-free interface between the MUSIC LANCAM® Family and AMD, National, Motorola, or similar Ethernet Controllers having an NRZ serial data port**
- **Selectable filtering and learning decisions on DA and SA compares**
- **Supports aging with built-in LRU purge routine**
- **Supports cascaded MUSIC LANCAM series for long station lists**
- **Host processor port for LANCAM initialization and housekeeping activities**
- **Supports system clock rates from 20 MHz to 33 MHz**
- **Compatible with MU9C8328**
- **100-pin PQFP package**
- **5 Volt operation**

GENERAL DESCRIPTION

The MU9C8328A speeds up bridging operations using Ethernet controller chips with serial NRZ data outputs, such as AMD's MACE™, National's SONIC™, and Motorola's QUICC™ controllers, by parsing the Ethernet frame independently of the Ethernet controller device, and notifying it whether to accept or reject the incoming frame. The MU9C8328A supports both positive and negative filtering on the Destination address and learning of new Source addresses, by efficiently controlling the compare activities of the MUSIC LANCAM Family. Filtering and learning routines are user configurable. These routines are automatically invoked by the internal state machine based on the contents of the incoming frame and the configuration settings. For aging and other housekeeping routines, the MU9C8328A provides the proper sequencing and timing of LANCAM accesses for an external processor.

The MU9C8328A receives serial NRZ data from the Ethernet controller chip, finds the Start delimiter, and loads the DA and SA into registers. The DA is sent to the LANCAM for filtering and, depending on the filter action



Block Diagram

24 June 1999 Rev. 0.8 Draft

Note: This document version has not completed MUSIC's internal approval process, therefore it should be rechecked with a released version or with factory personnel.

GENERAL DESCRIPTION *Continued*

selected, notifies the controller whether to copy or purge the frame. The SA is then sent to the LANCAM for comparison, and if no match is found, can be learned to the Next Free address in the LANCAM. Scheduling is done within the MU9C8328A so that each filtering action completes in the time of a minimum length frame. The filtering and learning routines are preprogrammed in the MU9C8328A, with decision options set in the Control register. A Status register is provided so the host processor can determine the results of activities. The specific Op-Code for the LANCAM learning instruction is by default a MOV NF, CR, V, but it can be overridden by writing a value to the Op-Code register. Aging and purging activity is directly controlled by the host processor. The READY signal notifies the host processor that processor operations are complete. The /INT signal notifies the processor that a network frame has been processed and the result stored in the Status register. The processor can turn off the network filtering activity to have total control of the LANCAM; during this time the controller can be notified to accept or reject all frames.

PIN DESCRIPTIONS

All signals are implemented in CMOS technology with TTL levels. Signal names that start with a slash ("/") are active LOW. Inputs should never be left floating. Refer to the Electrical Characteristics section for more information.

NETWORK INTERFACE

SERCLK (Serial Clock, Input, TTL)

SERCLK is the nominally 10 MHz clock from the Ethernet controller chip to the MU9C8328A. Frame parsing begins only after the internal clock detector determines that SERCLK is valid. Internally pulled down with nominal 50K resistor.

SERDAT (Serial Data, Input, TTL)

SERDAT is the NRZ data from the 10 MHz Ethernet controller chip. The MU9C8328A uses SERCLK to strobe SERDAT looking for a Start Frame delimiter (SFD), at which point it begins filtering and learning activity on the Destination Address (DA) and Source Address (SA).

/REJECT (Reject, Output, TTL)

The MU9C8328A takes /REJECT LOW to notify the Ethernet controller chip to reject a frame under conditions set in the Filter Control register.

/NETRDY (Network Ready, Input, TTL)

If /NETRDY is LOW, the MU9C8328A begins parsing frame data received on the SERDAT input if SERCLK is valid. The Ethernet controller chip, or the user, takes /NETRDY HIGH to indicate that SERCLK or SERDAT is invalid or is transmitting. The MU9C8328A frame parser and internal state machines are returned to an idle state after safely completing any LANCAM activity, while ignoring any compare results. Internally pulled down with nominal 50K resistor.

PROCESSOR INTERFACE

SYSCLK (System Clock, Input, TTL)

SYSCLK is a 20 MHz to 33 MHz continuous clock provided by the host system and is the master clock within the MU9C8328A. It is used to determine the presence of a valid clock on the SERCLK input, operate the three internal state machines, and provide the proper timing of the signals on the LANCAM port. If SYSCLK is below 30 MHz, a LANCAM speed grade of 120 ns is acceptable. Above 30 MHz, a LANCAM speed grade of 90 ns or better is required.

/CS (Chip Select, Input, TTL)

/CS is taken LOW by the host processor to gain access to the registers of the MU9C8328A or to directly access the LANCAM through the MU9C8328A internal LANCAM registers. The state of /CS becomes effective on the rising edge of SYSCLK. When /CS goes HIGH, the MU9C8328A continues filtering and learning based on conditions set in the Filter Control register and the frame activity on the network interface.

/AS (Address Strobe, Input, TTL)

The falling edge of /AS latches the A(2–0) bus, and when both /AS and /CS are LOW, the processor state machine is enabled by first rising edge of the SYSCLK to begin writes into or reads out of the MU9C8328A.

PIN DESCRIPTIONS *Continued*

/WE (Write Enable, Input, TTL)

/WE determines the direction of data flow into or out of the MU9C8328As processor interface. It also determines the state of /W to the LANCAM when the processor is accessing the MU9C8328As internal LANCAM registers. If /WE is LOW, the data is written into the register selected by the A(3–0) bus. If /WE is HIGH, then data is read out of the register selected by the A(3–0) bus.

A(3–0) (Address Bus, Input, TTL)

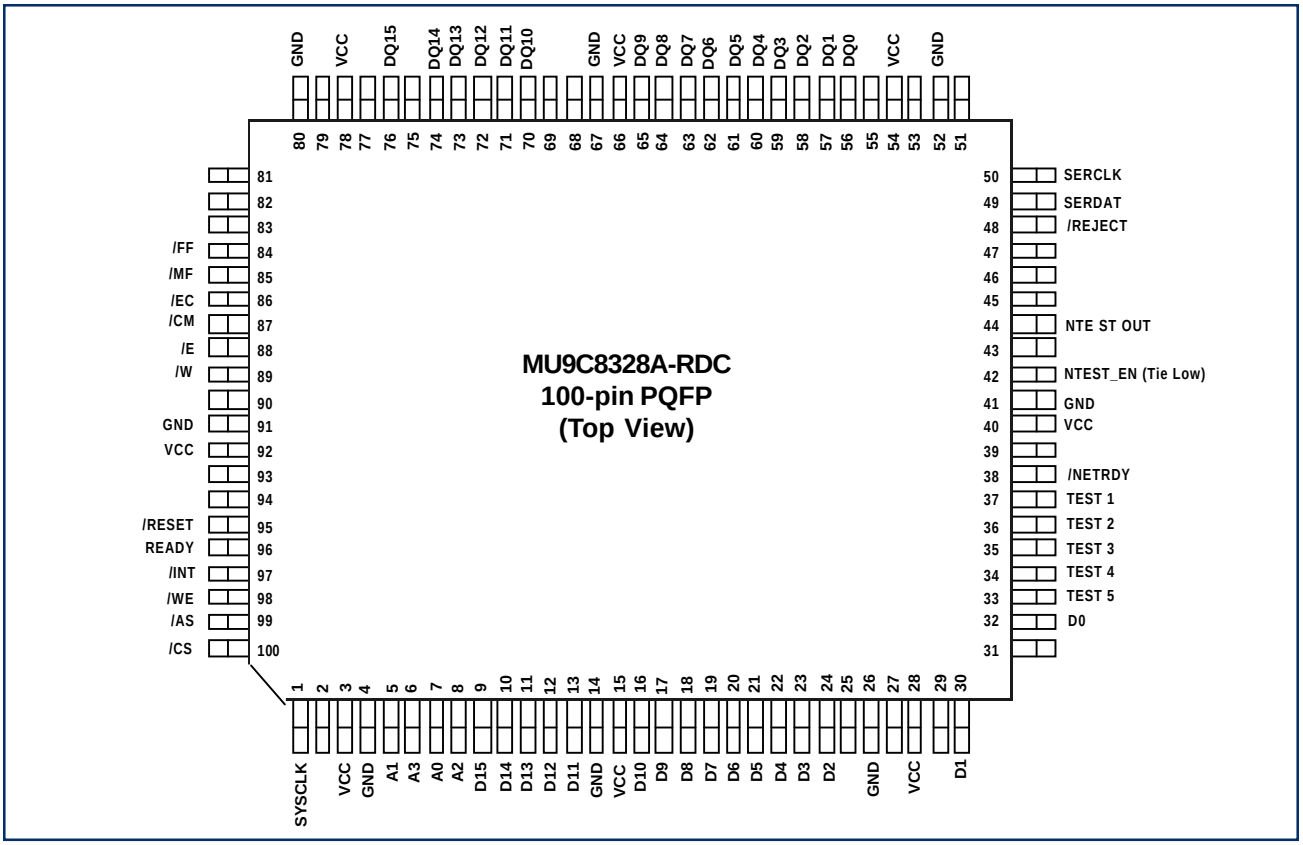
A(3–0) select the internal register in the MU9C8328A accessed by the host processor as shown in Table 1. A(3–0) are latched by the falling edge of /AS. A(3) is internally pulled down with a nominal 50K resistor to maintain compatibility with the MU9C8328.

D(15–0) (Data Bus, I/O, Three-state TTL)

D(15–0) is the processor data bus into and out of the MU9C8328A, and is demuxed to the internal registers as selected by the A(2–0) bus. If the register selected is the Control, Status or Op-Code register, when /WE is LOW, D(15–0) is loaded on the second rising edge of SYSCLK after both /AS and /CS are LOW. When /WE is HIGH, data from the selected register is output to the D(15–0) bus on the second rising edge of SYSLCK after both /AS and /CS are LOW. For CAM access, the write or read operation is completed when READY returns HIGH. If /CS is HIGH, or if data is not being read out of the MU9C8328A, the output buffers go to HIGH-Z. Internally pulled down with nominal 50K resistor.

READY (Ready, Output, Three-state, TTL)

When writing to the Control, Status, or Op-Code register, READY goes LOW on the first rising edge of SYSCLK after both /AS and /CS are LOW and returns HIGH on the next rising edge of SYSCLK. For a read cycle from those registers, READY may only show a negative-going spike at the first rising edge of SYSCLK after both /AS and /CS are LOW. The data will be valid before the next rising edge of SYSCLK. When writing to the CAM registers, READY will go LOW on the first rising edge of SYSCLK after both /CS and /AS are LOW. READY returns HIGH three SYSCLK cycles after. When reading from the CAM registers, READY will return HIGH five SYSCLK cycles later.



Pinout Diagram

PIN DESCRIPTIONS *Continued*

/INT (Interrupt, Output, Three-state TTL)
/INT goes LOW to signal the processor that a frame has been processed, and the results loaded into the Status register. /INT returns HIGH when the Status register is read.

/RESET (Reset, Input, TTL)
When /RESET is taken LOW, all the internal state machines are reset to their initial state. Any data stored in the input address parser is cleared, and the Control, Status, and Learn Op-Code registers are reset to their default values. /RESET is synchronous and should be held LOW for a minimum of two SYSCLK cycles. The user must set the LANCAM Segment Control register after asserting /RESET.

LANCAM INTERFACE

DQ(15–0) (CAM Data Bus, I/O, Three-state TTL)
The DQ(15–0) bus communicates 16-bit data or instructions between the MU9C8328A and the LANCAM. When no data is being transmitted by either, the bus goes HIGH-Z. Internally pulled down with nominal 50K resistor.

/E (Chip Enable, Output, TTL)
The MU9C8328A takes /E LOW to initiate LANCAM activity by registering the /W, /CM, /EC, and DQ(15–0) signals into the LANCAM. /E is taken HIGH to register returning data into the MU9C8328A.

/W (Write Gate, Output, TTL)
The MU9C8328A outputs /W to control the direction of data flow between the MU9C8328A and the LANCAM. If /W is LOW at the falling edge of /E, the MU9C8328A is outputting data to the DQ(15–0) bus for the LANCAM to input. When /W is HIGH at the falling edge of /E, the LANCAM outputs data to the DQ(15–0) bus for input to the MU9C8328A.

/CM (Data/Command Select, Output, TTL)
The MU9C8328A outputs /CM to control whether the LANCAM interprets the DQ(15–0) bus as containing command information or data. If both /CM and /W are LOW at the falling edge of /E, the MU9C8328A is outputting an instruction for the LANCAM to execute, or a value for one of the LANCAM configuration registers. If /CM is LOW while /W is HIGH, then the LANCAM will be outputting data from one of its configuration registers to the MU9C8328A. If /CM is HIGH while /W is LOW, the MU9C8328A is outputting data for the LANCAM to place in its data registers or memory. If /CM is HIGH while /W is HIGH, the LANCAM is outputting data from one of its data registers or memory to the MU9C8328A.

/EC (Enable Daisy Chain, Output, TTL)
The MU9C8328A takes /EC LOW to control a daisy chain of LANCAMs by generating the /MF output from the LANCAM in the case of a match between the contents of its Comparand register and its memory. When /EC is LOW, only the LANCAM containing the match will respond to write cycles, or output read data. When /EC is HIGH, all LANCAMs will respond to write cycles.

/MF (Match Flag, Input, TTL)
The LANCAM takes /MF LOW to indicate to the MU9C8328A that a match was found in its memory with the contents of its Comparand register. /MF returns HIGH after the MU9C8328A takes /EC HIGH, or the match condition is no longer valid. In a daisy chain of LANCAMs, the /MF signal comes from the /MF output of the last LANCAM in the string. Internally pulled down with nominal 50K resistor.

/FF (Full Flag, Input, TTL)
The LANCAM takes /FF LOW to indicate to the MU9C8328A that the LANCAM has no empty locations remaining. /FF is taken HIGH when the LANCAM has one or more locations still empty. In a daisy chain of LANCAMs, the /FF signal comes from the /FF output pin of the last LANCAM in the string. Internally pulled down with nominal 50K resistor.

TEST

NTEST_EN
Reserved–Tie low.

NTTESTOUT
Reserved–Do not connect.

TEST (5–0)
Reserved for manufacturing tests–Do not connect.

POWER AND GROUND

VCC, GND (Positive Power Supply, Ground)
The VCC pins must be connected externally to a power source regulated to 5.0 ± 0.5 Volts, and should be adequately bypassed to the Ground pins through both high and low frequency capacitors. The Ground pins should all be connected to a common ground plane.

FUNCTIONAL DESCRIPTION

The MU9C8328A works with the MUSIC LANCAMs to provide a complementary and versatile 10 MHz Ethernet filtering solution for bridges, routers, and switches. Using the serial NRZ data stream and clock available from many Ethernet controller chips, the MU9C8328A parses the incoming frame, finds the Start Delimiter, and forms the Destination and Source addresses into 16-bit words for relay to the LANCAM. After all three 16-bit DA segments have been loaded into the LANCAM, an automatic compare occurs between the incoming DA and the 48-bit MAC addresses stored in the LANCAM. If a match is found, the MU9C8328A is notified, and if Control register bit 5 is set for negative filtering, the /REJECT line will be asserted if Control register bit 3 is set. An interrupt can also be generated over the /INT pin if Control register bit 8 is set. Also, if Control register bit 0 is set, the Associated data in segment 0 of the matching entry in the LANCAM will be retrieved and stored in the Associated Data register for reading by the host processor. If a match is not found on the DA, and Control register bit 5 was set for positive filtering, the /REJECT line will be asserted. An interrupt can also be enabled for a no-match on a DA using Control register bit 10.

After the DA filtering, the Source Address is loaded into the LANCAM in three segments. Upon the last SA load, an automatic compare again takes place. If there is a match between the SA and an entry in the CAM, and Control register bit 7 was set, an interrupt is asserted. Positive and negative filtering on the SA is also possible, set by Control register bit 4, and the /INT pin may be asserted as well. In the case of a no-match on an SA, the SA can be automatically "learned" (that is, moved to the first empty location in the LANCAM) if Control register bit 1 is set.

If a Loss of Carrier is detected by SERCLK staying LOW for more than 16 SYSCLK cycles, an interrupt is triggered if Control register bit 12 is set. This interrupt also activates if a collision is detected.

The host processor can access the MU9C8328A internal registers, shown in Table 1, at any time, even when a frame is being processed. Access to the LANCAM through the LANCAM access registers (04H to 07H) is arbitrated, however, with the network having precedence. The host processor can have control of the LANCAM by setting the Network Enable bit in the Control register (bit 13) to a 0, which will disable network filtering until it is returned to a 1. While disabled, bit 14 in the Control register sets the MU9C8328A to accept all frames by keeping /REJECT HIGH, or to reject all frames by keeping /REJECT LOW.

Registers 04H through 07H give the host processor access to the LANCAM for Command and Data Write and Read cycles, with /EC HIGH or LOW. This is often needed for housekeeping activities, such as preventing the LANCAM from becoming full by aging out old entries based on time stamps stored in the Associated data (Segment 0) of the LANCAM memory.

Registers 08H holds the update Op-Code. This is 0300H after reset to maintain compatibility with the MU9C8328. To update a SA entry time stamp, the device must be initialized to auto-learn in the Control register and 0328H (MOV HM, CR) must be written to the update Op-Code register. When filtering the SA, if it does not exist in the CAM, the SA gets put into the next free address. If it already has been entered in the CAM, just the time stamp bits are updated with the value in the time stamp register.

Register 08H holds the update Op-Code, 09H is the Purge Routine Op-Code register and 0AH is the Time Stamp register. Writing a value to the TimeStamp register initiates a Purge routine. The lower 8 bits written to the Time Stamp register is the time stamp that will be purged. The upper 8 bits written to the register will be the new time stamp for data.

The /INT pin will go LOW at the end of the SA field to indicate an interrupt for any of the reasons set in the Control register. Reading the Status register to discover the nature of the interrupt will take the /INT pin HIGH again. The READY signal goes LOW after a host processor write to a register or the LANCAM to indicate that the Write cycle has begun and return HIGH after a fixed number of SYSCLK cycles. It will also go LOW during a read from the LANCAM and return HIGH when the data from the LANCAM is valid. Since a network compare activity has precedence over a host process access to the LANCAM, READY will stay LOW until the network activity is complete and the host-induced LANCAM read has completed.

Figure 1 shows a typical network filtering sequence, where the MU9C8328A's Control register was set to 2109H. This setting enables network filtering, enables an interrupt for a match found on the DA, enables negative filtering on the DA (reject if a DA match is found), enables asserting the /REJECT pin for compares on the DA, and enables retrieving the Associated Data field from the matching location in the LANCAM.

FUNCTIONAL DESCRIPTION *Continued*

A(3–0)	/WE	Resource Selected	Action
0H	L	Control register	Write
0H	H	Control register	Read
1H	L	Reserved	
1H	H	Status Register	Read
2H	L	Learn Op-Code Register	Write
2H	H	Learn Op-Code Register	Read
3H	L	Reserved	
3H	H	Associated Data Register	Read
4H	L	LANCAM Command Cycle with /EC LOW	Write
4H	H	LANCAM Command Cycle with /EC LOW	Read
5H	L	LANCAM Command Cycle with /EC HIGH	Write
5H	H	LANCAM Command Cycle with /EC HIGH	Read
6H	L	LANCAM Data Cycle with /EC LOW	Write
6H	H	LANCAM Data Cycle with /EC LOW	Read
7H	L	LANCAM Data Cycle with /EC HIGH	Write
7H	H	LANCAM Data Cycle with /EC HIGH	Read
8H	L	Update Op-Code Register	Write
8H	H	Update Op-Code Register	Read
9H	L	Purge Op-Code Register	Write
9H	H	Purge Op-Code Register	Read
AH	L	Time stamp Register	Write
AH	H	Time stamp Register	Read

Table 1: Address Decode

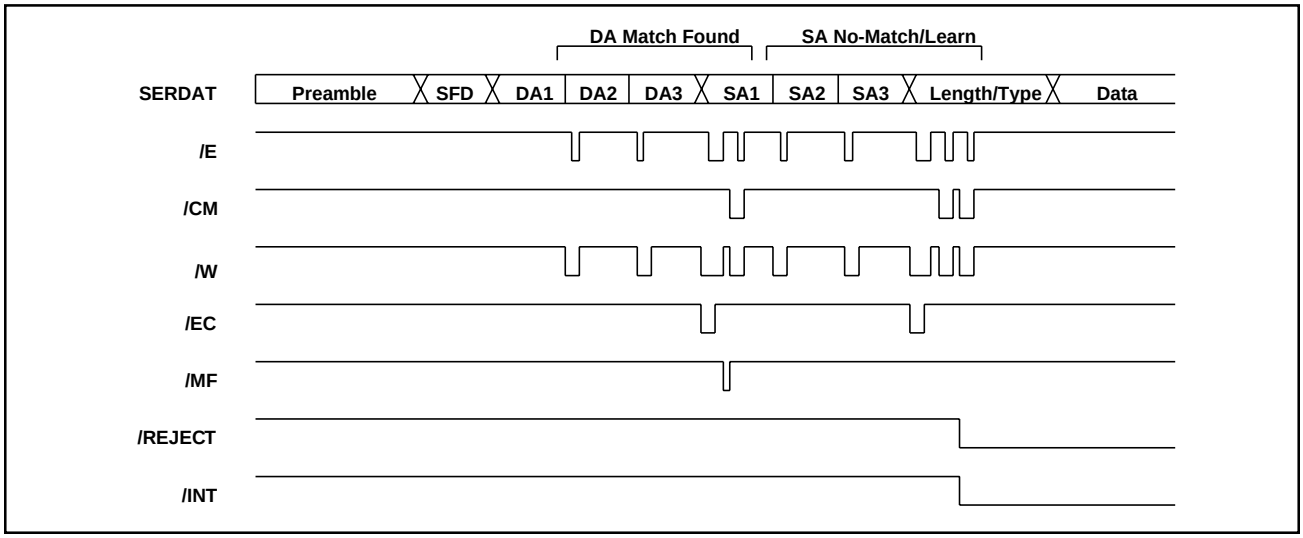


Figure 1: Typical Network Filtering

FUNCTIONAL DESCRIPTION *Continued*

CONTROL REGISTER (0000)		
Bit	**Mnemonic**	**Description**
15	DONE	1: Enables an interrupt when both the DA and SA CAM lookups are complete.
14	P/R	1: Passes all frames, 0: Rejects all frames. NETEN must be set to 0 for this option.
13	NETEN	1: Enables network filtering, 0: Disables network filtering.
12	ERR	1: Enables an interrupt for a frame error caused by loss of carrier or collision.
11	FULL	1: Enables an interrupt if the LANCAM is full.
10	NODA	1: Enables an interrupt for a no-match on DA.
9	NOSA	1: Enables an interrupt for a no-match on SA.
8	DA	1: Enables an interrupt for a DA match.
7	SA	1: Enables an interrupt for an SA match.
6	REJECT	1: Enables an interrupt for a reject.
5	DAPON	1: Rejects frame if there is no DA match (positive filtering). 0: Rejects frame if there is a DA match (negative filtering). This bit is a “Don’t Care” if DAEN is 0.
4	SAPON	1: Rejects frame if there is no SA match (positive filtering). 0: Rejects frame if there is an SA match (negative filtering). This bit is a “Don’t Care” if SAEN is 0.
3	DAEN	1: Enables asserting the /REJECT pin after a DA compares, based on bit 5.
2	SAEN	1: Enables asserting the /REJECT pin after an SA compares, based on bit 4.
1	LEARN	1: Enables auto-learning on no-match of SA.
0	ASSOC	1: Enables a read of Associated data after a DA match.

Table 2: Register Descriptions

FUNCTIONAL DESCRIPTION *Continued*

STATUS REGISTER (0001)		
Bit	**Mnemonic**	**Description**
15–8		Reserved.
7	COL	1 = Collision detected.
6	LOC	1 = Loss of carrier detected.
5	BUSY	1 = Network port is busy using the LANCAM.
4	MATCH	1 = A match was found.
3	FULL	1 = The LANCAM is full.
2	DAM	1 = A Destination Address match was found.
1	SAM	1 = A Source Address match was found.
0	REJECT	1 = The frame was rejected.
LEARN OP-CODE REGISTER (0010)		
Bit	**Mnemonic**	**Description**
15–0	ALOC	Contains the Op-Code to be used for an auto-learn, if enabled. Default is 0334H (MOV NF, CR, V), but can be overwritten.
UPDATE OP-CODE REGISTER (1000)		
Bit	**Mnemonic**	**Description**
15-0	UOC	Contains the Op-Code to be used for updating the time stamp on a SA match Default is 0300H (NOP). To update time stamp write 0328H (MOV HM, CR) to this register.
PURGE OP-CODE REGISTER (1001)		
Bit	**Mnemonic**	**Description**
15-0	POC	Contains the Op-Code to be used for the purge routine. Default is 043DH (VBC ALM,E).
TIME STAMP REGISTER (1010)		
Bit	**Mnemonic**	**Description**
15-8	NEW_TS	The value used for time stamp updates.
7-0	OLD_TS	The value used to purge old entries.

Table 2: Register Descriptions *Continued*

APPLICATIONS

Connections

Connection diagrams are shown in Figures 2, 3, and 4 for National's SONIC, AMD's MACE, and Motorola's QUICC Ethernet controller chips. Other controller chips that provide a serial NRZ received data port and clock can also be used in similar fashions. The /NETRDY line is provided for controller chips that output data on the received data line while transmitting. If /NETRDY is deasserted, the internal network state machine will safely complete any current activity and then wait until /NETRDY is asserted again before parsing another frame. If the controller chip does not output data on the received data line while transmitting, /NETRDY may be tied to ground, and the MU9C8328As valid clock detector will determine when it is time to start parsing a frame.

Initialization of the LANCAM

Before using, the MUSIC LANCAMs need to be configured for the number of LANCAMs in a daisy chain and for the filtering conditions in the Control and Segment Control registers. Before configuring the LANCAMs, bit 13 in the MU9C8328A Control register needs to be set to 0, to turn off network filtering. Table 3 shows the steps for configuring two LANCAMs in a daisy chain. The routine selects register 05H in the MU9C8328A, which sends Command Write cycles to the LANCAM. The sequence shown resets the LANCAMs, sets the Page address for both LANCAMs in the daisy chain, then sets the Control and Segment Control registers. If a Mask register were needed, then the sequence would be modified to set the Persistent destination to MR1 or MR2, use MU9C8328A register 07H to write data into the Mask register, change the final Control register value to 8051H or 8061H instead of 8041H to invoke MR1 or MR2 during compares, and then resetting

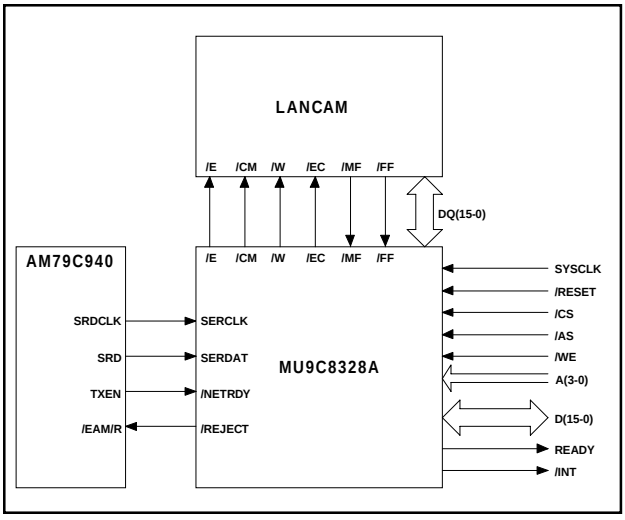


Figure 2: AMD's MACE™ Connection Diagram

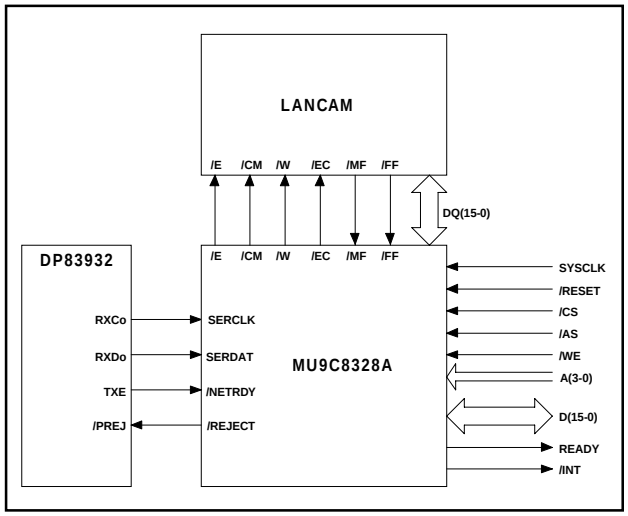


Figure 3: National's SONIC™ Connection Diagram

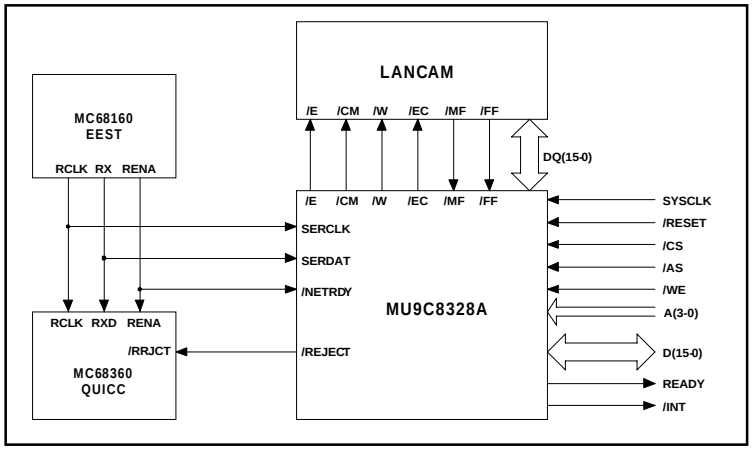


Figure 4: Motorola's QUICC™ Connection Diagram

APPLICATIONS *Continued*

the Persistent destination to the Comparand register as shown in Table 3. If only one LANCAM is used, Table 3 would be modified to replace steps 9 through 14 with a TCO DS (0228H) followed by a 0000H.

Enabling Network Activity

After the LANCAMs have been initialized, the MU9C8328A is enabled to begin processing network traffic by setting bit 13 (NETEN) in its Control register to a 1 along with the desired filtering actions and interrupt enables.

Responding to Interrupts

Depending on the filtering or error interrupt conditions set in the MU9C8328A Control register, the /INT line will assert at the end of the frame SA field. The host can then read the MU9C8328A Status register to determine the cause of the interrupt, whereupon the Status register is reset. If there was a DA match interrupt and read associated data was set, then the associated data segment stored in the LANCAM at the same location that matched the frame's DA can be read out of the Associated Data register (03H).

Step	A(2–0)	/WE	Mnemonic	D(15–0)	Comments
1	0H	L		C000H	Pass all frames during initialization
2	5H	H		0000H	Command Read to reset LANCAM state machines
3	5H	L	TCO_DS	0228H	Selects all Device Select registers
4	5H	L		FFFFH	Selects all LANCAMs
5	5H	L	TCO_CT	0200H	Selects all Control registers
6	5H	L		0000H	Resets all memory locations
7	5H	L	TCO_PA	0208H	Selects first Page Address register
8	5H	L		0000H	Writes first Page Address value
9	5H	L	SFF	0700H	Sets Full flag on first LANCAM
10	5H	L	TCO_PA	0208H	Selects second Page Address register
11	5H	L		0001H	Writes second Page Address value
12	5H	L	SFF	0700H	Sets Full flag on second LANCAM
13	5H	L	TCO_CT	0200H	Selects all Control registers
14	5H	L		0000H	Resets all Full flags
15	5H	L	SBR	0619H	Select Background Register set
16	5H	L	TCO_CT	0200H	TCO CT
17	5H	L		8111H	48RAM, 16CAM, MR1, Enhanced mode
18	5H	L	TCO_SC	0210H	Select Segment Control register
19	5H	L		0000H	Set Read and Write to segment 0
20	5H	L	SPD_MR1	0108H	Set Persistent Destination to Mask Register 1
21	7H	L		FFF0H	Setup Time Stamp in lowest 8 bits of segment 0
22	5H	L	SPD_CR	0100H	Set Persistent Destination to Comparand register
23	5H	L	SFR	0618H	Select Foreground Register set
24	5H	L	TCO_CT	0200H	Select Command register
25	5H	L		8041H	48CAM, 16RAM, No Mask, Enhanced mode
26	5H	L	SPD_MR1	0108H	Set Persistent Destination to Mask Register 1
27	5H	L	TCO_SC	0210H	Select Segment Control register
28	5H	L		1C04H	Set to write Segments 0, 1, 2, and 3
29	7H	L		FFF0H	Write to Segment 0 of MR1
30	7H	L		FFFFH	Write to Segment 1 of MR1
31	7H	L		FFFFH	Write to Segment 2 of MR1
32	7H	L		FFFFH	Write to Segment 3 of MR1
33	5H	L	SPD_CR	0100H	Set Persistent Destination to Comparand register
34	5H	L	TCO_SC	0210H	Select Segment Control register
35	5H	L		3808H	Write Segments 1–3, Read Segment 0
36	5H	L	SPS_HM	0005H	Set Persistent source to Highest match
37	0H	L		290BH	Enable filter, Negative filter on DA, enable learn

Table 3: LANCAM Initialization Code

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 Volts to 7.0 Volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-55°C to +125°C
DC Output Current	20 mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to GND.

OPERATING CONDITIONS (voltages referenced to GND at the device pin)

Symbol	Parameter		Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage		4.5	5.0	5.5	Volts	
V_{IH}	Input Voltage Logic 1		2.0		V_{CC} + 0.5	Volts	
			0.7 V_{CC}		V_{CC} + 0.5	Volts	D(15-0) and DQ(15-0) only
V_{IL}	Input Voltage Logic 0		-0.5		0.8	Volts	1
			-0.5		0.3 V_{CC}	Volts	1D(15-0) and DQ(15-0) only
T_A	Ambient Operating Temperature	Commercial	0		70	°C	Still Air
		Industrial	-40		+85	°C	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typical	Max	Units	Notes
I_{CC}	Average Power Supply Current			200	mA	tELEL = tELEL(min)
V_{OH}	Output Voltage Logic 1	2.4			Volts	I_{OH} = -8.0mA
V_{OL}	Output Voltage Logic 0			0.4	Volts	I_{OL} = 8.0mA
I_{IZ}	Input Leakage Current	-2		2	µA	$V_{SS} \leq VIN \leq V_{CC}$
		20	100	250	µA	$V_{IH} = V_{DD}$; 9
I_{OZ}	Output Leakage Current	-10		10	µA	$V_{SS} \leq V_{OUT} \leq V_{CC}$; DQ_N = HIGH Z

CAPACITANCE

Symbol	Parameter	Max	Units	Notes
C_{IN}	Input Capacitance	15	pF	f=1MHz, V_{IN} = 0 V.
C_{OUT}	Output Capacitance	15	pF	f=1MHz, V_{OUT} = 0 V.

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 Volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 Volts
Output Timing Reference Level	1.5 Volts

SWITCHING TEST FIGURES

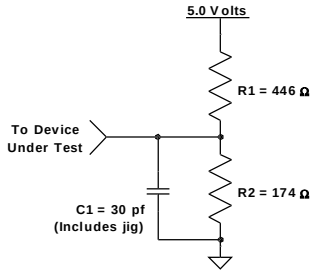


Figure 5: AC Test Load A

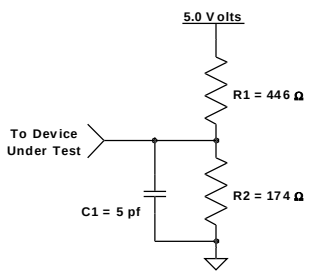


Figure 6: AC Test Load B

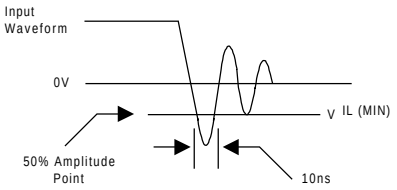


Figure 7: Input Signal Waveform

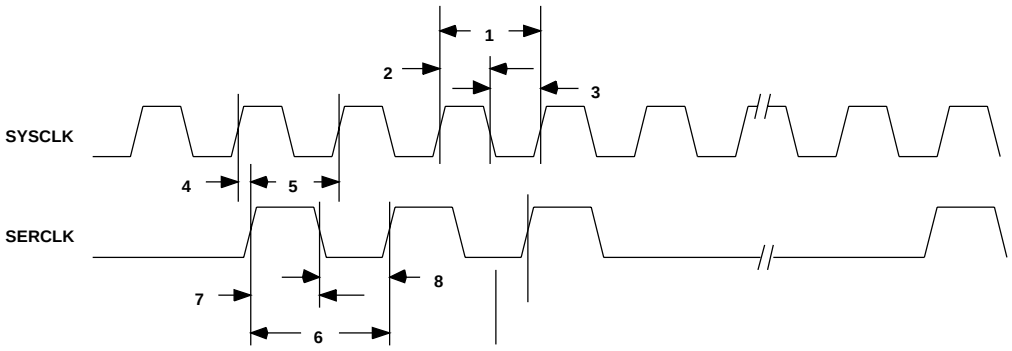
SWITCHING CHARACTERISTICS

No	Symbol	Parameter (all times in nanoseconds)	Min	Typ	Max	Notes
1	tKHKH	SYSCLK Period	30		50	
2	tKHKL	SYSCLK HIGH Pulse Width	0.4 · tKHKH		0.6 · tKHKH	
3	tKLKH	SYSCLK LOW Pulse Width	0.4 · tKHKH		0.6 · tKHKH	
4	tKHCH	SYSCLK HIGH to SERCLK HIGH Set-up Time	0			
5	tCHKH	SERCLK HIGH to SYSCLK HIGH Set-up Time	0			
6	tCHCH	SERCLK Period		100		
7	tCHCL	SERCLK HIGH Pulse Width	0.4 · tCHCH		0.6 · tCHCH	
8	tCLCH	SERCLK LOW Pulse Width	0.4 · tCHCH		0.6 · tCHCH	
9	tSLKH	Chip or Address Select LOW to SYSCLK HIGH Set-up	10			2
10	tSHKH	Chip or Address Select HIGH to SYSCLK HIGH Set-up	10			2
11	tSLSH1	Chip or Address Select LOW Pulse Width - Write Cycle	2 · tKHKH			
12	tAVSL	Address Bus VALID to Address Select LOW Set-up	5			
13	tSLAX	Address Select LOW to Address Bus INVALID Hold	10			
14	tWVKH	Write Enable LOW to SYSCLK HIGH Set-up Time	10			
15	tWVWX	Write Enable LOW Pulse Width	tKHKH			
16	tKHWH	SYSCLK HIGH to Write Enable HIGH Hold Time	10			
17	tDVKH	Data VALID to SYSCLK HIGH Set-up Time	10			
18	tKHDX	SYSCLK HIGH to Data INVALID Hold Time	10			
19	tKHRL	SYSCLK HIGH to Ready LOW Delay Time			30	
20	tKHRH	SYSCLK HIGH to Ready HIGH Delay Time			30	
21	tRLRH1	Ready LOW Pulse Width-Write Cycle		tKHKH		
22	tTHCH	SERDAT HIGH to SERCLK HIGH Set-up Time	10			
23	tCHTL	SERCLK HIGH to SERDAT LOW Hold Time	10			
24	tYLTV	NetReady LOW to SERDAT HIGH Set-up Time	10			3
25	tKHJL	SYSCLK HIGH to REJECT LOW Delay Time		11 · tKHKH		4
26	tKHDZ1	Chip or Address Select LOW Pulse Width-Read Cycle	2 · tKHKH			
27	tKHDV	SYSCLK HIGH to Data VALID Delay Time			30	7
28	tKHDZ	SYSCLK HIGH to Data HIGH-Z Delay Time			30	8
29	tRLRH2	Ready LOW Pulse Width-CAM Write Cycle	3 · tKHKH			
30	tKHEL	SYSCLK HIGH to CAM Enable LOW Delay Time			30	
31	tKHEH	SYSCLK HIGH to CAM Enable HIGH Delay Time			30	
32	tKHGV	SYSCLK HIGH to CAM Controls VALID Delay Time			30	5
33	tKHGX	SYSCLK HIGH to CAM Controls INVALID Delay Time			30	5
34	tEHML	CAM Enable HIGH to Match Flag LOW Delay Time			30	6
35	tRHSH	Ready HIGH to Chip or Address Select HIGH Set-up	5			
36	tSHDZ	Chip or Address Select HIGH to Data HIGH-Z Delay			30	
37	tKHDX	SYSCLK HIGH to Data Bus Active-Read	5			
38	tKHDV	SYSCLK HIGH to Data Bus VALID Delay Time			50	
39	tELQV	CAM Enable LOW to DQ Bus VALID-Read			85	6
40	tEHQZ	CAM Enable HIGH to DQ Bus HIGH-Z			20	6

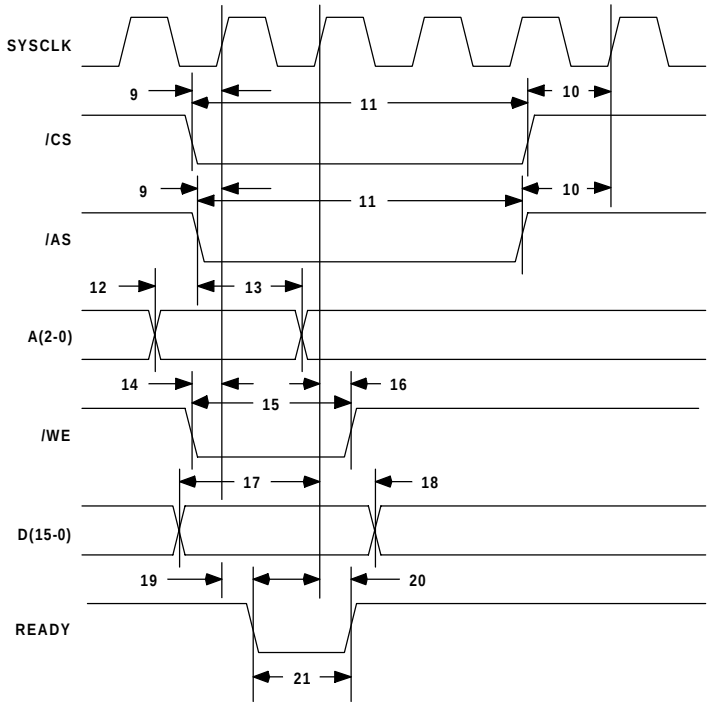
NOTES

1. -1.0 Volts for a duration of 10 ns measured at the 50% amplitude points for input-only lines (Figure 7).
2. If this timing parameter is violated, the read or write cycle will start one SYSCLK later (assuming /AS or /CS is held).
3. Before first network data pulse.
4. From the SYSCLK that strobed the last DA or SA segment into the LANCAM.
5. LANCAM Controls include /W, /CM, and /EC.
6. See the LANCAM Handbook for additional information on LANCAM Timing Specs.
7. With load specified in Figure 5.
8. With load specified in Figure 6.
9. Pin A(3)

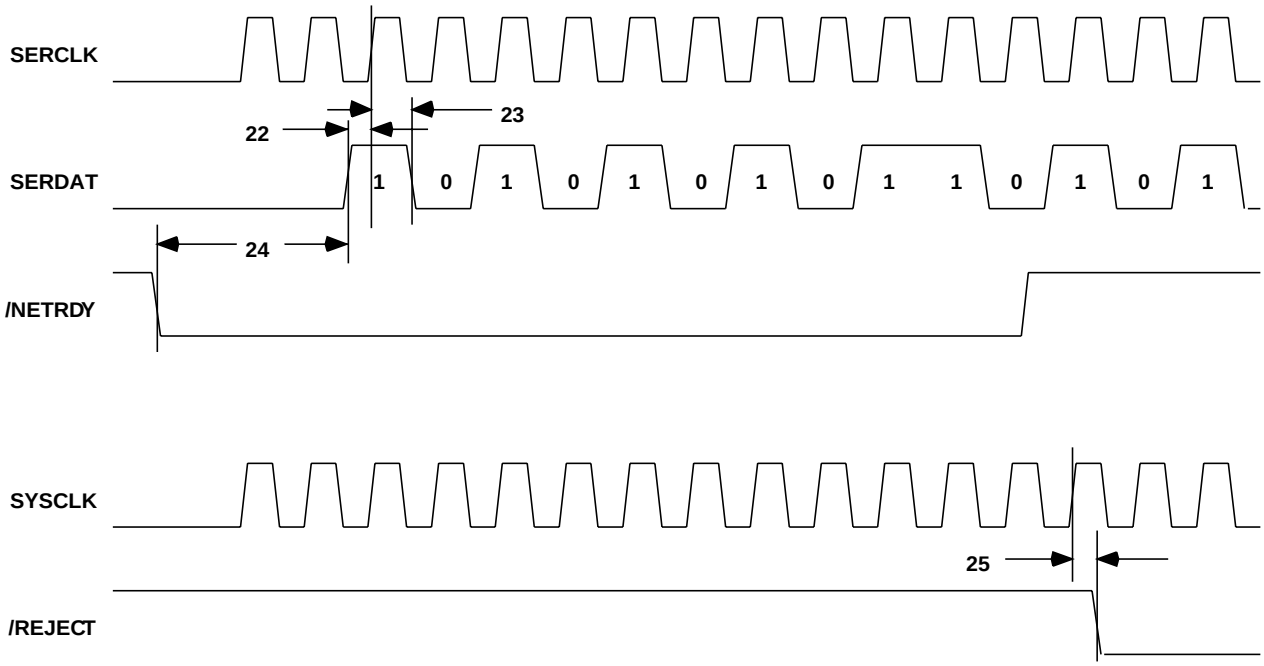
Clock Timing



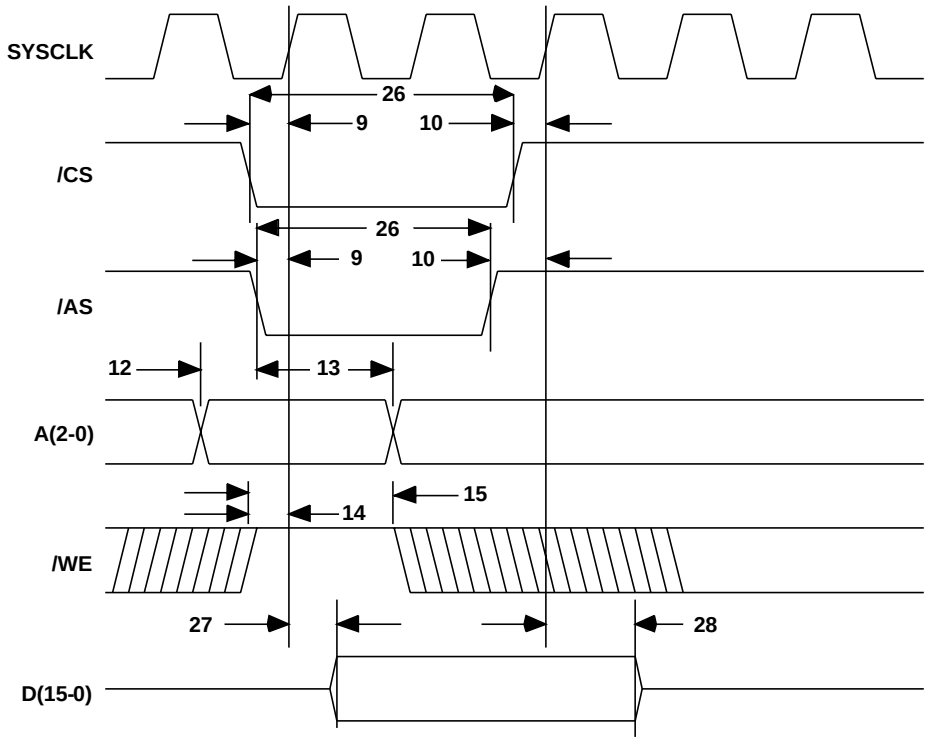
Processor Interface Write Cycle



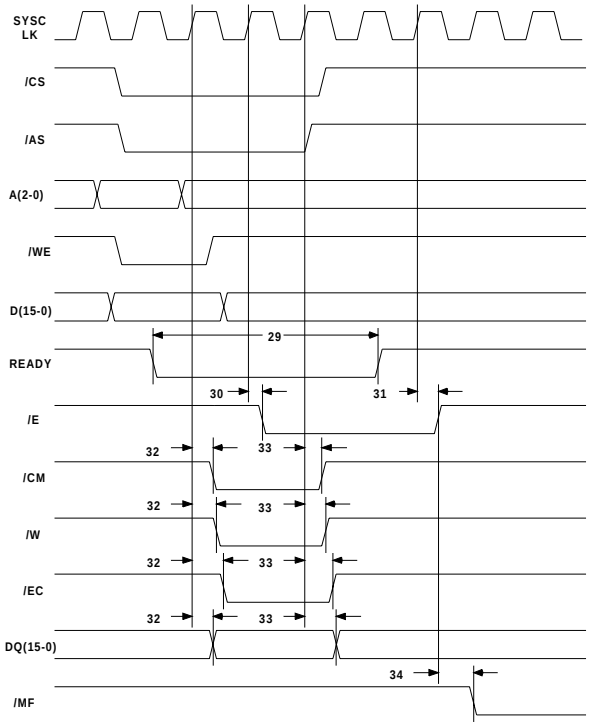
Network Interface Timing



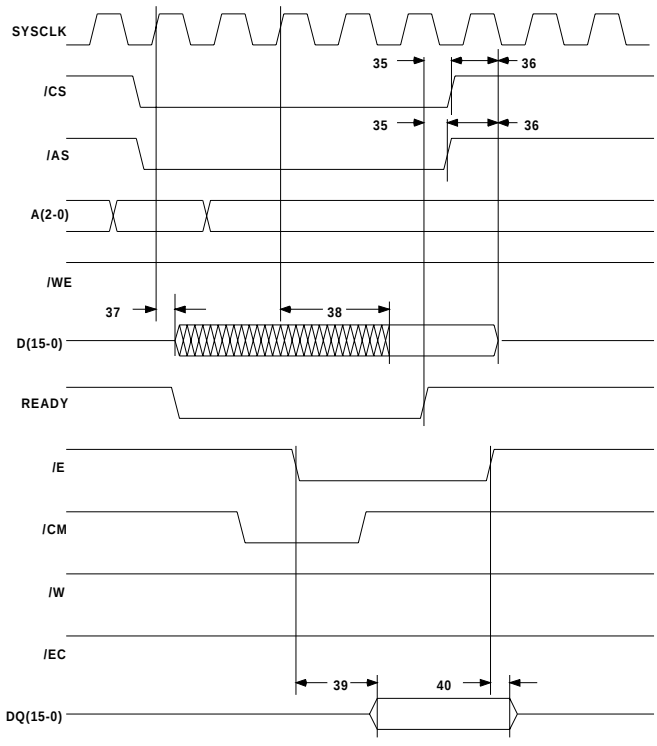
Processor Interface Read Cycle



Processor Interface Write Cycle to LANCAM



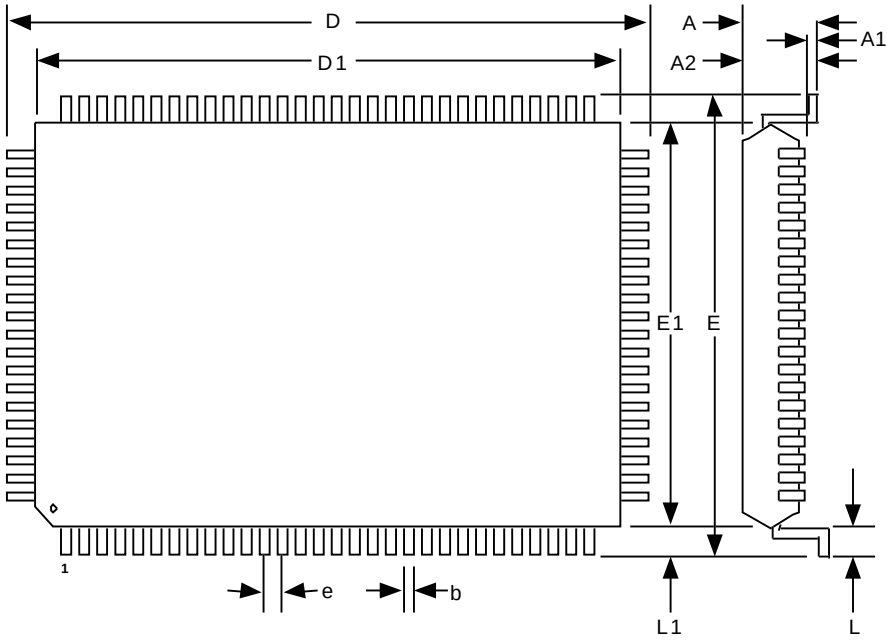
Processor Interface Read Cycle from LANCAM



ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	VOLTAGE
MU9C8328A - RDC	100-PIN PQFP	0–70° C	5.0 ± 0.5
MU9C8328A - RDI	100-PIN PQFP	-40– 85° C	5.0 ± 0.5

Package Outline



Dimensions are in mm.

	Dim. A	Dim. A1	Dim. A2	Dim. b	Dim. D	Dim. D1	Dim. a	Dim. E	Dim. E1	Dim. L	Dim. L1
100-pin PQFP	3.40	0.00	2.80	0.22	23.2	20.0	0.65	17.2	14.0	0.80	1.60
	Max	0.35	±0.25	0.38	±0.2	±0.2	Typ.	±0.2	±0.2	±0.15	Ref.

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