MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX018 UHF FM/FSK Receiver

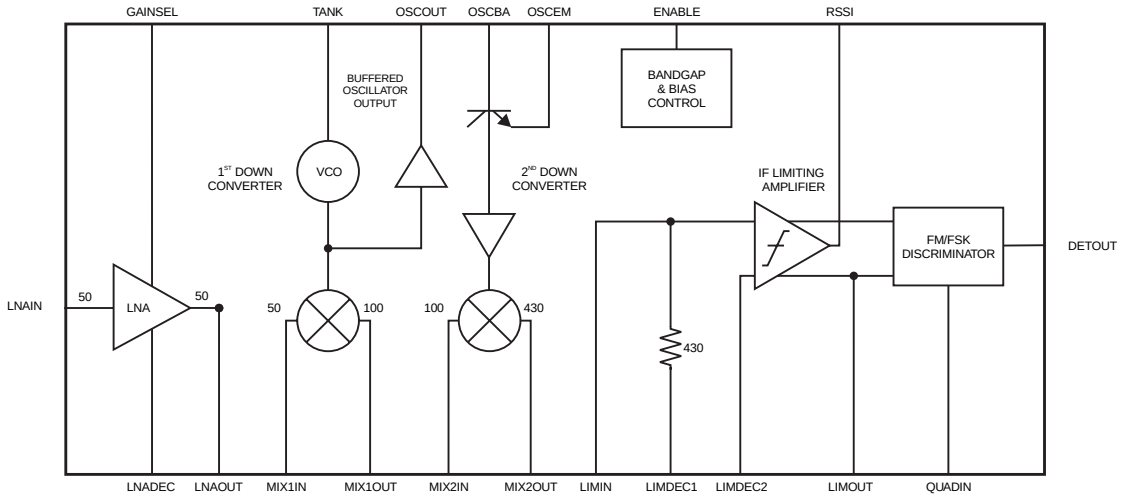
ADVANCE INFORMATION

Features

- **Double Conversion Super-Heterodyne Receiver and FM/FSK Demodulator**
- **LNA with Switched Gain**
- **High Performance UHF Down-Converter Stage with Integrated VCO**
- **2.7V Operation**
- **Zero-Power Mode (<10µA)**
- **Temperature Compensated RSSI**
- **28-Pin SSOP Package**

Applications

- **High Performance Analog/Digital Radio Links (860-965MHz)**
- **General ISM 915MHz Band**
- **Analog/Digital Cordless Phones**
- **Spread Spectrum Receivers**
- **Analog FM Receivers**
- **Handheld Data Terminals**
- **SO-HO Wireless Data Links**



The CMX018 is a single chip UHF FM/FSK double-conversion super-heterodyne receiver. It combines a dual gain mode Low Noise Amplifier (LNA), two down-converters (including integrated oscillators), limiting amplifier, RSSI, FM/FSK demodulator and zero-power mode control.

The CMX018 can be used in conjunction with the CMX017, an integrated FM/FSK modulator and transmitter, to implement a complete UHF radio link.

The CMX018 operates from a 2.7V to 3.3V power supply and is available in the following package style: 28-pin SSOP (CMX018D6).

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1 Internal Block Diagram

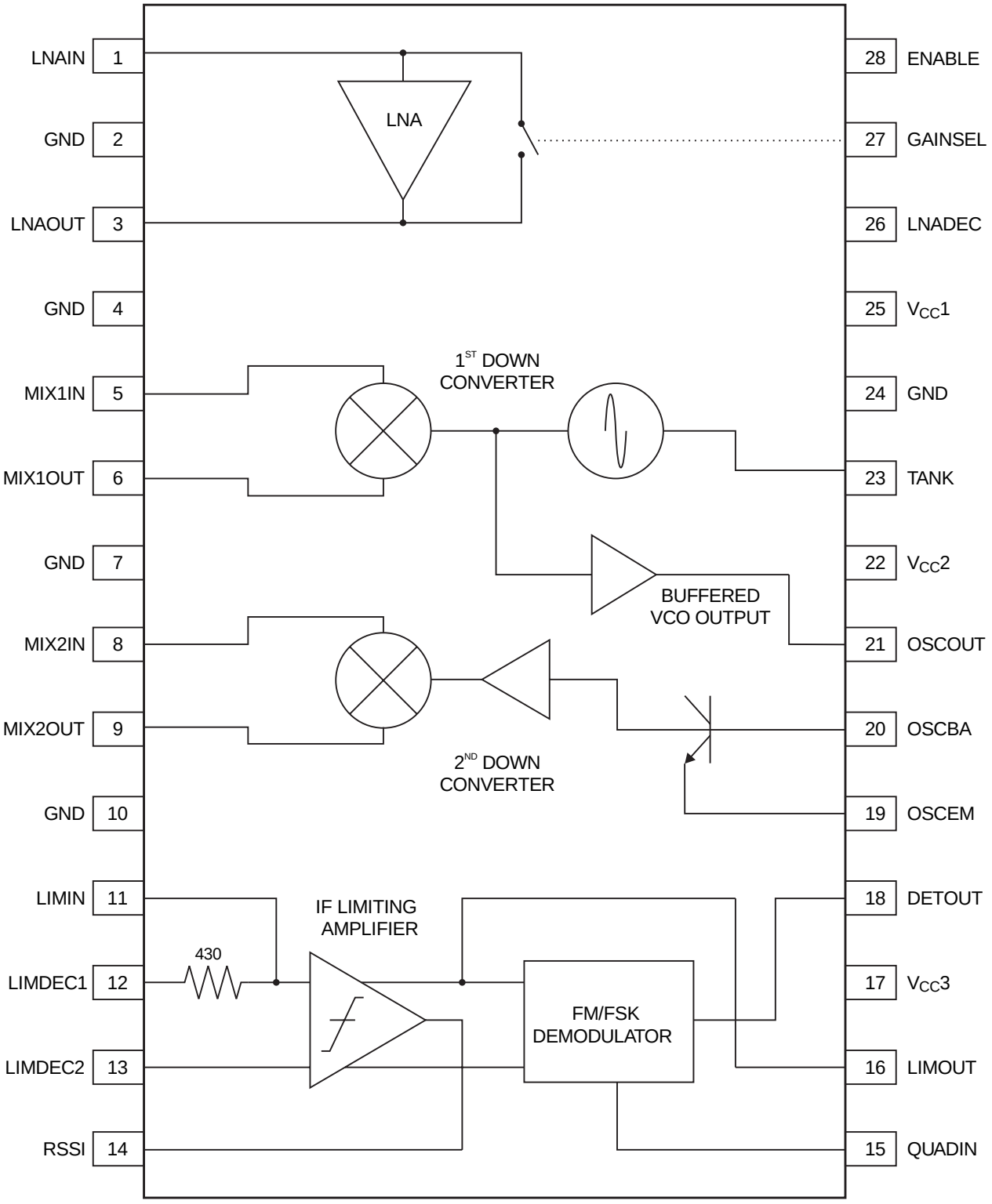


Figure 1: Internal Block Diagram

2 Signal List

Pin No.	Signal		Description
Package D6	Name	Type	
1	LNAIN	input	LNA RF Input
2	GND	ground	LNA Ground connection
3	LNAOUT	output	LNA RF Output
4	GND	ground	LNA Ground connection
5	MIX1IN	input	RF Input to the First Down-Converter
6	MIX1OUT	output	IF Output from the First Down-Converter
7	GND	ground	First Down-Converter Ground connection
8	MIX2IN	input	RF Input to the Second Down-Converter
9	MIX2OUT	output	IF Output from the Second Down-Converter
10	GND	ground	Second Down-Converter, Limiting Amplifier, RSSI, and Demodulator stages - Ground connection
11	LIMIN	input	Input to the Limiting Amplifier
12	LIMDEC1	input	External Decoupling capacitors – one required at each limiting Amplifier Inputs
13	LIMDEC2	input	
14	RSSI	output	Receive Signal Strength Indicator output
15	QUADIN	input	Quadrature input to the FM Demodulator
16	LIMOUT	output	Output from the Limiting Amplifier
17	Vcc3	power	Power supply to the Second Down-Converter, Limiting Amplifier, RSSI and Demodulator stages – nominally 3.0V
18	DETOUT	output	Output of the FM/FSK Quadrature Demodulator
19	OSCEM		Emitter connection to the Second Down-Converter Local Oscillator transistor
20	OSCBA		Base connection to the Second Down-Converter Local Oscillator transistor
21	OSCOUT	output	Buffered Local Oscillator (Open-Collector) output from the First Down-Converter
22	VCC2	power	First Down-Converter 3V Supply
23	TANK	input	First Down-Converter Local Oscillator (VCO) TANK/Resonator connection
24	GND	ground	First Down-Converter VCO Ground connection
25	VCC1	power	LNA Power Supply – nominally 3.0V
26	LNADEC		External LNA bias decoupling capacitor
27	GAINSEL	CMOS input	LNA Gain control logic input. A logic ‘0’ provides a typical power gain of 16dB and a logic ‘1’ provides an attenuation of 6dB
28	ENABLE	CMOS input	Zero-Power logic control. A logic ‘0’ powers down the device.

Table 1: Signal List

3 External Components

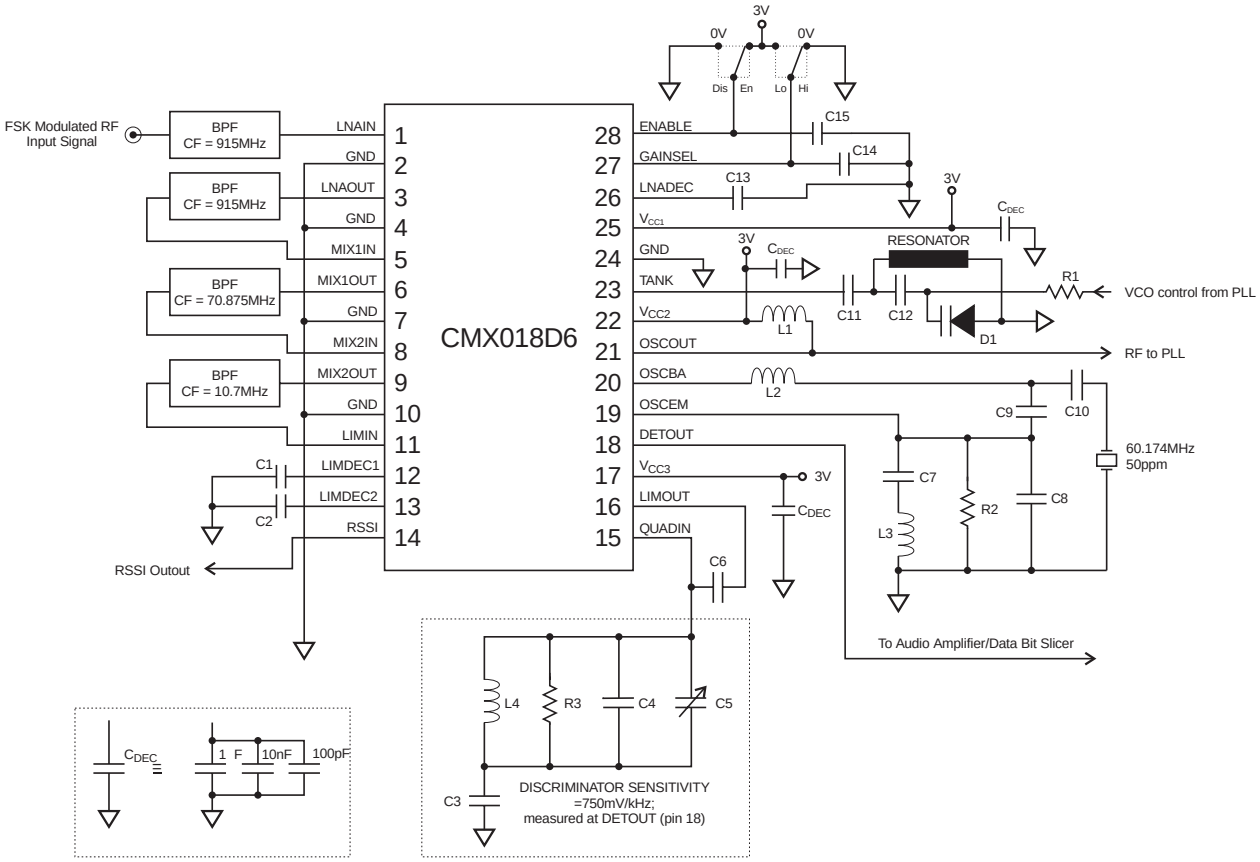


Figure 2: Example of CMX018 with External Components

C1	100nF		C15	100pF	
C2	100nF		D1	Varactor	Varactor diode, type SMV1233-011
C3	100nF		~	Resonator	Co-Axial Resonator, type RG402, length = 11mm, shorted end
C4	200pF		L1	22nH	
C5	8 – 50pF Trimmer		L2	680nH	
C6	5pF		L3	680nH	
C7	220pF		L4	1µH	
C8	6.8pF		R1	10kΩ	
C9	15pF		R2	10kΩ	
C10	33pF		R3	2.0kΩ	Value is application dependent
C11	4.7pF				
C12	6.2pF		X1	60.175MHz	50ppm crystal
C13	10nF				
C14	100pF				

Note: Components are surface mount, type SMD0603, unless otherwise indicated.

Table 2: Example of CMX018 with External Components

4 General Description

The CMX018 is a single chip UHF FM/FSK double-conversion super-heterodyne receiver. It combines a dual gain mode Low Noise Amplifier (LNA), two down-converters (including integrated oscillators), limiting amplifier, RSSI, FM/FSK demodulator and zero-power mode control.

The receiver frequency is selected using an external PLL or synthesizer, which is driven by the buffered RF oscillator signal from the first down-converter.

The CMX018 can be used in conjunction with the CMX017, an integrated FM/FSK modulator and transmitter, to implement a complete UHF radio link.

4.1 Low Noise Amplifier

The LNA includes a switched gain function, which is used to increase the dynamic range of the receiver. The gain is selected using the GAINSEL logic input at pin 2. With a logic '0' at the GAINSEL input a high gain is selected and the amplifier achieves the lowest noise figure. This mode is used where maximum sensitivity is required for low level input signals. Where high level signals are present at the receiver input, which cause difficulties due to inter-modulation, the gain of the LNA can be reduced by typically 22dB from about +16dB to about –6dB. The attenuation is selected by applying a logic '1' at the GAINSEL input; this minimizes the amount of non-linear distortion in the overall receiver at the expense of small signal sensitivity. The input and output impedances of the LNA are typically 50Ω.

4.2 First Down-Converter

The first down-converter includes a double balanced mixer with a low noise pre-amplifier, and on-chip oscillator components. The oscillator is configured as a 'high-sided' voltage controlled local oscillator, using an external varicap diode and tank resonator circuit, such that the first IF is typically centered at 70MHz. A buffered oscillator signal (OSCOUT at pin 21) is provided to drive the frequency synthesizer which controls the frequency tuning. The input impedance is typically 50Ω and the output impedance is typically 100Ω.

4.3 Second Down-Converter

The second down-converter also includes a double balanced mixer with a low noise pre-amplifier, and on-chip oscillator components. The oscillator is configured as a 'low-sided' local oscillator, using an external crystal at typically 60MHz, such that the second IF is centered at 10.7MHz. The input impedance is typically 100Ω and the output impedance is typically 430Ω.

4.4 Limiting Amplifier and RSSI

The limiting amplifier provides the IF amplification and limiting prior to the FM/FSK demodulator. An RSSI circuit is included which has temperature compensation. An RF signal level of -100dBm at the LNA input will produce an RSSI voltage of typically TBD mV. The RSSI voltage will increase with increasing RF input level at a rate of 20mV/dB up to a typical voltage of TBD V at a -60dBm RF input. In practice the absolute RSSI voltage will depend upon the insertion losses associated with each of the IF filters. The input impedance is typically 430Ω.

4.5 FM/FSK Demodulator

A quadrature detector is employed together with an external discriminator and phase shift network to demodulate the FM or FSK signal.

4.6 Zero-Power Mode

The device is powered down by applying a logic '0' level at the ENABLE input (pin 28). In this mode the device current is reduced to less than 10μA. This feature is useful when the device is operating within a transceiver where the receiver needs to be enabled and disabled.

A delay should be allowed for the receiver to settle after power-up. This is likely to be less that the crystal oscillator stabilization time, which may be altered by adjusting the value of R2, shown in Figure application.

5 Application Notes

5.1 General

Example Schematic and Layout

The following schematic (Figure 3) and printed circuit layout (Figure 4 and Figure 5) show a typical application interface for the CMX018. To aid legibility, the schematic and layout are available electronically from the MX-COM website http://www.mxcom.com**.**

Alternative components and component values are shown on the schematic. These should be selected according to the intended application. The schematic uses the following ICs:

U2	Motorola	MC34072D-SO8
U3	IC Works	WB1315X
U4	Analog Devices	AD8532-SO8

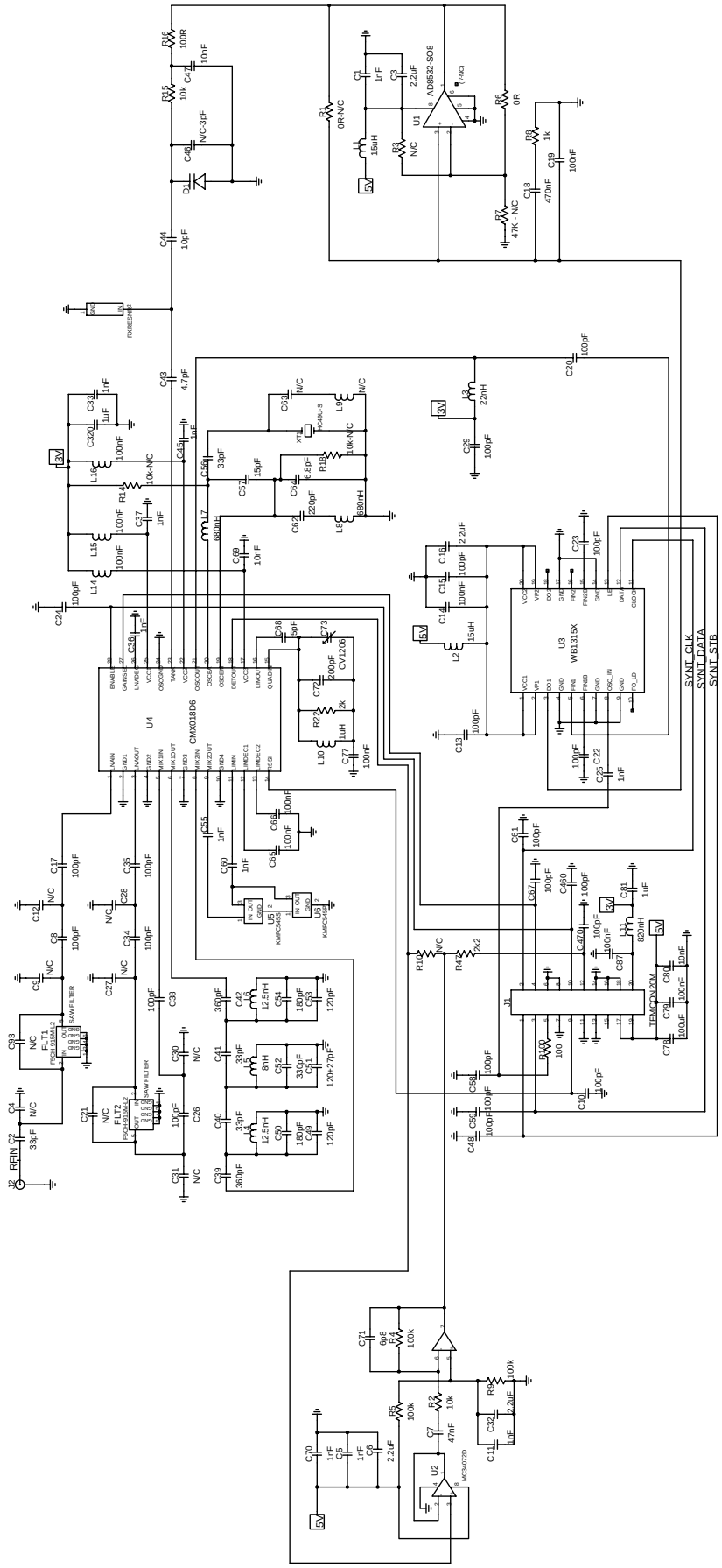


Figure 3: Application Schematic

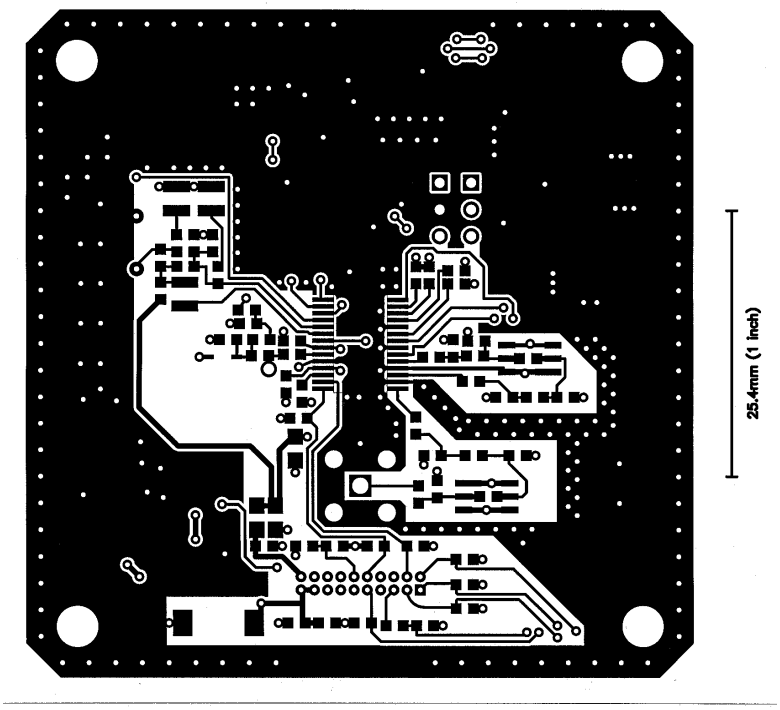


Figure 4: Application Layout - Top Copper

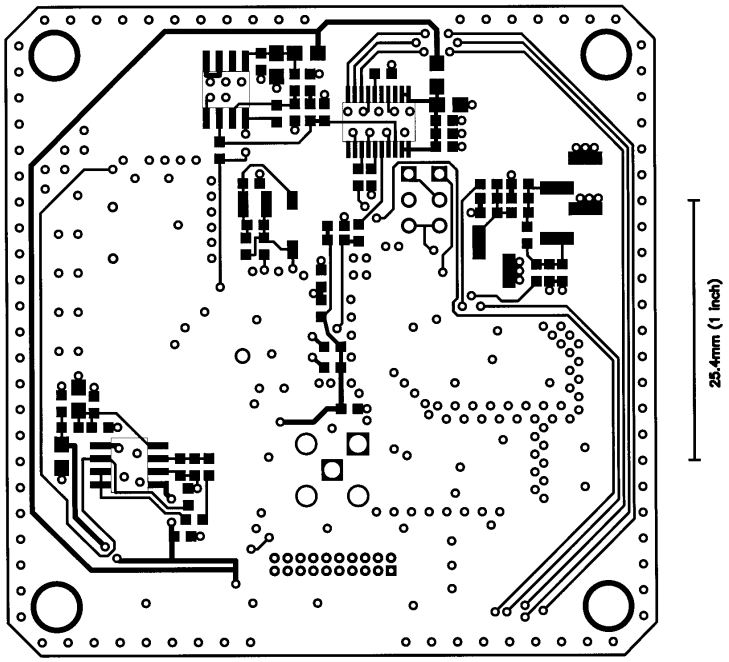


Figure 5: Application Layout - Bottom Copper (not reversed)

Available from **http://www.mxcom.com**.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Pins	Min.	Max.	Units
Supply Voltage (V_{CC})	17, 22, 25	-0.3	7.0	V
Input Voltage	27, 28	-0.3	V_{CC} + 0.3	V
LNA Input Power	1		0	dBm
D6 Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			550	mW
Derating above 25°C			9	mW/°C above 25°C
Storage Temperature		-55	+125	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply Voltage (V_{CC})		2.7	3.3	V
RF Input Range		860	965	MHz
Operating Temperature		-10	+60	°C

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{CC} = 2.7V to 3.3V, T_{AMB} = - 10°C to +60°C,
RF = 915MHz, 50Ω source and load impedance.

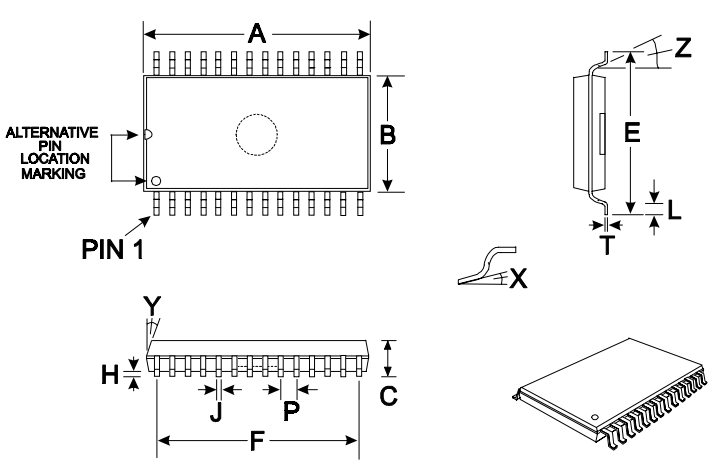
	Pin	Note	Min.	Typ.	Max.	Units
DC Parameters						
I_{CC} (ENABLE = V_{CC} and GAINSEL = 0V)	17, 22, 25			50		mA
I_{CC} (ENABLE = V_{CC} and GAINSEL = V_{CC})	17, 22, 25			42		mA
I_{CC} (ENABLE = 0V)	17, 22, 25				10	µA
AC Parameters						
LNA (RF = 915MHz)						
Power Gain (GAINSEL = 0V)	1, 3			16		dB
Power Gain (GAINSEL = V_{CC})	1, 3			-6.0		dB
Noise Figure	1, 3			3.0		dB
Input 1dB Gain Compression Point (GAINSEL = 0V)	1			-20		dBm
Input 1dB Gain Compression Point (GAINSEL = V_{CC})	1			16		dBm
Input Third Order Intercept Point (GAINSEL = 0V)	1			-10		dBm
Input Third Order Intercept Point (GAINSEL= V_{CC})	1			25		dBm
Reverse Isolation (GAINSEL = 0V)	3, 1			-35		dB
Reverse Isolation (GAINSEL = V_{CC})	3, 1			-6.0		dB
Input Impedance	1			50		Ω
Output Impedance	3			50		Ω
Input Return Loss (50Ω source)	1			*10*		dB
Output Return Loss (50Ω load)	3			*15*		dB
VCO to LNA Leakage	1			-45		dBm
First Down Converter (RF = 915MHz and IF = 70MHz)						
Conversion Gain	5, 6			15		dB
Noise Figure	5, 6			15		dB
Input 1dB Gain Compression Point	6			-12		dBm
Input Third Order Intercept Point	6			-4.0		dBm
Input Impedance	5			50		Ω
Output Impedance	6			100		Ω
Input Return Loss (50Ω source)	5			TBD		dB
Output Return Loss (50Ω load)	6			TBD		dB
Buffered oscillator output power	21			-10		dBm
RF to IF Leakage	5, 6			TBD		dB
LO to IF Leakage	6			TBD		dBm
LO to RF Leakage	5			TBD		dBm

	Pin	Note	Min.	Typ.	Max.	Units
Second Down Converter (RF = 70MHz and IF = 10.7MHz)						
Conversion Gain	8, 9			24		dB
Noise Figure	8, 9			13		dB
Output 1dB Gain Compression Point	9			-11		dBm
Output Third Order Intercept Point	9			-2		dBm
Input Impedance	8			100		Ω
Output Impedance	9			430		Ω
Limiting Amplifier and RSSI (IF = 10.7MHz)						
Bandwidth	11, 16			40		MHz
Internal Voltage Gain	11			74		dBV
Input Impedance	11			430		Ω
RSSI Dynamic Range	14			*TBD*		dB
RSSI Slope	14			*TBD*		V/dB
RSSI Voltage Range	14	1		*TBD*		V
Demodulator (IF = 10.7MHz)						
Output Swing	18	2		*TBD*		MV_{P-P}
Output Impedance	18			1		kΩ

Notes:

1. Input power = TBD to TBD
2. 125kHz Deviation, 1kΩ Load

6.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A	0.396 (10.06)		0.407 (10.34)
* B	0.205 (5.21)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
F		0.333 (8.45)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.56)		0.037 (0.94)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.23)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 28-Pin Plastic SSOP Mechanical Outline: *Order as part no. CMX018D6*

6.3 Handling Precautions

This device is a high performance RF integrated circuit and is ESD sensitive.
Adequate precautions must be taken during handling and assembly of this device.

