MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX214/224

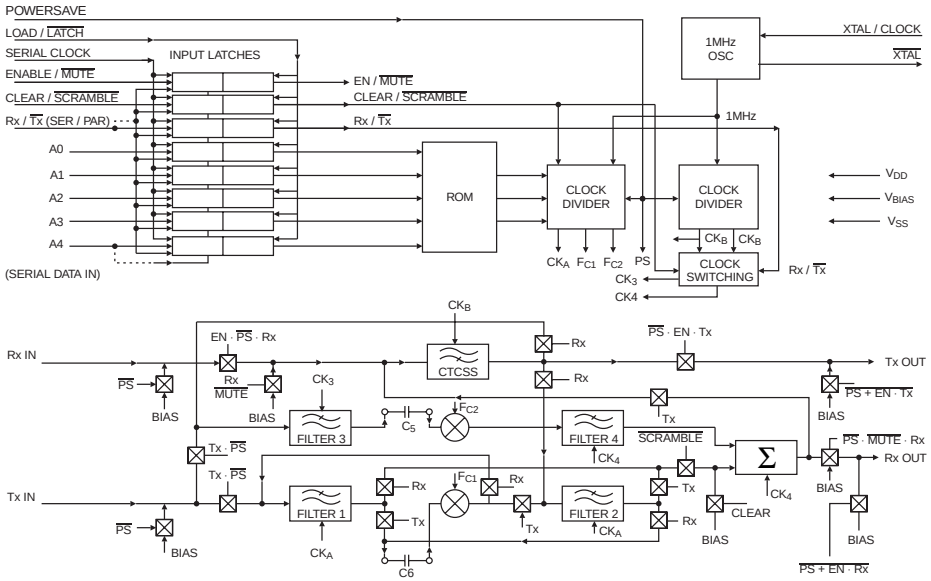
Variable Split Band Inverter

Features

- **CTCSS Highpass Filter**
- **Good Recovered Audio Quality**
- **Fixed and Rolling Code Modes**
- **Serial (MX214) and Parallel (MX224) Loading Options**
- **32 Programmable Split Points**
- **Half-Duplex Capability**

Applications

- **Mobile Radio Voice Security**
- **Cellular Telephone Voice Security**



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The MX214/224 ICs include a highpass filter that rejects subaudio frequencies, ensuring full CTCSS compatibility. This CTCSS filter is not included on the earlier generation MX204 VSB Inverter.

The MX214/224 splits the voiceband (300-2700Hz) into upper and lower subbands, and inverts each subband about itself. The 'split point' (defined as the frequency where the voice band is subdivided), is externally programmable to 32 distinct values in the 300 to 3000Hz range. In the 'fixed code' mode, a single point is used. Fixed mode operation nets approximately 4 mutually exclusive secure channels.

In 'rolling code' mode, the split point is changed many times per second, usually under control of a microprocessor. Rolling code scrambling requires synchronization, offers higher security than fixed code operation, and provides a much greater number of mutually exclusive secure channels.

The MX214/224 offers a recovered audio product close to that of a telephone. The on-chip ' Mute' function is useful when implementing rolling code continuous synchronization schemes. 'Powersave' and 'Clear/Scramble' controls are also included on-chip. Timing and filter clocks are derived internally from an on-chip 1MHz reference oscillator driven by a 1MHz crystal or clock pulse input.

The MX214 and the MX224 operate from a single 5.0V supply and available in the following packges: 22-pin CDIP (MX214J/MX224J), 22-pin PDIP (MX214P/MX224P), and 24-pin PLCC (MX214LH/MX224LH).

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MX-COM, Inc. reserves the right to change specifications at any time without notice.

1. Block Diagram

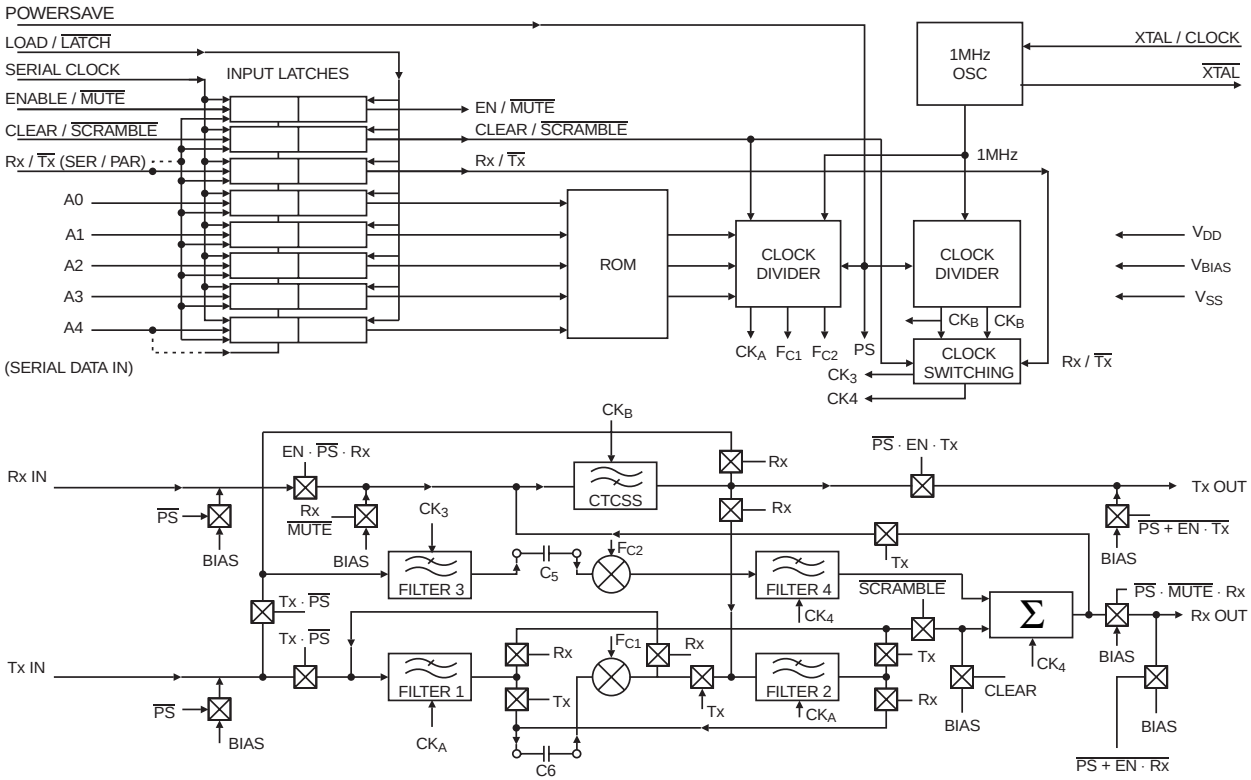

Figure 1: Block Diagram

2. Signal List

MX214 Pin No.		MX224 Pin No.		Signal Name	Description
J/P	LH	J/P	LH		
7	1	1	1	Xtal/Clock	Input to the clock oscillator inverter. A 1MHz crystal input or externally derived 1MHz clock is injected here.
8	2	2	2	$\overline{\text{Xtal}}$	Output of the clock oscillator inverter.
9	3			Serial Data Input	This pin is used to input an 8-bit word representing the digital control functions. This word is loaded using the serial data clock and in input in the following sequence: MUTE, CLEAR, Rx/$\overline{\text{Tx}}$, A0, A1, A2, A3, A4. The Load/$\overline{\text{Latch}}$ is operated on the completion. Reference the timing diagram in Figure 8.
		3 – A4 4 – A3 5 – A2 6 – A1 7 – A0	3 – A4 4 – A3 5 – A2 6 – A1 7 – A0	Programming Inputs	In parallel mode, these five digital inputs define the split point frequency. Each of the 5 input pins has a 1MΩ internal pull-up resistor. See Table 4 for programming information.
		8	8	Rx/$\overline{\text{Tx}}$	This digital input selects the Receive and Transmit paths and configures upperband and lowerband filter bandwidths while setting the CTCSS highpass filter position on the signal path. See Table 2, Figure 6, and Figure 7. 1MΩ internal pull-up resistor (Rx).
13	8			Parallel/$\overline{\text{Serial}}$	This pin must be connected to V_{SS} for serial loading. Internal 1MΩ pull-up resistor.
		9	9	Clear/Scramble	This digital input puts the device into 'Clear' or 'Scramble' mode by controlling the application of carrier frequency to the Upper and Lower band balanced modulators. In 'Scramble' mode, the balanced modulator carrier frequency values are selected by the split point address A0-A4. See Table 4. In 'Clear' mode, the carriers are disabled and the balanced modulators are bypassed internally, i.e. the lower band signal is not added to the output signal. 1MHz internal pull-up resistor (Clear).
		10	10	Enable/Mute	This digital function is used to disable the Receive or the Transmit signal paths for rolling code synchronization while maintaining bias conditions. Synchronization data can be transmitted during the Mute periods, as is done in the MX1204 VSB Scrambler Module. 1MΩ Internal pull-up resistor (Enable)
14	10			Serial Clock Input	This is the externally applied data clock frequency used to shift input data along in devices wired in the Serial-loading mode. One full data clock cycle is required to shift one data bit completely into the register. See Timing Diagram Figure 8. 1MΩ Internal pull-up resistor.

MX214 Pin No.		MX224 Pin No.		Signal Name	Description
J/P	LH	J/P	LH		
15	11	11	11	Load/$\overline{\text{Latch}}$	This pin controls the loading of the 8 digital function inputs (ENABLE, CLEAR, A0-A4) into the internal register. When this pin is at a logic '1', all eight inputs are transparent and new data acts directly. For controlled changing of parameters in the parallel, Load/$\overline{\text{Latch}}$ must be kept at logic '0' while a new function is loaded, then strobed 0-1-0 to latch the inputs in. For serial loading, the serial data should be loaded with the Load/$\overline{\text{Latch}}$ at logic '0' and then the Load/$\overline{\text{Latch}}$ strobed 0-1-0 on completion of data loading. Internal 1MΩ pull-up resistor (Load). See Figure 8.
16	12	12	12	Powersave	This digital input is used to place the MX214/224 into Powersave mode where all parts of the device except the 1MHz oscillator are shut down. All signal input and output lines are made open circuit, free of all bias. This allows signal paths to be routed externally around the device, while reducing current consumption. A logic '0' at this input enables the device to work normally as shown in Table 2. Internal 1MΩ pull-up resistor.
17	13	13	13	V_{SS}	Negative supply (GND)
18	14	14	14	Internal connection	This pin is internally connected. Leave open circuit.
19	15	15	15	Rx Output	This is the processed received audio signal output. This pin is held at a DC 'bias' voltage for all functions except Powersave. This buffered output is driven by the summing circuit in the Rx mode. Signal paths and bias levels are detailed in Table 2 and Figure 7.
20	16	16	16	Tx Output	This is the processed audio output for the transmission channel. This pin is held at a DC 'bias' voltage for all functions except Powersave. This summed and buffered signal is passed through the CTCSS high pass Filter to the output pin in the Tx Mode. Signal paths and bias levels are detailed in Table 2 and Figure 6.
21	17	17	17	V_{BIAS}	Normally at $V_{DD}/2$, this pin requires an external decoupling capacitor (C7) to V_{SS}.
22	18	18	18	Rx Input	This is the analog received signal input. This pin is held at a DC 'bias' voltage by a 300kΩ on-chip bias resistor, which is selected for all functions except Powersave. It must be connected to external circuitry by capacitor C3. See Figure 2 and Figure 3. This input is routed through the CTCSS High Pass Filter in Rx mode to remove subaudio frequencies from the voiceband. Signal paths and bias levels are detailed in Table 2 and Figure 7.
1	19	19	19	Highband Filter Output	The output of the Input Filter of the Upperband limit. The Rx/$\overline{\text{Tx}}$ functions sets the lowpass filter at 3400Hz or 2700Hz respectively. This output must be connected to the Highband Balanced modulator input via capacitor C5. See Figure 2 and Figure 3.

MX214 Pin No.		MX224 Pin No.		Signal Name	Description
J/P	LH	J/P	LH		
2	20	20	20	Highband Balanced Modulator Input	The input to the Balanced Modulator of the Upperband limit. This input must be connected to the Highband Filter Output via capacitor C5. See Figure 2 and Figure 3.
3	21	21	21	Lowband Balanced Modulator Input	The input to the Balanced Modulator of the Lowerband limit. This input must be connected to the Lowband Filter Output via capacitor C6. See Figure 2 and Figure 3.
4	22	22	22	Tx input	This analog 'Clear' audio input for the VSB Scrambler. This pin is held at a DC 'bias' voltage by a 300kΩ on-chip bias resistor, which is selected for all functions except powersave. In must be connected to external circuitry by capacitor C4. See Figure 2 and Figure 3. This input, in Tx mode, is connected to Upper and Lowerband input filters. Signal paths and bias levels are detailed in Table 2 and Figure 6.
5	23	23	23	Lowband Filter Output	The output of the Input filter of the lowerband limit. The $Rx/\overline{Tx}$ function determines which filter is used (Filter 1 or 2). See Figure 6 and Figure 7. This output must be connected to the Lowband balanced modulator input via capacitor C6. See Figure 7.
6	24	24	24	V_{DD}	A single 5.0V supply is required.
10, 11, 12			4, 5, 6, 7, 9	N/C	No Connection

Table 1: Signal List

	$Rx/\overline{Tx}$ = 1	**$Rx/\overline{Tx}$ = 0**	**MUTE = 0**	**POWERSAVE**
Rx Path	Enabled	Disabled	Disabled	Disabled
Rx Out Level	Bias	Bias	Bias	High Impedance
Tx Path	Disabled	Enabled	Disabled	Disabled
Tx Out Level	Bias	Bias	Bias	High impedance

Table 2: Functions Influencing Signal Paths

3. External Components

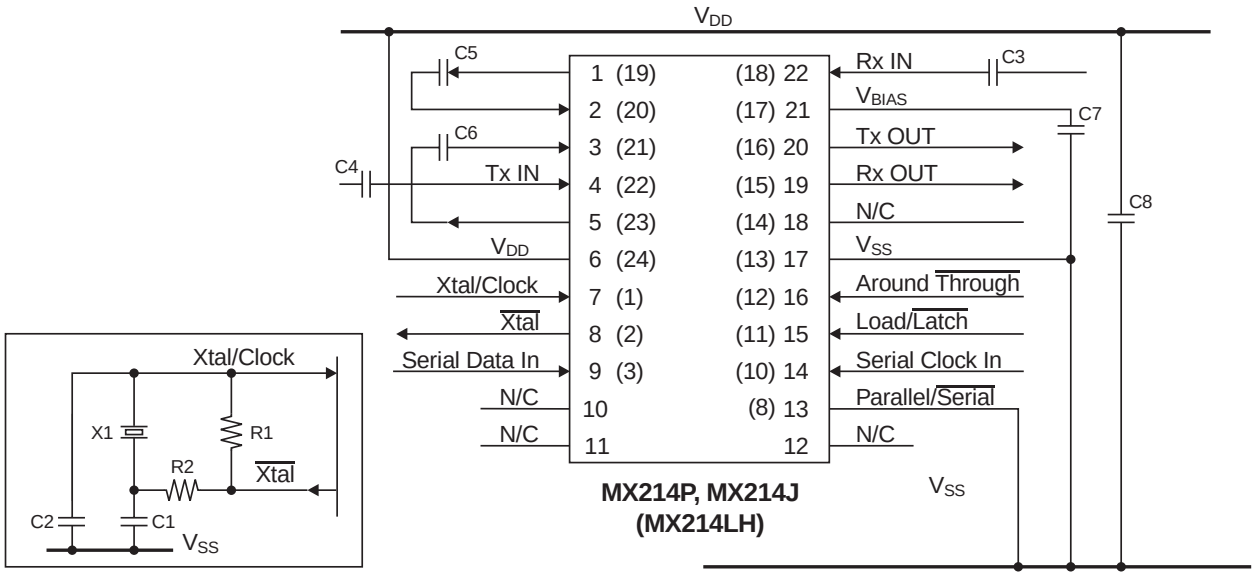

Figure 2: Recommended External Components 'MX214 Serial Loading'

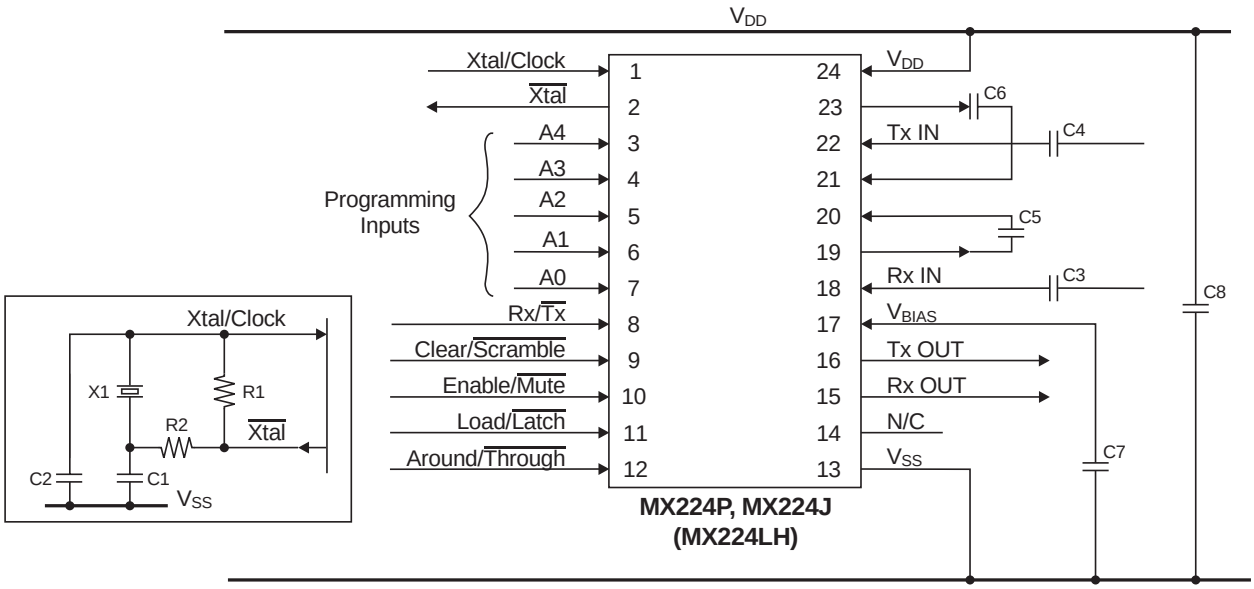

Figure 3: Recommended External Components 'MX224 Parallel Loading'

Component	Notes	Value	Tolerance
R1		1.0MΩ	±10%
R2		Selectable	
C1		33pF	±20%
C2		68pF	±20%
C3		15nF	±20%
C4		15nF	±20%
C5	1	1.0µF	±20%
C6	1	1.0µF	±20%
C7		1.0µF	±20%
C8		1.0µF	±20%
X1	2	1MHz	

Table 3: Recommended External Components

Notes:

1. C5 and C6 are coupling capacitors between filter outputs and balanced modulator inputs.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

The MX214/224 Variable Split Band Inverters are designed for mobile and cellular radio voice security applications. Digital control functions are loaded serially into the MX214. The MX224 is loaded in parallel.

The MX214/224 ICs include a highpass filter that rejects subaudio frequencies, ensuring full CTCSS compatibility. This CTCSS filter is not included on the earlier generation MX204 VSB Inverter.

The MX214/224 splits the voiceband (300-2700Hz) into upper and lower subbands, and inverts each subband about itself. The 'split point' (defined as the frequency where the voice band is subdivided), is externally programmable to 32 distinct values in the 300 to 3000Hz range. In the 'fixed code' mode, a single point is used. Fixed mode operation nets approximately 4 mutually exclusive secure channels.

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The MX214/224 offers a recovered audio product close to that of a telephone. The on-chip ' Mute' function is useful when implementing rolling code continuous synchronization schemes. 'Powersave' and 'Clear/Scramble' controls are also included on-chip. Timing and filter clocks are derived internally from an on-chip 1MHz reference oscillator driven by a 1MHz crystal or clock pulse input.

5. Application

The MX214 represents both the MX214 and the MX224 throughout this section.

Recommended external components are shown in Figure 2 and Figure 3. In 'Scramble' mode, split point frequencies are selected and set in accordance with the ROM address code present at the inputs A0-A4. See Table 4. In 'Clear' mode, both upper and Lowerband filter limits are used (see Figure 6 and Figure 7), the carrier frequencies are turned off, and the balanced modulators are bypassed internally. The Lowband audio is removed from the output signal prior to summing.

ROM Address A4-A0	Split Point Hz	Low Band Carrier, Hz f_{C1}	High Band Carrier, Hz f_{C2}	ROM Address A4-A0	Split Point Hz	Low Band Carrier, Hz f_{C1}	High Band Carrier, Hz f_{C2}
00000	2800	3105	6172	10000	1135	1436	4504
00001	2625	2923	6024	10001	1050	1351	4424
00010	2470	2777	5813	10010	976	1278	4347
00011	2333	2631	5681	10011	913	1213	4310
00100	2210	2512	5555	10100	857	1157	4273
00101	2100	2403	5494	10101	792	1094	4166
00110	2000	2304	5376	10110	736	1037	4132
00111	1909	2212	5263	10111	688	988	4065
01000	1826	2127	5208	11000	636	936	4032
01001	1750	2049	5102	11001	591	891	3968
01010	1680	1984	5050	11010	552	853	3937
01011	1555	1858	4950	11011	512	813	3906
01100	1448	1748	4807	11100	471	772	3846
01101	1354	1655	4716	11101	428	728	3816
01110	1272	1572	4629	11110	388	688	3787
01111	1200	1501	4587	11111	350	650	3731

Table 4: ROM Address Programming

The MUTE function disables the MX214/224's audio outputs to allow periodic transmission of synchronization data. A logic '0' at this input isolates the device while leaving the audio input and output ins at bias level (See Table 2). When the MX21/224 is in Powersave mode, audio signals may be hardwired around the device since the input and output pins are open circuit. See Table 2.

5.1 Audio Quality

Figure 4 shows the recommended basic audio system layout using pre- and de-emphasis circuitry to maintain good recovered speech quality. The Transmit mode, ***Do Not*** pre-emphasize the audio output of the MX214. In the Receive mode, de-emphasis should be used after the MX214.

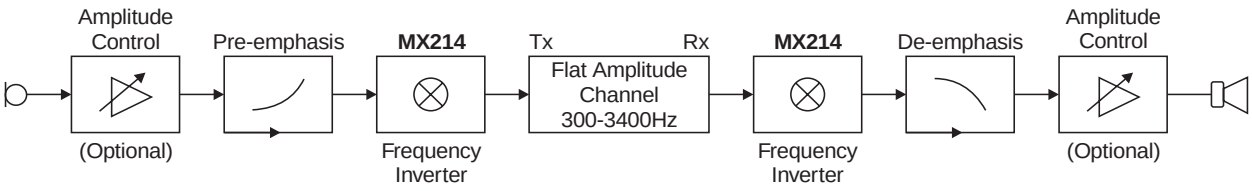


Figure 4: Recommended Basic Communication Audio System Layout

Figure 5 shows the recommended basic audio system layout if it is necessary to install the MX214 within a radio having pre- and de-emphasis circuitry as a standard. This is where post-emphasis access is not possible in the transmitter.

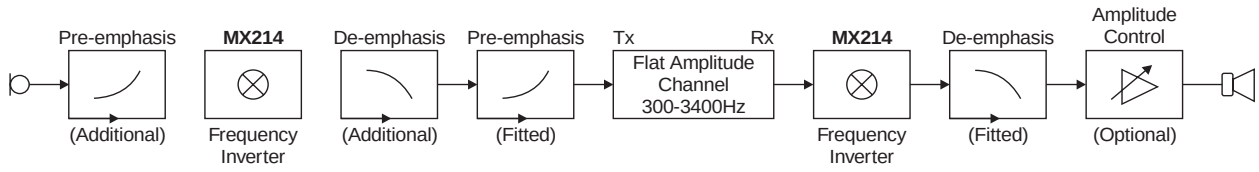


Figure 5: Recommended Basic Radio Communication Audio System Layout.

During the Transmit function the low pass and CTCSS filters are configured automatically as shown in Figure 6, with cut-off frequencies (-3dB) indicated.

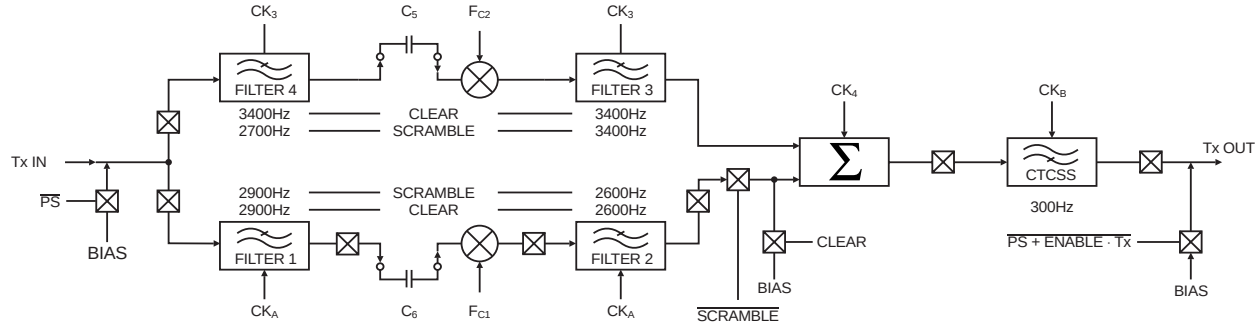


Figure 6: Basic Tx Path

During the Receive function the Low Pass and CTCSS filters are configured automatically as shown in Figure 7, with cut-off frequencies (-3dB) indicated.

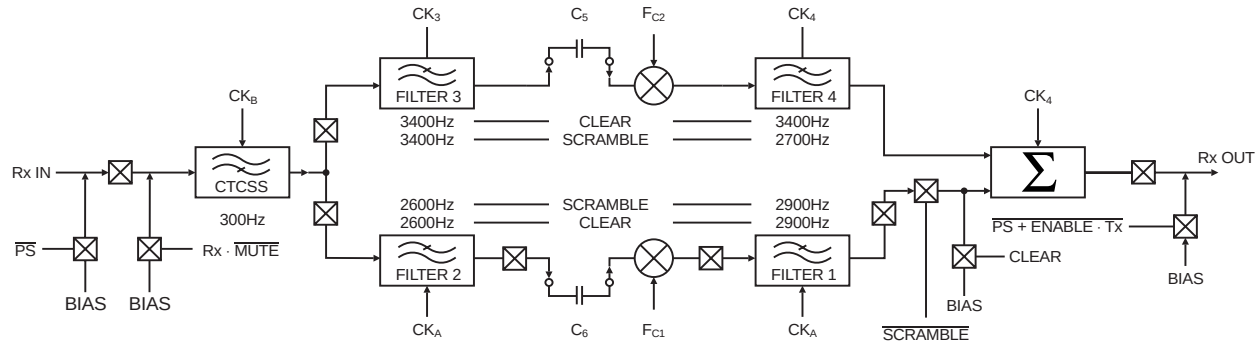


Figure 7: Basic Rx Path

6. Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
P/LH Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-30		70	°C
Storage Temperature		-40		85	°C
J Package					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-30		85	°C
Storage Temperature		-55		125	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})	4.5	5.0	5.5	V
Operating Temperature (P/LH)	-30		70	°C
Operating Temperature (J)	-30		85	°C
Xtal Frequency		1.0		MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.

V_{DD} = 5.0V @ T_{AMB} = 25°C
Audio Level 0dB ref. = 775mV_{RMS}, Xtal/Clock Frequency = 1.0MHz

	Notes	Min.	Typ.	Max.	Units
Static Values					
Voltage		4.5	5.0	5.5	V
Current					
Enabled			8		mA
Powersave			1.2		mA
Analog Input Impedances					
Tx/Rx Input (Enabled)			100		kΩ
Tx/Rx Input (Powersave)		1			MΩ
Balanced Modulator			40		kΩ
Analog Output Impedances					
Rx Output (Tx Mode)			100		kΩ
Rx Output (Rx Mode)				2	kΩ
Rx Output (Powersave)		1			MΩ
Tx Output (Tx Mode)				2	kΩ
Tx Output (Rx Mode)			100		kΩ
Tx Output (Powersave)		1			MΩ
Input LPF				1	kΩ
Digital Values					
Digital Input Impedance		100			kΩ
Dynamic Values					
Input Logic ‘1’		3.5			V
Input logic ‘0’				1.5	V
Xtal/Clock Frequency			1		MHz
Analog Input Level		-18		6	dB
Carrier Breakthrough	1		-55		dB
Baseband Breakthrough	1, 2, 3		-33		dB
Filter Clock Breakthrough	1, 2, 3		-50		dB
Output Noise	1, 4		-45		dB
Passband Characteristics					
Clear Mode	7				
Passband Gain			0		dB
Output Lower 3dB Point (Rx or Tx)			300		Hz
Output Upper 3dB Point (Rx or Tx)			3400		Hz
Scramble-Descramble	5				
Received Signal Passband Gain	6		0		dB
Received Signal Lower 3dB Point			400		Hz
Received Signal Upper 3dB Point			2700		Hz
Transmitted Signal Lower 3dB Point			300		Hz
Transmitted Signal Upper 3dB Point			3400		Hz

	Notes	Min.	Typ.	Max.	Units
CTCSS (Highpass Filter)					
-3dB Point			300		Hz
Passband gain			0		dB
Stopband Attenuation at f < 250Hz			40		dB

Operating Characteristics Notes:

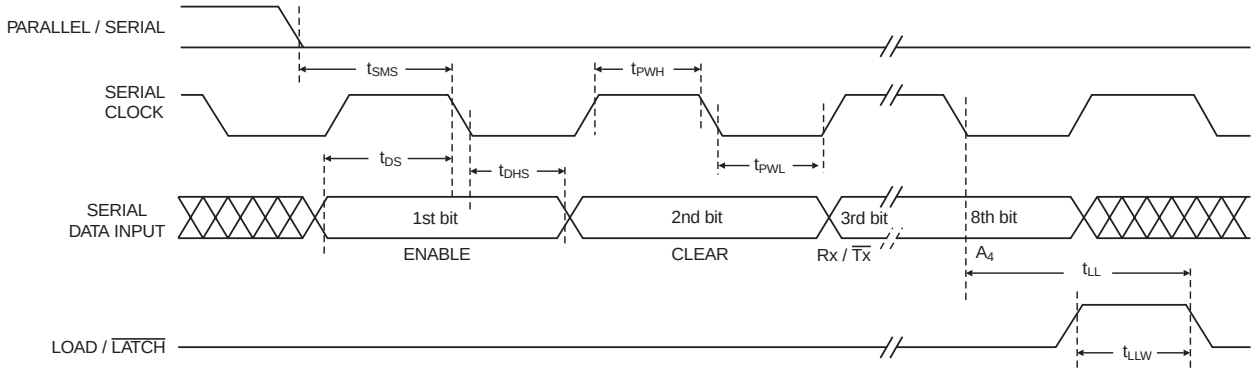
1. Measured at the output of a single device.
2. Tx Mode.
3. Rx Mode.
4. With input AC short-circuited to V_{SS}.
5. Measured at the output of a receiving device in a scrambler-descrambler system with a transmission channel having a flat amplitude response and a bandwidth of 300Hz to 3400Hz and measured relative to the input signal at the transmitting device.
6. Excluding split point ±150Hz.
7. Measured at the Rx or Tx output pin of a single source.

6.1.4 Timing

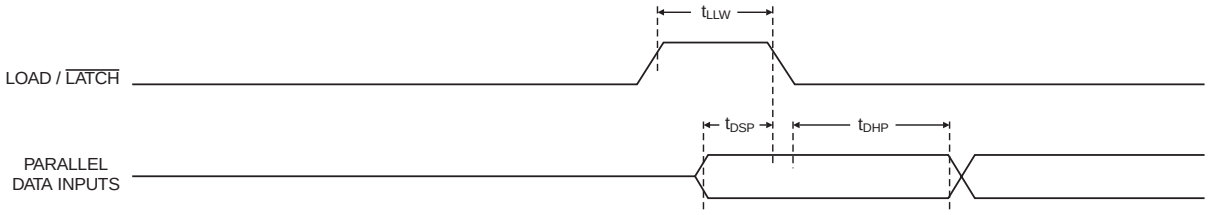
Timing		Notes	Min.	Typ.	Max.	Units
Serial Mode						
t_{SMS}	Serial Mode Enable Set-Up		250			ns
t_{PWH}	Serial Clock 'High' Pulse Width		250			ns
t_{PWL}	Serial Clock 'Low' Pulse Width		250			ns
t_{DS}	Data Set Up Time		150			ns
t_{DHS}	Data Hold Time		50			ns
t_{LL}	Load/$\overline{\text{Latch}}$ Set Up Time		250			ns
t_{LLW}	Load/$\overline{\text{Latch}}$ Pulse Width		150			ns
Parallel Mode						
t_{LLW}	Load/$\overline{\text{Latch}}$ Pulse Width		150			ns
t_{DSP}	Data Set Up Time		150			ns
t_{DHP}	Data Hold Time		20			ns

Table 5: Serial and Parallel Timing

Serial Loading



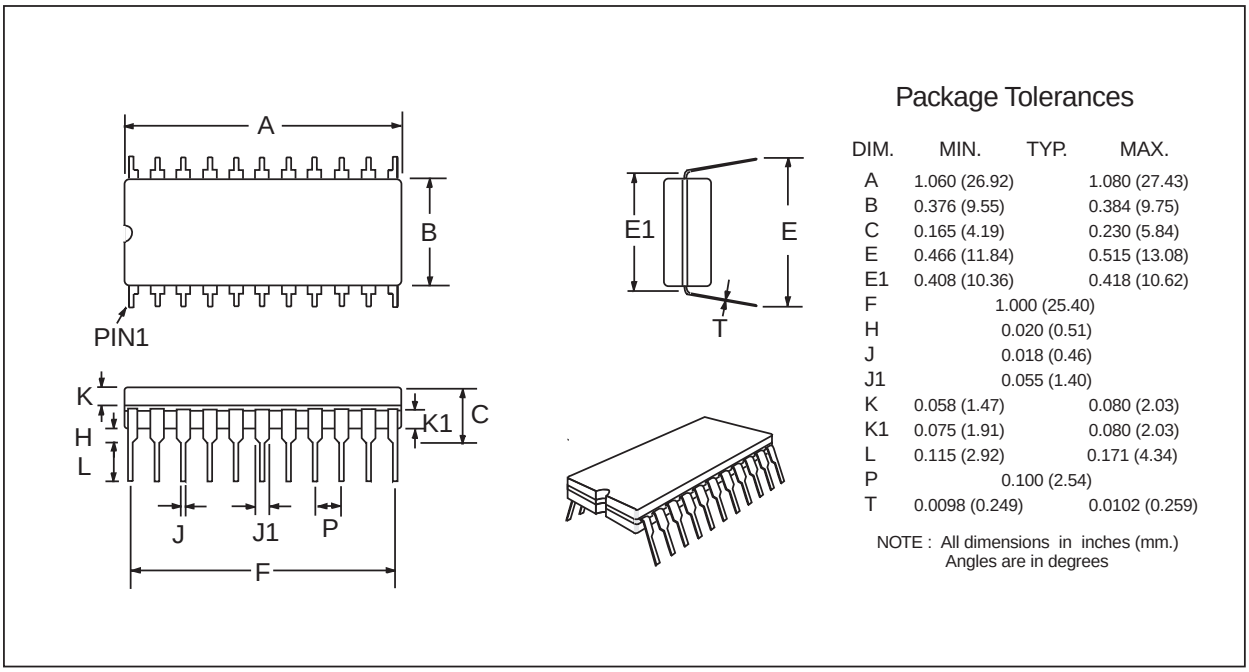
Parallel Loading



NOTE: For 'Serial Load' devices the data loading sequence is: - Enable - Clear - Rx/$\overline{\text{Tx}}$ - A_0 - A_1 - A_2 - A_3 - A_4

Figure 8: Loading Timing Diagram

6.2 Packages

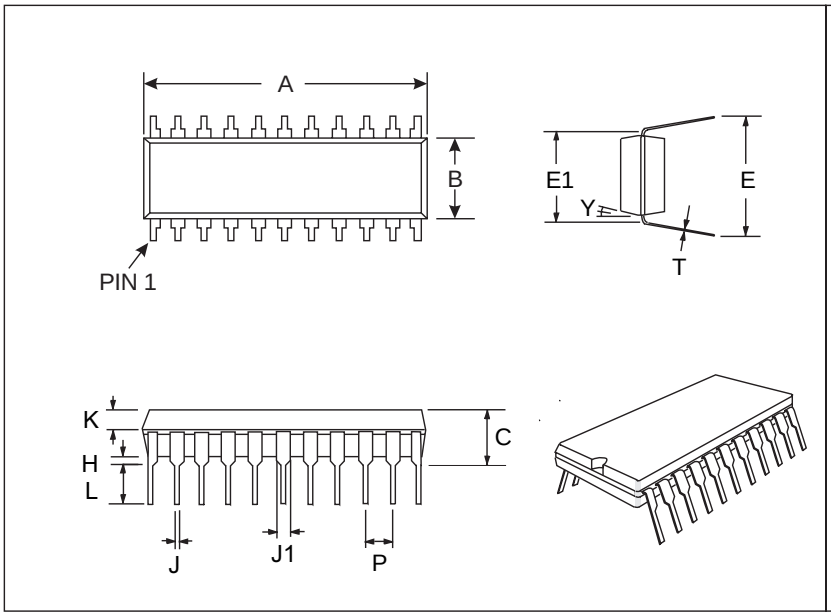


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.060 (26.92)		1.080 (27.43)
B	0.376 (9.55)		0.384 (9.75)
C	0.165 (4.19)		0.230 (5.84)
E	0.466 (11.84)		0.515 (13.08)
E1	0.408 (10.36)		0.418 (10.62)
F		1.000 (25.40)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.40)	
K	0.058 (1.47)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 22-pin CDIP Mechanical Outline: *Order as part no. MX214J or MX224J*

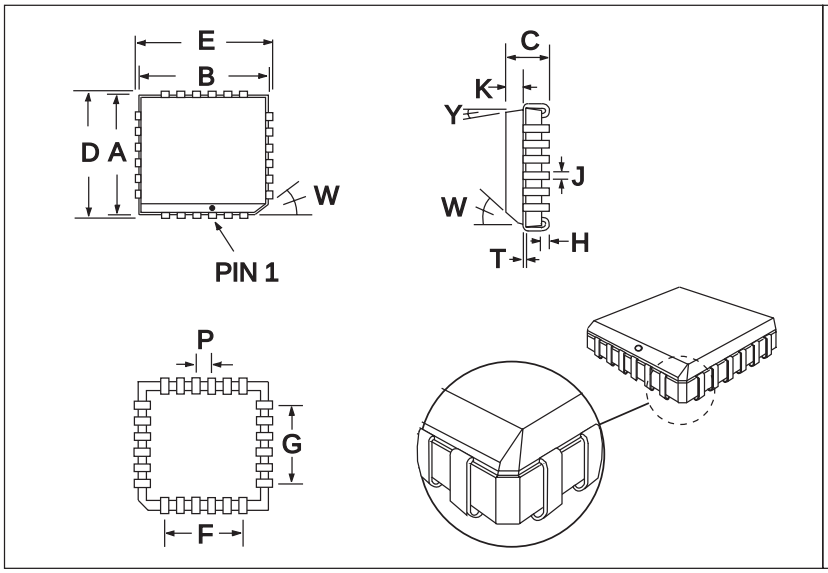


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 22-pin PDIP Mechanical Outline: *Order as part no. MX214P or MX224P*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PLCC Mechanical Outline: ***Order as part no. MX214LH or MX224LH***

