MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

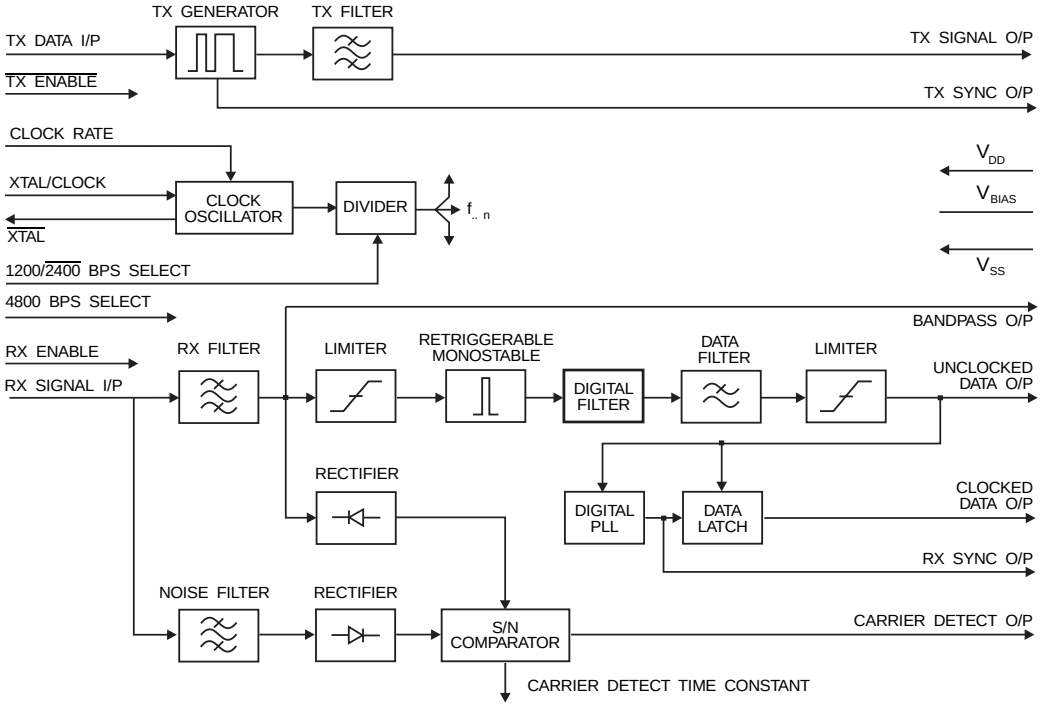
MX469 1200/2400/4800bps MSK Modem

Features

- **Selectable Data Rates 1200/2400/4800bps**
- **Full-Duplex MSK**
- **RX and TX Bandpass Filters**
- **Clock Recovery and Carrier Detect Capabilities**
- **Pin Selected Xtal/Clock Inputs 1.008MHz or 4.032MHz**

Applications

- **Radio and General Applications**
- **Data-Over-Radio**
- **PMR/Cellular Signaling**
- **Portable Data Terminals**
- **Personal/Cordless Telephone**



The MX469 is a full-duplex pin-selectable 1200/2400/4800bps Minimum Shift Key (MSK) Modem for FM radio links. The mark and space frequencies are 1200/1800, 1200/2400, and 2400/4800Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point. The use of a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) provides data-rate, transmit frequencies, and RX/TX synchronization. The transmitter and receiver operate entirely independently including individual section powersave functions.

The MX469 includes on-chip circuitry for Carrier Detect and RX Clock Recovery, both of which are made available at output pins. RX, TX, and Carrier Detect circuits contain bandpass filters to provide high quality signals in their respective paths. The carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high-noise environments.

The MX469 demonstrates high sensitivity and good bit-error-rate under adverse signal conditions.

This low-power device requires few external components and is available in the following packages: 24-pin SOIC (MX469DW), 22-pin PDIP (MX469P), and 20-pin SOIC (MX469D3).

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MXCOM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

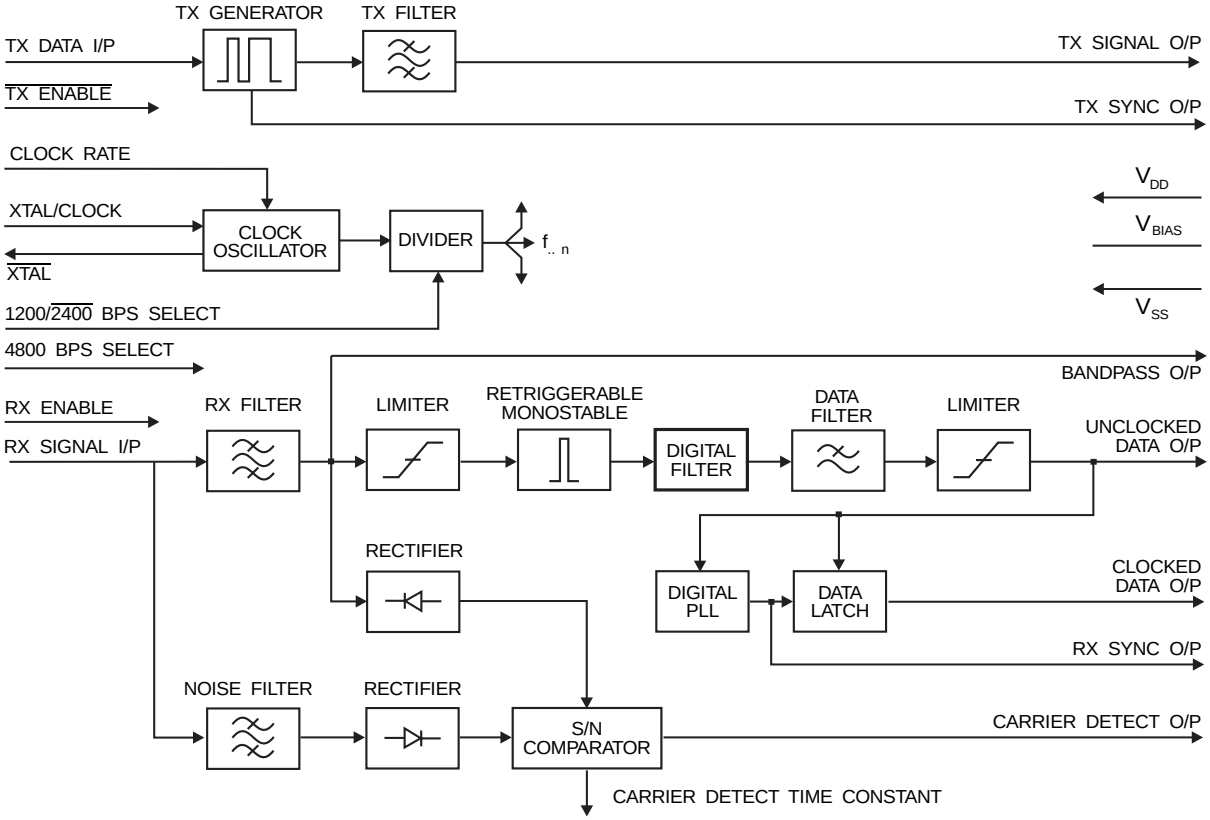


Figure 1: Block Diagram

2. Signal List

			Signal	Type	Description
P	**DW**	**D3**			
1	1	1	Xtal/Clock	input	The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin. The selection of this frequency will affect the operational Data Rate of this device. Refer to Table 3. Operation of any MX•COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, it is recommended that a current limiting device (resistor or fast-reaction fuse) be installed on the power supply (V_{DD}).
2	2	2	$\overline{\text{Xtal}}$	output	Output of the on-chip inverter.
3	3	3	TX Sync	output	A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the MSK signal (See Figure 3).
5	5	4	TX Signal	output	When the transmitter is enabled, this pin outputs the (140-step pseudo sinewave) MSK signal (See Figure 3). With the transmitter disabled, this output is set to a high-impedance state.
6	7	5	TX Data	input	Serial logic data to be transmitted is input to this pin.
7	8	6	$\overline{\text{TX Enable}}$	Input	A logic '0' will enable the transmitter (See Figure 3). A logic '1' at this input will put the transmitter into powersave while forcing "TX Sync Out" to a logic '1' and "TX Signal Out" to a high-impedance state. This pin is internally pulled to V_{DD}.
8	9	7	Bandpass	output	The output of the RX Bandpass Filter. This output impedance is typically 10kΩ and may require buffering prior to use.
9	10	8	RX Enable	Input	The control of the RX function. The control of other outputs is provided in Table 2
10	11	9	V_{BIAS}	power	The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} by a capacitor (C2). See Figure 2 and RX Enable notes. This bias voltage is maintained under all powersave conditions.
11	12	10	V_{SS}	power	Negative supply (GND).
12	13	11	Unclocked Data	output	The recovered asynchronous serial data output from the receiver.
13	14	12	Clocked Data	output	The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "RX Sync O/P". (See Figure 4 and Figure 6).
14	15	13	Carrier Detect	output	For 1200 and 2400bps operation only. When an MSK signal is being received this output is a logic '1'. The Carrier Detect signal should be ignored during 4800bps operation.
15	16	14	RX Signal	input	The MSK signal input for the receiver. This input should be coupled via a capacitor, C3.

			Signal	Type	Description
P	**DW**	**D3**			
17	18	15	RX Sync	output	A flywheel squarewave output. This clock will synchronize to incoming RX MSK data. (See Figure 4 and Figure 6).
16	19	16	1200/$\overline{2400}$ BPS Select	input	A logic ‘1’ on this pin selects the 1200bps option; tone frequencies are one cycle of 1200Hz represents a logic ‘1’, one-and-a-half cycles of 1800Hz represents a logic ‘0’. A logic ‘0’ on this pin selects the 2400bps option; tone frequencies are one-half cycle of 1200Hz represents a logic ‘1’, one cycle of 2400Hz represents a logic ‘0’. This pin has an internal 1MΩ pull-up resistor. Operational Data Rate Configurations are illustrated in Table 3
18	20	17	4800 BPS Select	input	A logic '1' on this pin combined with a logic '0' on the 1200/2400 BPS Select pin will select the 4800 option (1MΩ pulldown resistor). Tone frequencies are: one-half cycle of 2400Hz represents a logic '1', one cycle of 4800Hz represents a logic '0'. This state can only be achieved using a 4.032MHz Xtal input. Operational Data Rate Configurations are illustrated in Table 3
19	21	18	Clock Rate	input	A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic ‘1’ = 4.032MHz, logic ‘0’ = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
20	23	19	Carrier Detect Time Constant	output	Part of the carrier detect integration function. The value of C4 connected to this pin will affect the carrier detect response time and therefore the noise performance (See Figure 2, Note 3).
22	24	20	V_{DD}	power	Positive supply. A single 5-volt supply is required.
4, 21	4, 6, 17, 22		N/C		No Internal Connection.

Table 1: Signal List

RX Enable	=	RX Function	Clock Data Output	Carrier Detect	Rx Sync Out
1	=	Enabled	Enable	Enabled	Enabled
0	=	Powersave	0	0	1 or 0

Table 2: RX Enable Control Functions

XTAL/CLOCK Frequency	1.008MHz		4.032MHz		
Clock Rate pin	0	0	1	1	1
1200/2400 Select Pin	1	0	1	0	0
4800 Select Pin	0	0	0	0	1
Data Rate (bps)	1200	2400	1200	2400	4800

Table 3: Operational Data Rate Configuration

3. External Components

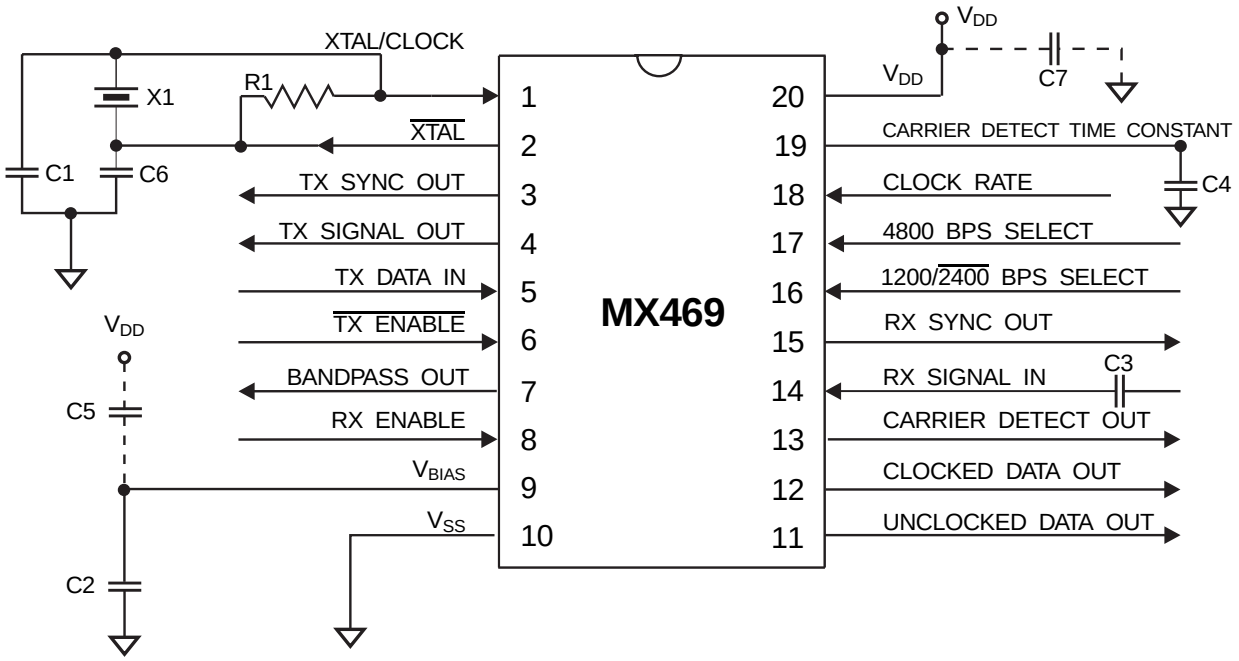


Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1		1.0MΩ	±10%
C1		33pF	±5%
C2		1.0µF	±20%
C3		0.1µF	±20%
C4	Note 1	0.1µF	±10%
C5	Note 2	1.0µF	±25%
C6	Note 3	33pF	±5%
C7	Note 2	1.0µF	±20%
X1	Note 4	1.008MHz or 4.032MHz	See 'Clock-Rate' Pin

Table 4: Recommended External Components

Notes:

1. The value of C4 determines the Carrier Detect time constant. A long time constant results in improved noise immunity but increased response time. C4 may be varied to trade-off response time for noise immunity.
2. Decoupling circuits depend upon whether the input signal is referenced to V_{BIAS} or V_{SS}. Use C5 when the input signal is referenced to V_{BIAS}. Use C7 when the input signal is referenced to V_{SS}. It is not necessary to use both C5 and C7.
3. C6 reduces Xtal voltage overshoot. Reference the MX-COM Xtal Application Note.
4. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

4.1 Timing

4.1.1 1200bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}			416		µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0		800	µs
Data Set-Up Time	t_{DSET}	1	2.0			µs
Data Hold Time	t_{DH}		2.0			µs
TX Delay to O/P Time	t_{TXD}			1.2		µs
TX Data Rate Period	t_{TDR}			833		µs
RX Data Rate Period	t_{RDR}		800		865	µs
Undetermined State					2.0	µs
Internal RX Delay	t_{ID}			1.5		ms

Notes:

1. Consider the Xtal/clock tolerance.
2. All TX timings are related to the TX Sync Output.

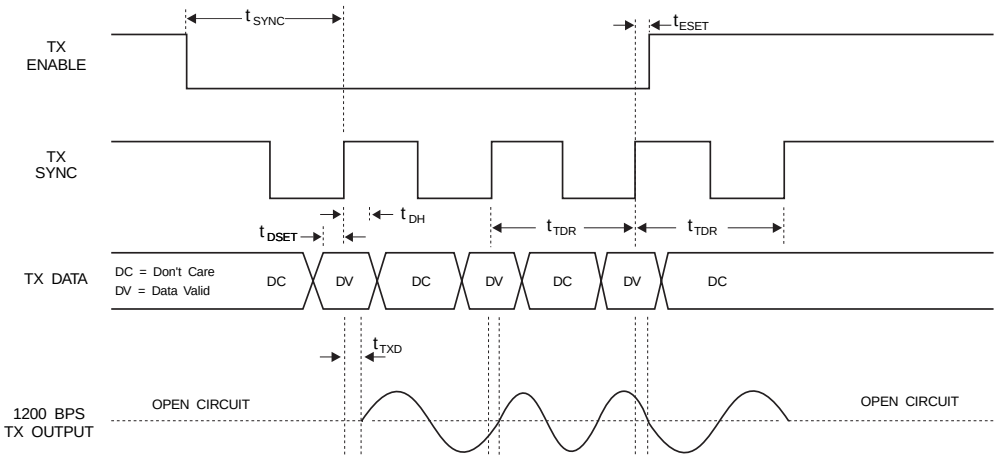


Figure 3: Transmitter Timing: 1200bps

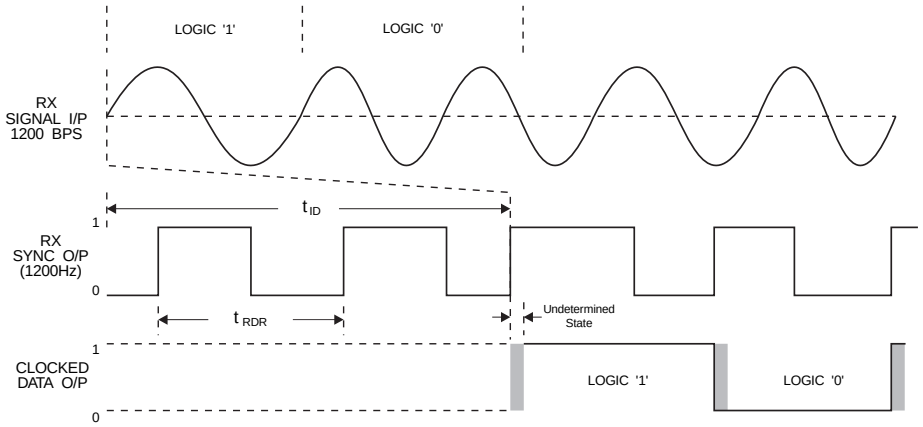


Figure 4: Receiver Timing Diagram: 1200bps

4.1.2 2400bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}			208		µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0		400	µs
Data Set-Up Time	t_{DSET}	1	2.0			µs
Data Hold Time	t_{DH}		2.0			µs
TX Delay to O/P Time	t_{TxD}			1.2		µs
TX Data Rate Period	t_{TDR}			416		µs
RX Data Rate Period	t_{RDR}		400		433	µs
Undetermined State					2.0	µs
Internal RX Delay	t_{ID}			1.5		ms

Notes:

1. Consider the Xtal/Clock tolerance.
2. All TX timings are related to the TX Sync Output.

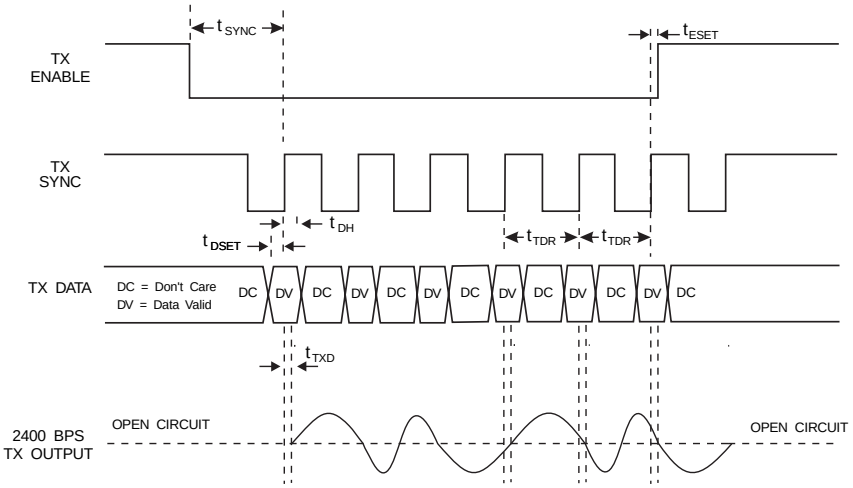


Figure 5: Transmitter Timing: 2400bps

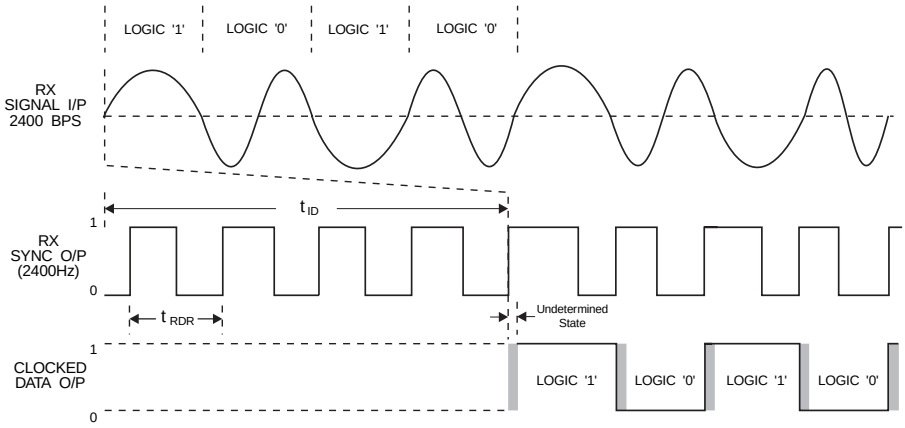


Figure 6: Receiver Timing: 2400bps

4.1.3 4800bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}			104		µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0		200	µs
Data Set-Up Time	t_{DSET}	1	2.0			µs
Data Hold Time	t_{DH}		2.0			µs
TX Delay to O/P Time	t_{TxD}			1.2		µs
TX Data Rate Period	t_{TDR}			208		µs
RX Data Rate Period	t_{RDR}		200		216	µs
Undetermined State					2.0	µs
Internal RX Delay	t_{ID}			1.0		ms

Notes:

1. Consider the Xtal/Clock tolerance.
2. All TX timings are related to the TX Sync Output.

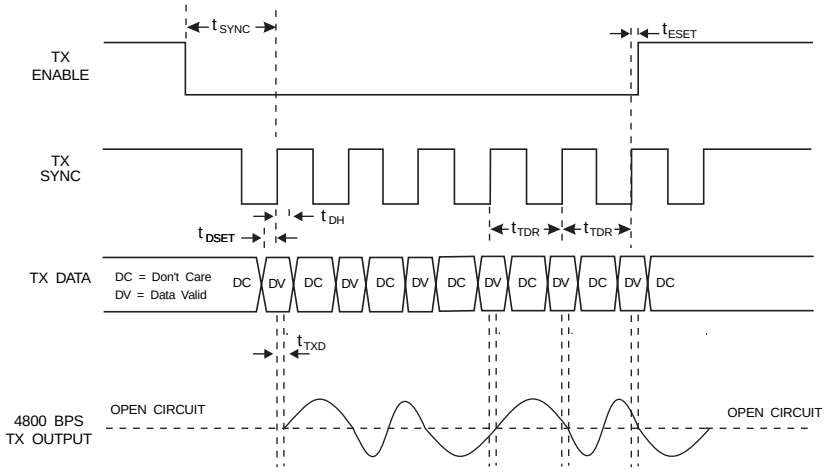


Figure 7: Transmitter Timing: 4800bps

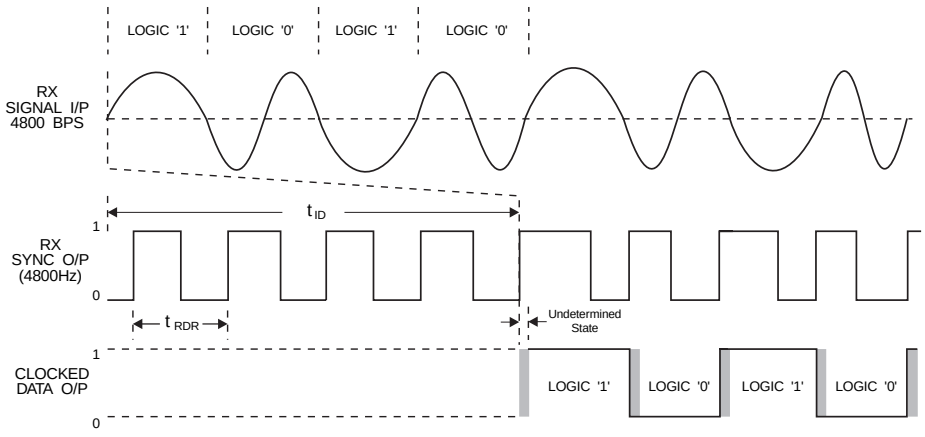


Figure 8: Receiver Timing: 4800bps

5. Application

5.1 Synchronous Modem Design Considerations

The MX469 is an easily applied data pump, which can be used with many protocols. Because it is an MSK, or minimum shift keying, modem, it achieves a more noise resistant, higher data rate in a narrower bandwidth than other FSK (frequency shift keying) modems. This characteristic is especially important for wireless applications because it fundamentally determines the bandwidth of RF transmissions, which are strictly limited and controlled by regulatory agencies. Using MSK signaling, the MX469 data modem can achieve a 2400bps data rate within the typical 300-3000 Hz voice band of many common radios.

In order to achieve this advantage, an MSK modem must precisely control the bit rate and timing of the modulated Tx output signal bits. This control is asserted by the MSK modem with a data clock signal, which is output, by the modem to pace the Tx data source (e.g. a microcontroller). The data clock signal, in effect, indicates when the Tx data source should provide the next Tx data bit to the modem. See Figure 9. Because this type of interface involves the use of a modem generated bit clock signal to control the timing of when new Tx data bits must be supplied from the data source, the interface is called synchronous.

Another characteristic of a synchronous modem is that, to receive data, it must first learn the data bit timing of the Rx signal stream before it can accurately demodulate Rx data bits. Accordingly, a synchronous modem undergoes a period of training or synchronization when it first begins to receive a stream of MSK modulated signal. During this initial receive phase, the received signal is evaluated over several bit times as the modem 'locks on' and achieves proper receive synchronization. The training sequence, called a preamble, is a specific data pattern which must be added to the 'front' of a transmit data stream with the start of each new transmission. A specific preamble data pattern (e.g. 16 bits of alternating 0,1,0,1… for the MX469) is used to optimize the training accuracy while minimizing the number of preamble bits required.

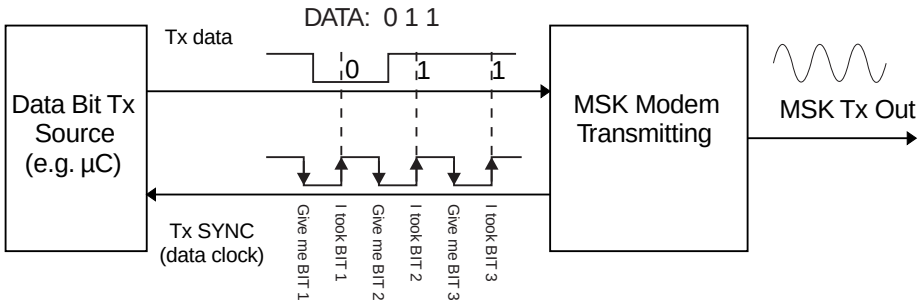


Figure 9: Synchronous Transmit Operation

Non-synchronous or asynchronous interfaces are commonly found in wired applications which do not have the bandwidth efficiency requirements of wireless systems. A well known example is the serial port of a personal computer which can transmit a 1200 bps (or faster) data signal over a single Tx signal without using an additional data clock signal to control the precise rate and timing of data bits being transmitted to a typical telephone line data modem. Popular modem standards such as Bell 202 and v.23 use FSK signaling to pass such asynchronous serial port data signals over telephone systems.

Another aspect of asynchronous interfaces and modems is that they can carry data streams which are not at the exact, nominal data rate. For example, a 1200 bps FSK modem will typically operate properly when supplied with transmit data streams of 1201 bps or 1199 bps.

Because of the differences in synchronous and asynchronous interfaces, they cannot successfully operate if directly connected. In other words, a personal computer's RS232 serial port cannot directly interface to an MSK modem. This is because:

- The asynchronous interface may provide data bits too fast or too slow compared to the precise rate required for MSK signaling (a bit rate, or pacing, incompatibility).
- The timing of each specific data bit presented by an asynchronous interface will not be aligned with the precise bit timing required for MSK signaling (a bit timing incompatibility).

Synchronous and asynchronous interface can be successfully interfaced for applications requiring the advantages of both. This typically involves the use of data buffering and retiming circuits to resolve the timing and pacing issues.

5.2 Bit Error Rate

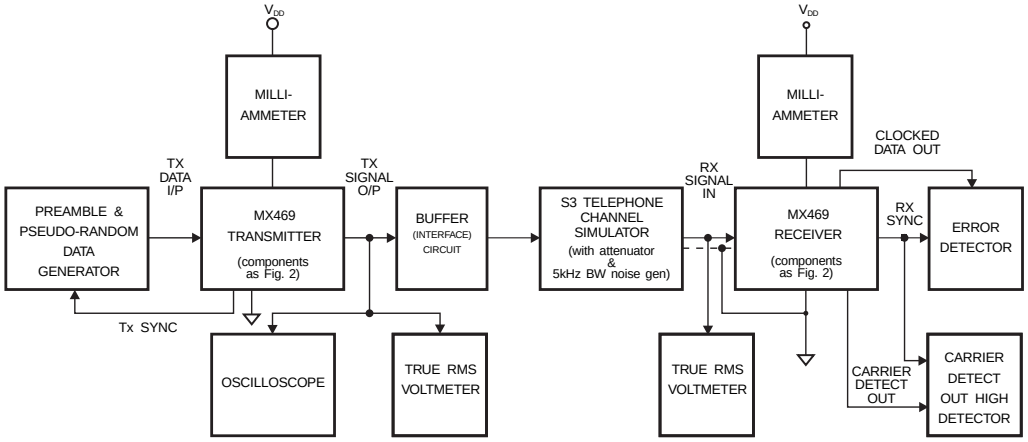


Figure 10: MX469 Test Set-Up

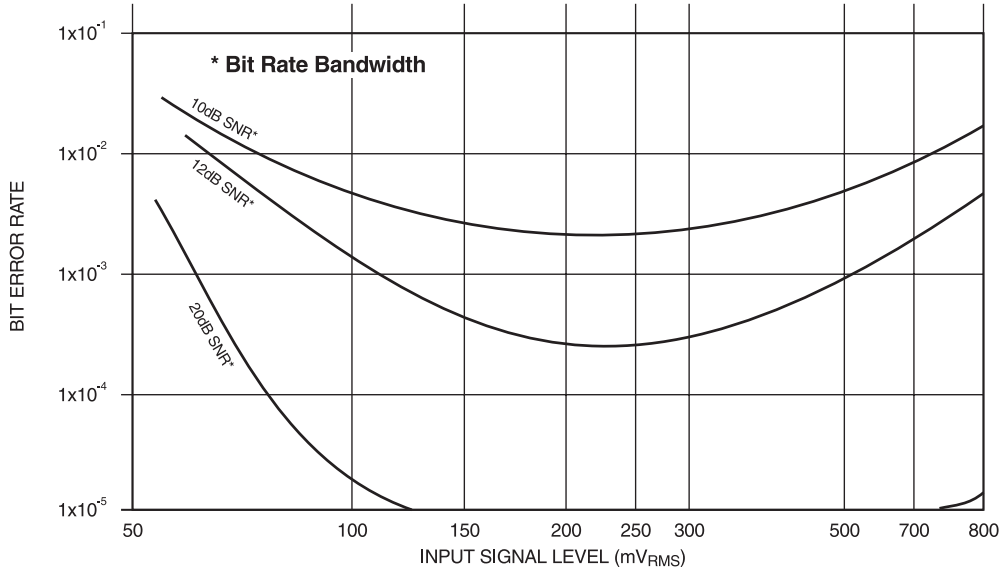


Figure 11: Typical Variation of Bit Error Rate with Input Level

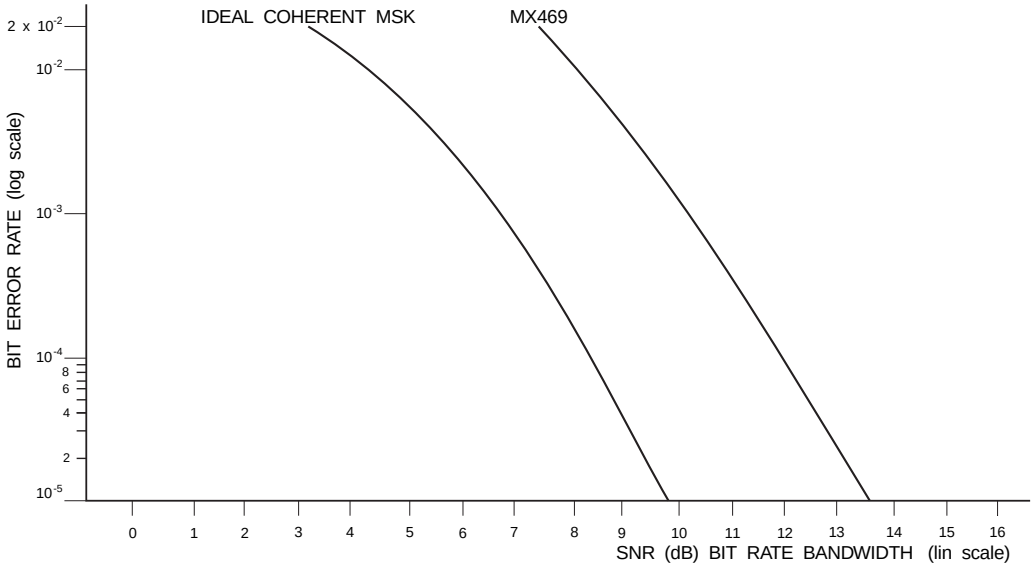


Figure 12: RX Bit-Error-Rate vs. Signal-to-Noise Ratio

6. Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
DW / D3 / P Packages					
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency		1.008		4.032	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.

V_{DD} = 5.0V @ T_{AMB} = 25°C
Audio Level 0dB ref. = 300mV_{RMS}, Xtal/Clock Frequency = 4.032MHz
Signal-to-Noise Ratio measured in the Bit-Rate Bandwidth
1200bps BRB = 1200Hz
2400bps BRB = 2400Hz
4800bps BRB = 4800Hz

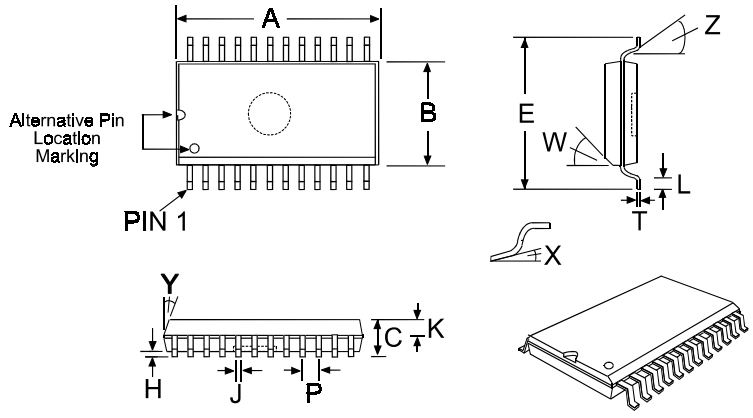
	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Current					
RX Enabled, TX Disabled			3.6		mA
RX and TX Enabled			4.5		mA
RX and TX Disabled			650		µA
Logic ‘1‘ Level	1	4.0			V
Logic ‘0’ Level	1			1.0	V
Digital Output Impedance			4.0		kΩ
Analog and Digital Input Impedance		100			kΩ
TX Output Impedance			0.6	1.0	kΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0			MΩ
R_{OUT}			10.0		kΩ
Inverter DC Voltage Gain			10.0		V/V
Gain Bandwidth Product			10.0		MHz
Dynamic Values					
Receiver					
Signal Input Dynamic Range					
SNR = 50dB	3, 4	100	230	1000	mV_{RMS}
Bit Error Rate					
SNR = 12dB	4		7.0		10^{-4}
1200bps			2.5		10^{-4}
2400bps			1.5		10^{-3}
4800bps			1.5		10^{-3}
SNR = 20dB	4				
1200/2400/4800bps			1.0		10^{-8}
Receiver Synchronization SNR =12dB	7				
Probability of Bit 8 Being Correct			99		%
Probability of Bit 16 Being Correct			99.5		%
Carrier Detect	5, 10				
Sensitivity	7, 8			150	mV_{RMS}
Probability of C.D. Being High					
After Bit 8 (1200bps) SNR = 12dB	5, 9		98		%
After Bit 16 SNR = 12dB	5, 9		99.5		%
0dB Noise No Signal	9		5		%

	Notes	Min.	Typ.	Max.	Units
Transmitter Output					
TX Output Level			775		mV_{RMS}
Output Level Variation					
1200/1800Hz		0		±1.0	dB
1200/2400Hz		0		±1.0	dB
2400/4800Hz		0		±1.0	dB
Output Distortion			3.0	5.0	%
3rd Harmonic Distortion			2.0	3.0	%
Logic '1' Carrier Frequency					
1200bps	6		1200		Hz
2400bps	6		1200		Hz
4800bps	6		2400		Hz
Logic '0' Carrier Frequency					
1200bps	6		1800		Hz
2400bps	6		2400		Hz
4800bps	6		4800		Hz
Isochronous Distortion					
1200Hz - 1800Hz/1200Hz - 2400Hz			25.0	40.0	µs
1800Hz - 1200Hz/2400Hz - 1200Hz			20.0	40.0	µs
2400Hz - 4800Hz/4800Hz - 2400Hz			10.0	20.0	µs

Operating Characteristics Notes:

1. With reference to V_{DD} = 5.0 volts.
2. Xtal frequency (ref. Clock Rate pin), type and tolerance depends upon system requirements.
3. See Figure 4 (variation of BER with Input Signal Level).
4. SNR = Signal-to-Noise in the Bit-Rate Bandwidth.
5. See Figure 2.
6. Dependent upon Xtal tolerance.
7. 10101010101 ...01 pattern.
8. Measured with a 150mV_{RMS} input signal (no noise).
9. Reference (0dB) level for C.D. probability measurements is 230mV_{RMS}.
10. For 1200bps and 2400bps operation only: when operating at 4800bps the carrier detect output should be ignored.

6.1.4 Packages

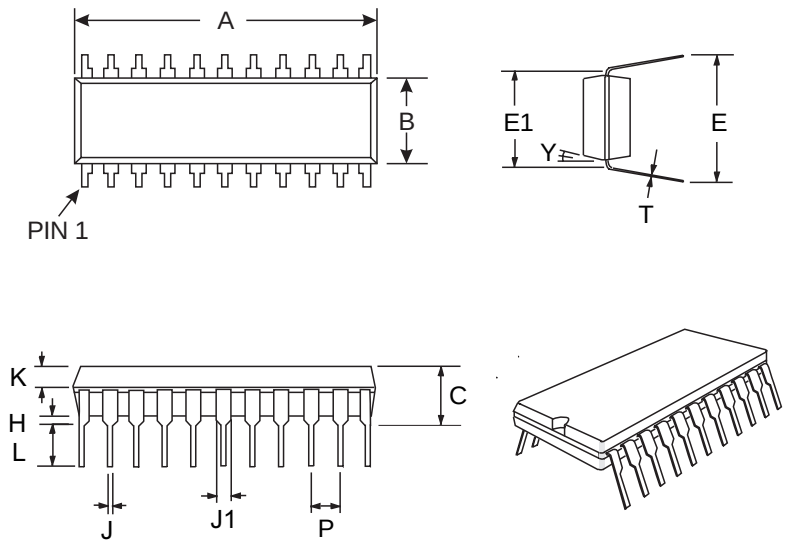


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions In Inches (mm.)
Angles are in degrees

Figure 13: 24-pin SOIC Mechanical Outline: Order as part no. MX469DW

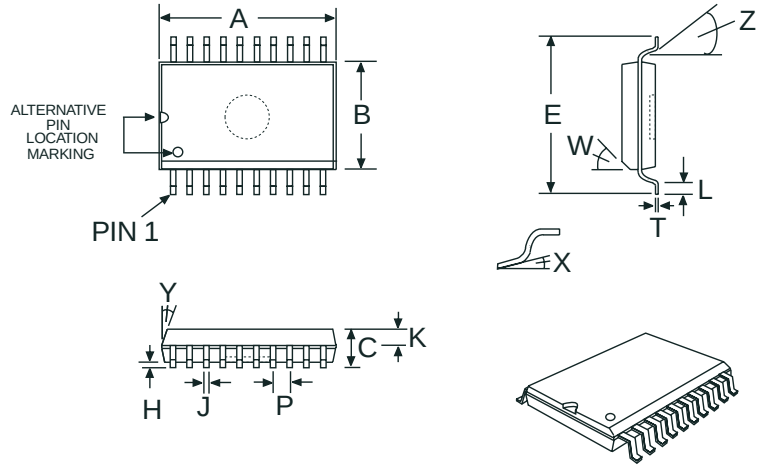


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 22-pin PDIP Mechanical Outline: *Order as part no. MX469P*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.495 (12.57)		0.510 (12.95)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 20-pin SOIC Mechanical Outline: *Order as part no. MX469D3*

