MX•COM, INC.
COMMUNICATION ICs

CMX673

DATA BULLETIN

Call Progress Tone Detector

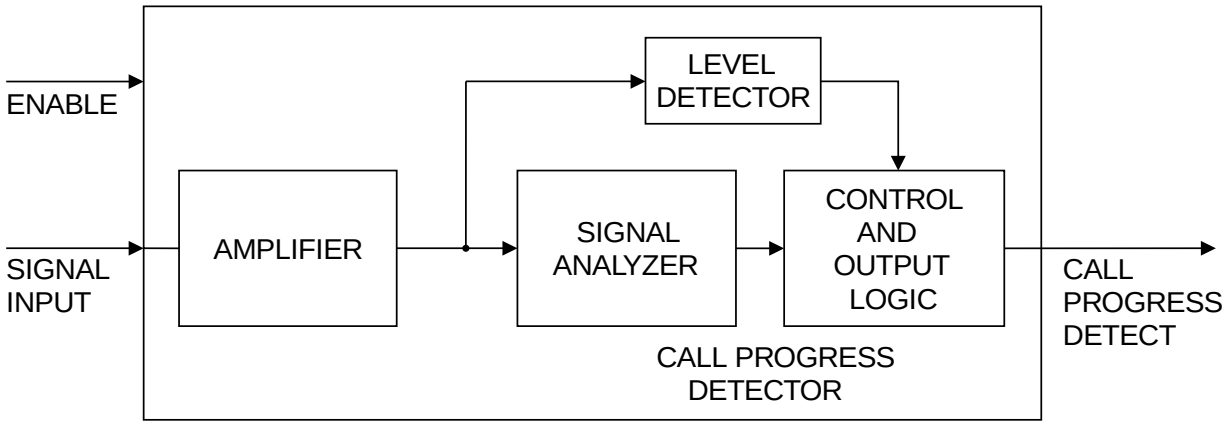
PRELIMINARY INFORMATION

Features

- **Worldwide Tone Compatibility**
- **Fast Response**
  Stutter Dial Tone
  Single and Dual Tones
- **Industry Compatible Pin Out**
- **Wide Dynamic Signal Range**
- **Low Power: 0.5mA at 3.0V**
- **3.0V to 5.0V Operation**
- **3.58MHz Xtal/Clock Oscillator**

Applications

- **Worldwide Payphone Systems**
- **Featurephone active feature confirmation**
- **Telephone Redialing Systems**
- **Dialing Modems**
- **Banking and Billing Systems**
- **Telecom Test Equipment**
- **Telecom Security Systems**



The CMX673 is a low voltage multi-purpose Call Progress Tone detector for use in Public Switched Telephone Network System (PSTN) applications. Call progress detection allows equipment that dials into the PSTN to monitor the progress of the resulting call. Various states such as Ringing, Busy, Not available, and Answer can be determined. Using digital signal processing techniques the CMX673 accurately analyzes tones in the 315Hz to 650Hz frequency band and distinguishes valid call progress tone signals from line noise or voice. This contrasts with other call progress detection devices that are based on simple filtering techniques. When combined with cadence measurement of the CMX673 output, the rapid detect response time of the CMX673 allows it to support a wide range of call progress functions including 'stutter dial tone' detection used in voice messaging systems.

A single, low cost 3.58MHz crystal ensures accurate and repeatable performance. With supply requirements between 2.7V and 5.5V the CMX673 is easily integrated into a wide range of telecom applications.

The convenient CMX673 pin out allows it to be readily incorporated into existing product designs to quickly achieve its benefits. Small geometry CMOS design techniques provide a complete call progress detector that analyzes both frequency and amplitude in a small single package. Available packages are: 8-pin PDIP (CMX673P1), 16-pin SOIC (CMX673D4), and 20-pin TSSOP (CMX673E3).

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1 Block Diagram

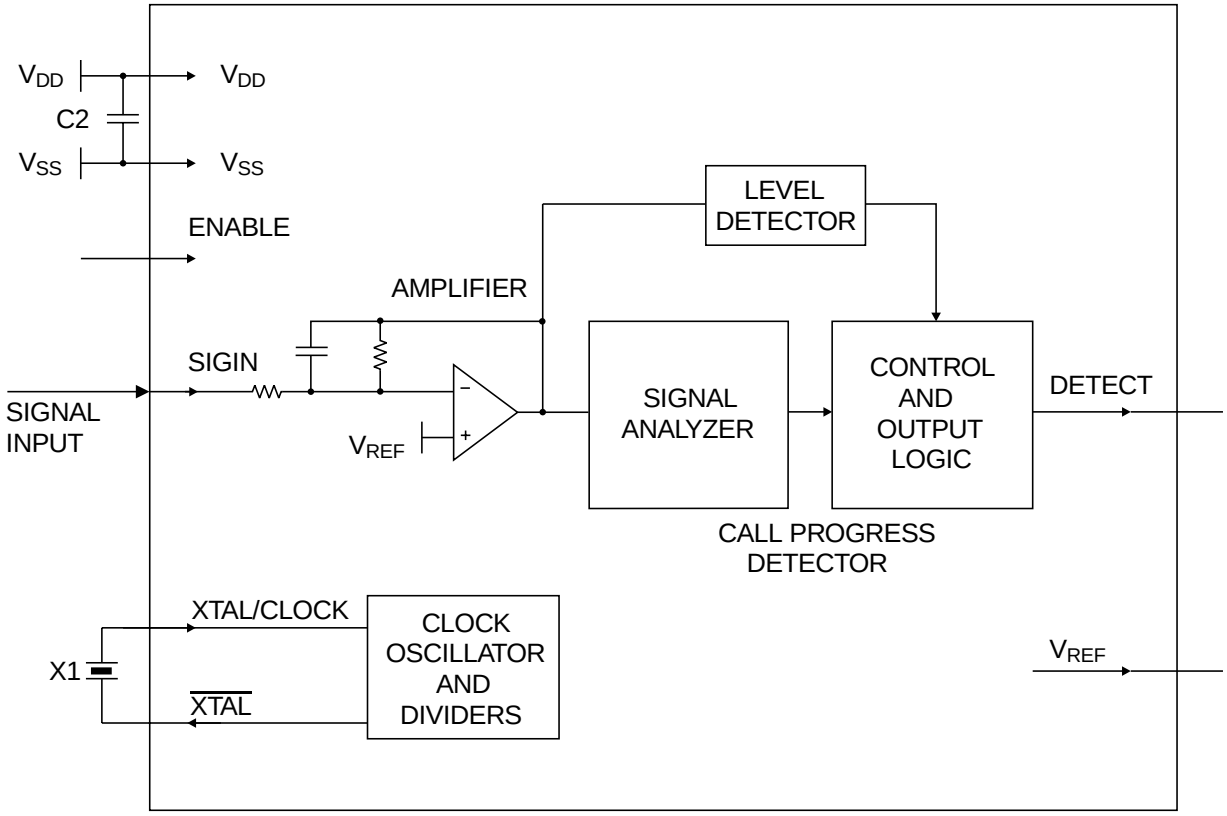


Figure 1: Block Diagram

2 Signal List

Packages			Signal		Description
E3	**D4**	**P1**	**Name**	**Type**	
3	2	1	XTAL/CLOCK	input	The input to the on-chip oscillator and external clock input. Components are on chip.
5	4	2	$\overline{\text{XTAL}}$	output	The inverted output of the on-chip oscillator.
7	5	3	ENABLE	input	A logic '1' applied to this input enables the DETECT output. A logic '0' will reset DETECT output to a logic '0'.
8	7	4	DETECT	output	When a call progress signal is detected, this output goes to a logic '1'.
13	10	5	SIGIN	input	Signal input. Signals to this pin should be AC coupled. The DC bias of this pin is set internally.
15	12	6	V_{SS}	Power	The negative supply rail (ground).
17	14	7	V_{REF}	output	Internally generated reference voltage, held at $V_{DD}/2$
18	15	8	V_{DD}	Power	The positive supply rail. This pin should be bypassed to V_{SS} by a capacitor.
1, 2 4, 6 9, 10 11, 12 14, 16 19, 20	1, 3 6, 8 9, 11 13, 16		NC		Internal Connection. Do not make any connection to these pins.

Table 1: Signal List

3 External Components

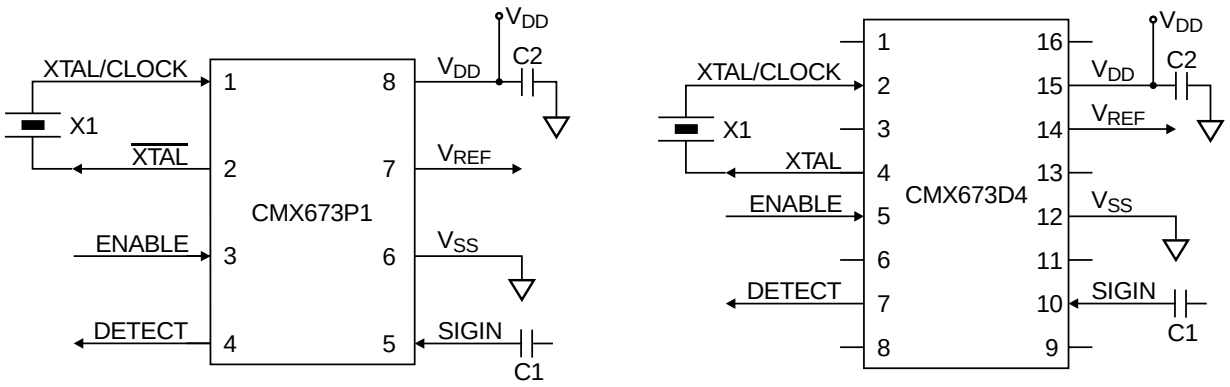


Figure 2: Recommended External Components

C1	Note 1	0.1µF	± 20%
C2		1µF	± 20%
X1	Note 2, 3	3.579545MHz	

Table 2: Recommended External Components

Note:

1. C1 is not required if the input is referenced to V_{REF}.
2. Reference Section 6.1
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4 General Description

4.1 Overall Function Description

The CMX673 Call Progress Tone Detector uses different tone detection methods from those commonly found with other products.

Many traditional devices use a bandpass filter followed by an energy detector. The filter is usually designed to pass input signals with a frequency between about 300Hz and 700Hz, and the amplitudes of signals in this range are then checked against a level threshold. Any signal of acceptable level in this frequency band is classed as a Call Progress tone, including signals due to speech and noise. False outputs caused by speech are a common feature with these products, and background noise may lead to a stuck “detect” output.

The CMX673, by contrast, uses a stochastic signal processing technique based on analysis in both the frequency and time domains, with signal amplitude forming part of the decision process. This analysis includes checks on whether the signal has a “profile” which matches international standards for Call Progress tone, or a profile more likely to match that of speech, noise or no signal.

4.2 Glossary

The following Glossary, and the Decode Truth Table in Section 4.4 provide an explanation of the decoding functions and features offered by the CMX673.

Call Progress Tones: The single and dual frequency tones in the range 350Hz to 620Hz specified widely for call progress signaling.

Call Progress Band: The nominal range 315Hz to 650Hz within which the CMX673 will detect Call Progress tones. The detection algorithm requires that the tones have the characteristics typical of Call Progress Tones.

No Signal: No Signal is classified by the absence of an input signal, a signal below 250Hz, or a signal between 750Hz and 10kHz
Note: Signals above 10kHz should be at a level below -38dBm to avoid aliasing.

Nominal: Subject to dynamic tolerances within the signal analysis process. Absolute values are not material or adverse to performance.

4.3 Block Diagram Description

Amplifier: The input signal is amplified by a self-biased inverting amplifier. The DC bias of this input is internally set at $V_{DD}/2$.

Signal Analyzer: The frequency range, quality and consistency of the input signal is analyzed by this functional block. To be classified as a call progress signal the input signal frequencies should lie between 315Hz and 650Hz. The signal to noise ratio must be 16dB or greater. The signal must be consistent over a period of about 80ms. These decode criteria are continuously monitored and the assessment is updated every 6ms; reference Figure 4.

Control Logic: This block categorizes the nature of the signal into two decoded output states and controls the output pin. See the Decode Output Truth Table in Section 4.4.

Level Detector: The level detector operates by measuring the level of the amplified input signal and comparing it with a preset threshold. The level detector output goes to the Control and Output Logic block. The data output is gated with the level detector's output. The data output is valid only if the level detector output is true.

Xtal/Clock Oscillator: If the on-chip Xtal oscillator is to be used, then external component X1 is required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin and the $\overline{\text{XTAL}}$ pin should be left unconnected.

4.4 Decode Output Truth Table

"DETECT"	CONDITIONS
0	No Signal
1	Call Progress Band: Will detect 350+440, 400+450, 440+480 400, 425,440, 450, 480+620, 600 and 620Hz tones

Note: DETECT responds to the whole range of call progress tones from 315Hz to 650Hz.

Table 3: Decode Output Truth Table

5 Application Notes

5.1 General

On power-up, it will take 80ms to initialize the internal state, this delay should be accounted for before the DETECT output is valid.

5.1.1 Typical Telephone Line Circuit

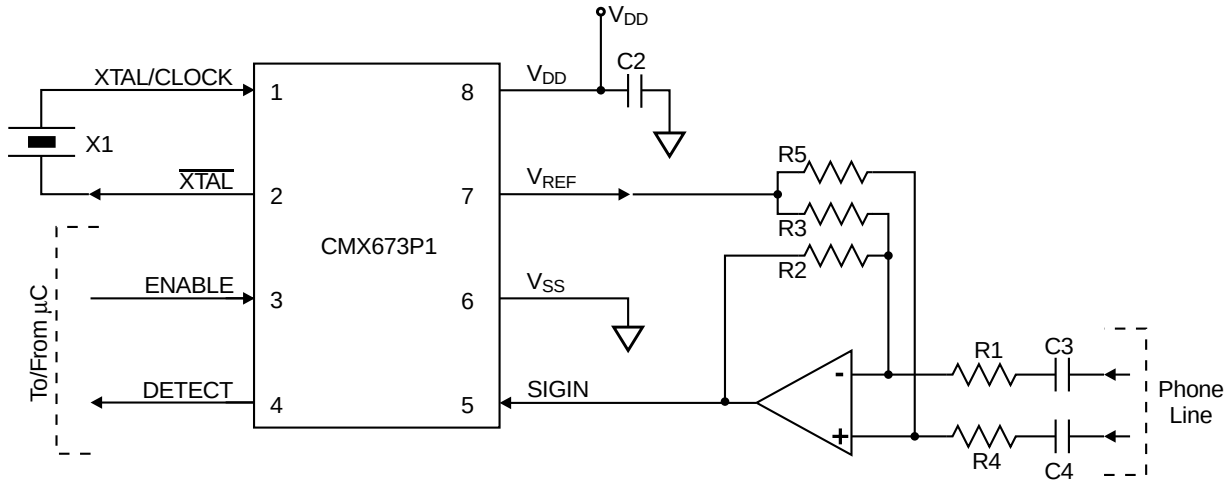


Figure 3: A typical Telephone Line Circuit Application

R1	Note 1	470kΩ	±1%
R2	Note 1	470kΩ	±1%
R3	Note 1	240kΩ	±1%
R4	Note 1	470kΩ	±1%

R5	Note 1	160kΩ	±1%
C3	Note 1	0.01µF 250V	±2%
C4	Note 1	0.01µF 250V	±2%

Note:

1. Resistor and Capacitor tolerance levels are as indicated, unless otherwise stated.
2. A low offset opamp is needed.

An Alternative set of component values can be used:

R1	Note 1	499kΩ	±1%
R2	Note 1	499kΩ	±1%
R3	Note 1	54.9kΩ	±1%
R4	Note 1	499kΩ	±1%

R5	Note 1	49.9kΩ	±1%
C3	Note 1, 2	0.001µF (300V)	±2%
C4	Note 1, 2	0.001µF (300V)	±2%

Note:

1. Resistor and Capacitor tolerance levels are as indicated, unless otherwise stated.
2. A higher value of C3 and C4 will reduce the level sensitivity tolerance at around -38dBm.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
P1 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13.0	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
D4 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13.0	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
E3 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Xtal Frequency		3.57	3.59	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, S/N = 16dB, Noise Bandwidth = 5kHz,
V_{DD} = 3.0V to 5.0V, T_{AMB} = -40°C to 85°C, 0dB = 775mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (ENABLE = '1')					
(V_{DD} = 5.0V)	1		1.0	1.5	mA
(V_{DD} = 3.0V)	1		0.5	1.0	mA
AC Parameters					
SIGIN pin					
Input Impedance	2		0.1		MΩ
Minimum Input Signal Level			-38.0		dB
Input Signal Dynamic Range		40.0			dB
Signal to Noise Ratio		16.0			dB
Xtal/Clock Input					
'High' Pulse Width	3	100			ns
'Low' Pulse Width	3	100			ns
Gain (input = 1mV_{RMS} at 100Hz)		20.0			dB
Level Detector					
Must Detect Signal Level	4	-38.0			dB
Must Not Detect Signal Level	4			-50.0	dB
Call Progress Band	7				
Must Detect Range		315		650	Hz
Must Not Detect Range		750		250	Hz
Logic Interface					
Input Logic "1" Level	5	80%			V_{DD}
Input logic "0" level	5			20%	V_{DD}
Input leakage current (V_{IN} = 0 to V_{DD})	5	-5.0		5.0	µA
Input Capacitance	5		10.0		pF
Output logic "1" level (I_{OH} = 120µA)	6	90%			V_{DD}
Output logic "0" level (I_{OL} = 360µA)	6			10%	V_{DD}

Notes:

1. Not including any current drawn from the detector pins by external circuitry.
2. Small signal impedance over the frequency range 100Hz to 2000Hz and at V_{DD} = 5.0V.
3. Timing for an external input to the XTAL/CLOCK pin.
4. Input signal level at V_{DD} = 5.0V, scale signal for different V_{DD}.
5. ENABLE pin.
6. DETECT pin.
7. Nominal values that are subject to dynamic tolerances within the signal analysis process, as a result of using stochastic signal processing techniques.

6.1.4 Timing

For the following conditions unless otherwise specified:
Xtal Frequency = 3.579545MHz, V_{DD} = 3.0V to 5.0V, T_{AMB} = -40°C to +85°C, S/N = 20dB.

Signal Timings		Notes	Min.	Typ.	Max.	Units
t_I	Burst Length Ignored				40.0	ms
t_L	Burst Length Detected		80.0			ms
t_{GI}	Call Progress Tone Gap Length Ignored	1			20.0	ms
t_{GD}	Call Progress Tone Gap Length Detected	1	40.0			ms
t_{RP}	Call Progress Tone Response Time	2			80.0	ms
t_{DRP}	Call Progress Tone De-Response Time	2			80.0	ms

Notes:
1. Only applies to bursts of the same frequency.
2. Measured with 350 + 440Hz tone pair.

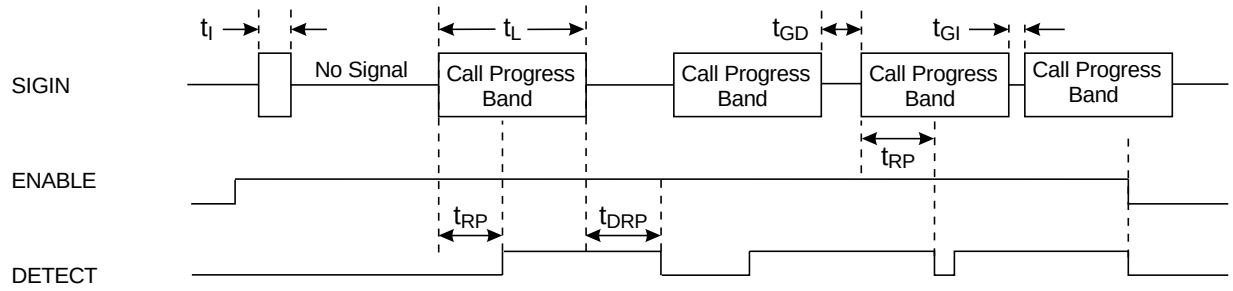
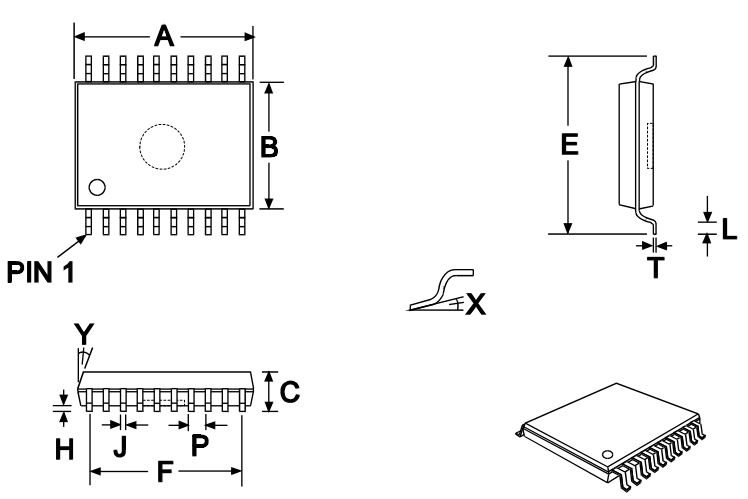


Figure 4: µC Parallel Interface Timings

6.2 Packaging

The CMX673 is available in the following packages. Additional package styles may be available to meet specific design requirements.



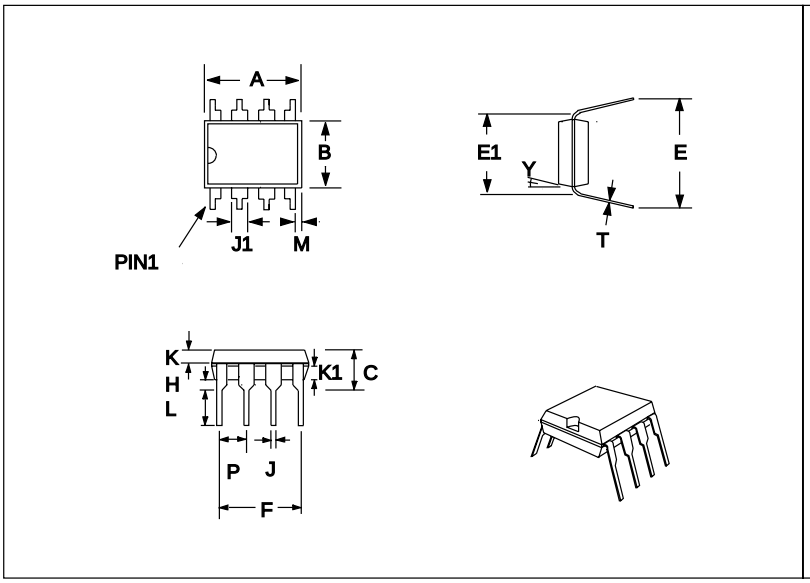
DIM.	MIN.	TYP.	MAX.
* A	0.252 (6.40)		0.260 (6.60)
* B	0.169 (4.30)		0.177 (4.50)
C	———		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
F		0.230 (5.85)	
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.026 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
X	0°		7°
Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 20-pin TSSOP (E3) Mechanical Outline: *Order as part no. CMX673E3*

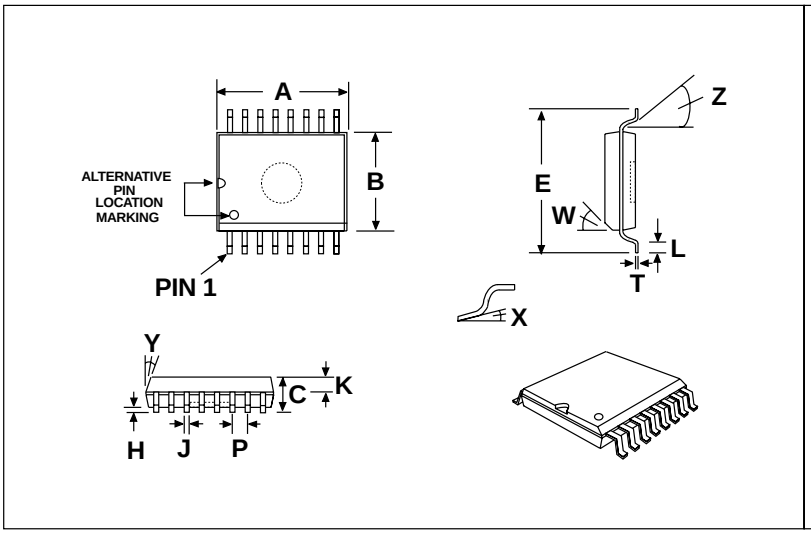


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.346 (8.790)		0.400 (10.16)
B	0.240 (6.10)		0.260 (6.60)
C	0.145 (3.68)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.87).
E1	0.290 (7.37)		0.325 (8.22)
F		0.30 (7.62)	
H	0.015 (0.38)		0.040 (1.01)
J	0.015 (0.38)		0.023 (0.58)
J1	0.045 (1.14)		0.065 (1.65)
K		0.060 (1.52)	
K1		0.060 (1.52)	
L	0.121 (3.07)		0.150 (3.81)
M	0.020 (0.51)		0.033 (0.84)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 8-pin PDIP Mechanical Outline: ***order as part no. CMX673P1***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin SOIC Mechanical Outline: ***order as part no. CMX673D4***

