MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX829 Baseband Signal Processor

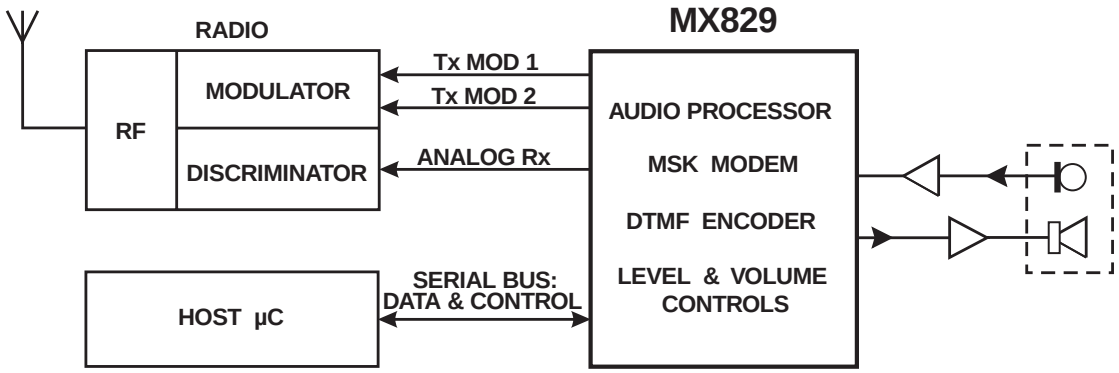
PRELIMINARY INFORMATION

Features

- **Rx Audio Processing**
- **Tx Audio Processing**
- **1200/2400 Baud Modem**
- **DTMF Encoder**
- **Low Voltage Operation**
- **"C-BUS" Compatible**
- **Host µC Interface**

Applications

- **ETS/MPT/PAA Standards Compatible**
- **LMR/PAMR/PMR Trunked Systems**
- **Multi-standard Modem Formats**



The MX829 is a low voltage CMOS integrated circuit, designed to provide baseband audio and system signal-processing functions required for LMR/PAMR/PMR trunked radio applications. The MX829 operates in half-duplex mode under the serial-bus control of a host µC.

The MX829 incorporates a dual-rate 1200/2400bps MSK modem, with a software-flexible choice of synchronization codewords, data run-length and CRC checking to suit a wide range of applications. These features allow very flexible handling of user defined data on traffic channels in addition to the network signaling sent on control channels. A 16 character DTMF encoder is available in the transmit mode. Software programmable output level-adjustment facilitates two-point modulation circuits.

The audio processing stages include transmit and receive filtering (based on standards specified for 12.5kHz and 25kHz LMR/PAMR/PMR channel operation), transmit deviation limiting, and a programmable Rx volume control. Power saving is automatic when audio functions are disabled.

The MX829 is designed for use in radios compatible with MPT1327, PAA1382 and ETS 300 086 Trunking Standards. The features and flexibility of the MX829 ensure that it is equally suitable for use with modified or proprietary standards.

The MX829 is available in the following packages: 24-pin SSOP (MX829DS), 24-pin SOIC (MX829DW), and 24-pin PDIP (MX829P).

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CONTENTS

Section **Page**

1. Block Diagram

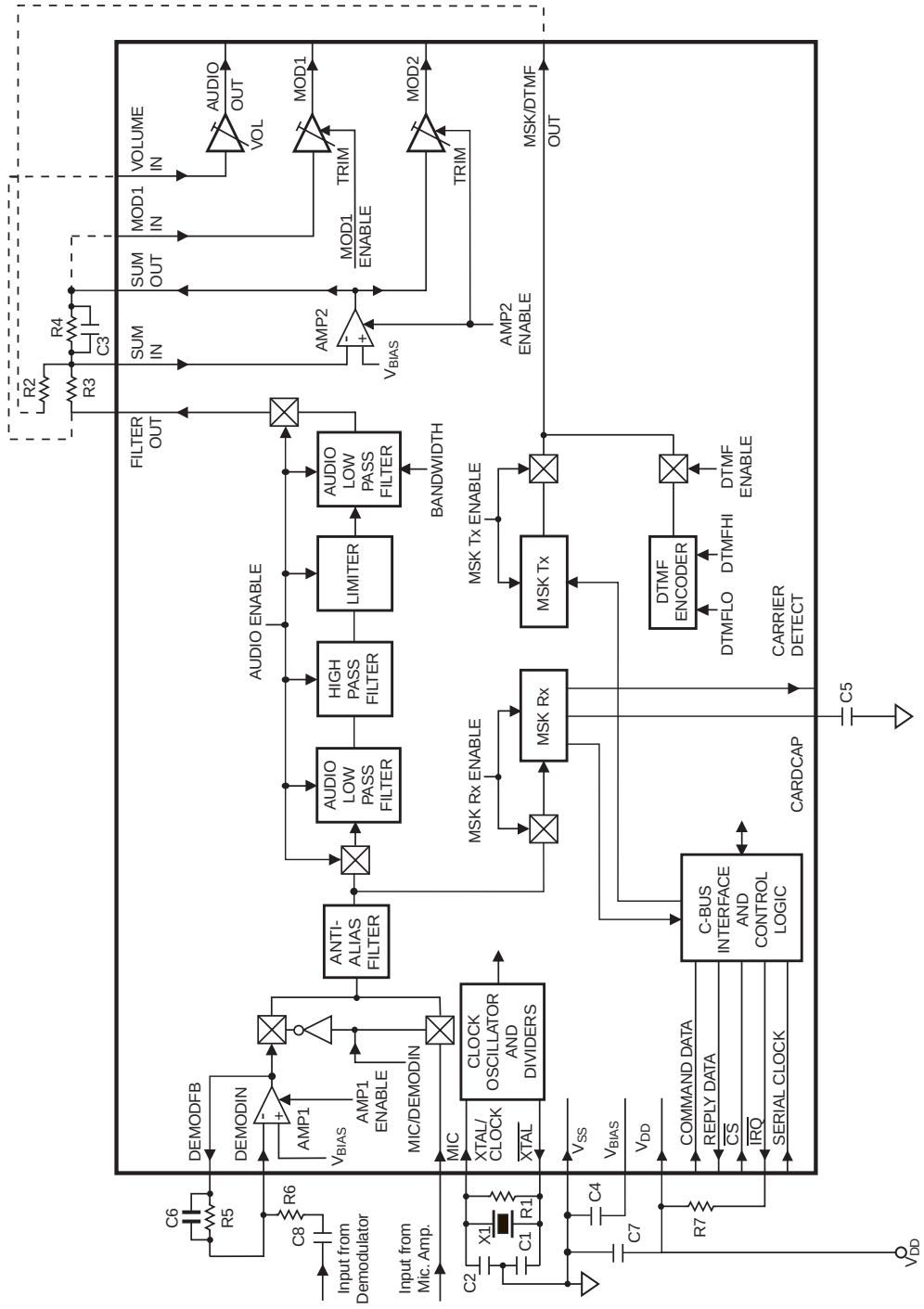

Figure 1: Block Diagram

2. Signal List

PIN NO	SIGNAL	TYPE	DESCRIPTION
1	$\overline{\text{XTAL}}$	output	Inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	Input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	"C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the device. See section 7.1.4
4	COMMAND DATA	input	"C-BUS" serial data input from the µController. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See section 7.1.4.
5	REPLY DATA	output	"C-BUS" serial data output to the µController. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{\text{CS}}$ input. This 3-state output is held at high impedance when not sending data to the µController. See section 7.1.4.
6	$\overline{\text{CS}}$	input	"C-BUS" data loading control function: this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See section 7.1.4.
7	$\overline{\text{IRQ}}$	output	This output indicates an interrupt condition to the µController by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pull-up resistor is required. The conditions that cause interrupts are indicated in the STATUS register and are effective if not masked out by a corresponding bit in the CONTROL register. The reading of the Status Register resets the IRQ to a high impedance and sets the contents of the Status Register to 0.
8	CARRIER DETECT	output	The carrier detect output for the MSK Rx.
9	CD CAP	output	The carrier detect integrating capacitor.
10	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed to a capacitor mounted close to the device pins.
11	MIC	input	AC coupled Tx audio input (external amplification is required for use as a microphone input).
12	V_{SS}	Power	Negative supply (ground).
13	DEMOD IN	input	AC coupled inverting input to the Rx input amplifier (AMP1).
14	DEMOD FB	output	Output of the Rx input amplifier (AMP1)
15	FILTER OUT	output	Output of the audio filter/limiter section. In powersave mode this output is connected to V_{BIAS} via a 500kΩ resistor.
16	MSK/DTMF OUT	output	The 1200 or 2400 baud MSK Tx output and the DTMF encoder output. When enabled but not transmitting MSK or DTMF signals, or when in powersave mode, this output is connected to V_{BIAS} via a 500kΩ resistor. On power-up, this output can be any level: a General Reset command is required to ensure that this output attains V_{BIAS} initially.
17	SUM IN	input	Input to the audio summing amplifier (AMP2).
18	SUM OUT	output	Output of the audio summing amplifier (AMP2).
19	MOD1 IN	input	Input to MOD1 audio gain control.
20	VOL IN	input	Input to the audio volume control.
21	AUDIO OUT	output	Output of the audio volume control.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	Power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

3. External Components

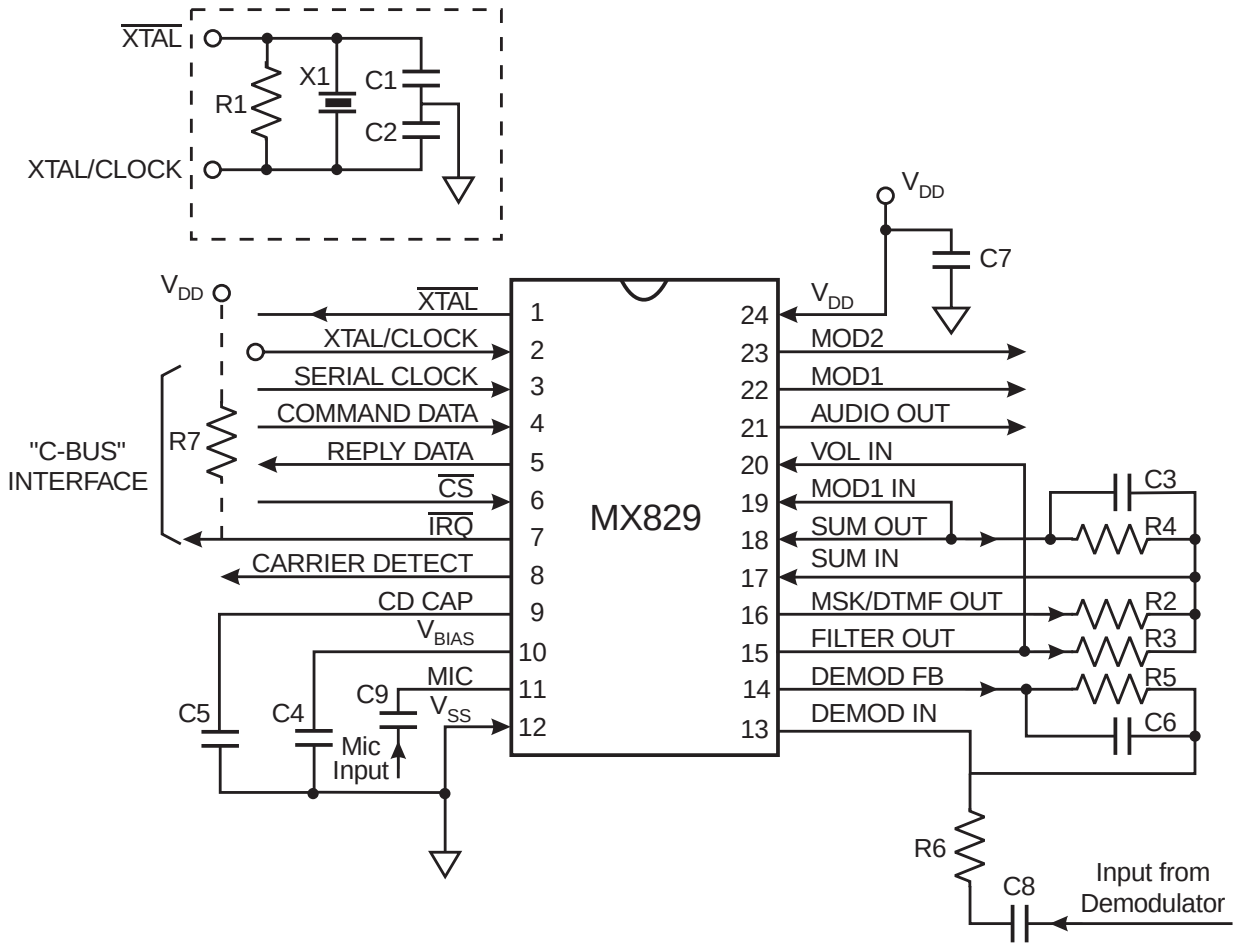

Figure 2: Recommended External Components

C1		22pF	±20%
C2		22pF	±20%
C3		68pF	±20%
C4		0.1µF	±20%
C5		0.1µF	±10%
C6		100pF	±20%
C7		0.1µF	±20%
C8	Note 2		±20%
C9		5.6nF	±20%

R1		1MΩ	±5%
R2	Note 1		±10%
R3	Note 1		±10%
R4		100kΩ	±10%
R5		100kΩ	±10%
R6	Note 2		±10%
R7		22kΩ	±10%
X1	Note 3	4.032MHz	±100ppm

External Component Notes:

1. R2, R3, R4 and C3 form the gain components for the Summing Amplifier (AMP2).
   R2 and R3 should be chosen as required from the system specification, using the following formula:

$$\text{Audio Gain} = -\frac{R4}{R3} \qquad \text{DTMF Gain} = -\frac{R4}{R2}$$

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2. R5, R6, C6 and C8 form the gain components for the Rx Input Amplifier (AMP1).

   R6 should be chosen as required by the signal level, using the following formula:

$$\text{Gain} = -\frac{R5}{R6}$$

   C8 x R6 should be chosen so as not to compromise the low frequency performance of this product.

3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

The MX829 consists of five main sections: the Audio Filter, the Programmable Attenuators, the DTMF encoder, the MSK transmitter, and the MSK receiver. These sections are controlled via a serial ("C-BUS") interface. The five sections are described below.

4.1 Audio Filtering

This consists of an input amplifier and a common audio filter section, which may be switched between Rx and Tx. The filter section comprises an anti-alias filter followed by low-pass and high-pass filtering with an amplitude limiter to set the maximum deviation. Three variable attenuation blocks may be used to set the volume (in Rx) or the modulation level (in Tx). Pre- and de-emphasis can be added externally using resistors and capacitors around AMP1, AMP2 and the microphone amplifiers, see Figure 7,Figure 8, and Figure 9. The anti-alias filter is designed to reduce aliasing effects above 50kHz which is approximately half the internal filter's sample rate.

The filtering is designed to meet the ETS 300 086 specification.

Various powersave modes are incorporated.

4.2 MOD1 and MOD2 Attenuators

The MOD1 input can be connected directly to SUM OUT, so that the MOD1 and MOD2 outputs can then be used for two point modulation. Alternatively, the MOD1 attenuator can be used for auxiliary gain adjustment, in which case the input signal must be ac coupled with a suitable capacitor.

4.3 DTMF Encoder

This generates the standard DTMF tones according to the CONTROL 2 Register settings. It also has a powersave mode.

4.4 MSK Tx

The Tx function of the MSK modem continuously operates in a free format mode, which means that the preamble and frame sync have to be programmed like normal data bytes. However, a 2-byte checksum may be generated automatically by simply marking the beginning and end of the data to be used. Any number of whole bytes may be used to generate the checksum.

After the last byte has been transmitted one additional "hang bit" is automatically added to the end. All Tx operations are programmed from the "C-BUS" via an 8-bit buffer. The Tx part of the MSK Modem has a Powersave mode

The modulation output is one cycle of 1200Hz for a "1" and one and a half cycles of 1800Hz for a "0" at 1200 baud, or one half cycle of 1200Hz for a "1" and one cycle of 2400Hz for a "0" at 2400 baud.

4.5 MSK Rx

In Rx, the modem automatically achieves bit sync and then recognizes the previously selected SYNC and/or SYNT word of the MPT1327, ETS 300 230 or PAA1382 specifications. At the same time as one of the above, it can also recognize a user programmed 16-bit RX SYNC WORD.

On reception of the SYNC, SYNT or RX SYNC WORD, the device will automatically (or manually at any time) start checking the data and checksum. It provides a 1-bit correct/incorrect result every byte, so that any number of bytes can be checked.

The Rx part of the MSK modem operates at 1200 or 2400 baud and has a powersave mode. Both MSK Rx and Tx work in half duplex mode.

5. Software Description

5.1 Address/Commands

Instructions and data are transferred, via "C-BUS", in accordance with the timing information given in Figure 14.

Instruction and data transactions to and from the MX829 consist of an Address/Command (A/C) byte followed by either:

1. a further instruction or data (1 or 2 bytes)
2. a status or Rx data reply (1 byte)

5.1.1 8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$10	CONTROL 1	AMP1	AMP2	AUDIO	MSKRX	MSKTX	UK/F	MIC	B/W
$11	CONTROL 2	CHKSUM	DTMFEN	DTMFHI	DTMFLO	DTMF3	DTMF2	DTMF1	DTMF0
$13	AUDIO ATTENUATION	0	0	0	<---------- GAIN ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$40	CONTROL 3/ IRQ ENABLE	0	1200/2400	TXIDLEM	RXDATAM	TXDATAM	RX SYNC WORD PRIME	SYNT PRIME	SYNC PRIME
$43	TXDATA	<---------- TXDATA ----------> BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

5.1.2 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$12	MOD LEVELS (1)	0	0	MOD 1 ENABLE	<---------- MOD 1 ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	<---------- MOD 2 ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$44	RX SYNC WORD (1)	<---------- RX SYNC WORD ----------> BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	(2)	<---------- RX SYNC WORD ----------> BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

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5.2 Write Only Register Description

5.2.1 RESET Register (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific states as listed below:

REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 D0)
CONTROL 1	0	0	0	0	0	0	0	0
CONTROL 2	0	0	0	0	0	0	0	0
CONTROL 3/IRQ ENABLE	0	0	0	0	0	0	0	0
AUDIO ATTENUATION	0	0	0	0	0	0	0	0
TXDATA	X	X	X	X	X	X	X	X
MOD LEVELS (1)	0	0	0	0	0	0	0	0
MOD LEVELS (2)	0	0	0	0	0	0	0	0
RX SYNC WORD (1)	X	X	X	X	X	X	X	X
RX SYNC WORD (2)	X	X	X	X	X	X	X	X
STATUS	0	0	0	0	0	0	0	0
RXDATA	X	X	X	X	X	X	X	X

X = undefined

5.2.2 CONTROL1 Register (Hex address $10)

This register is used to control the functions of the device as described below:

AMP1 (Bit 7)	When this bit is "1", AMP1 is enabled. When this bit is "0", AMP1 is disabled (i.e. powersaved).
AMP2 (Bit 6)	When this bit is "1", both AMP2 and MOD2 are enabled. When this bit is "0", both AMP2 and MOD2 are disabled (i.e. powersaved) and the MOD2 output is pulled to V_{BIAS} via a 1MΩ resistor.
AUDIO (Bit 5)	When this bit is "1", the audio filter/limiter section is enabled. When this bit is "0", the audio filter/limiter section is disabled (i.e. powersaved).
MSKRX (Bit 4)	When this bit is "1", the MSK Rx is enabled. When this bit is "0", the MSK Rx is disabled (i.e. powersaved).

Note: The MSK Rx and Tx cannot both be enabled at the same time. If both MSKRX and MSKTX are "1", then they will both be disabled (i.e. powersaved).

MSKTX (Bit 3)	When this bit is "1", the MSK Tx is enabled. When this bit is "0", the MSK Tx is disabled (i.e. powersaved).

Note: The MSK Tx and Rx cannot both be enabled at the same time. If both MSKTX and MSKRX are "1", then they will both be disabled (i.e. powersaved).

The DTMF Encoder and MSK Tx cannot both be enabled at the same time. If both DTMFEN and MSKTX are "1", then they will both be disabled.

UK/F (Bit 2)	When this bit is "1", the SYNC/SYNT is set to the PAA standard of "1011010000110011" (SYNC) When this bit is "0", the SYNC/SYNT is set to the MPT standard of "1100010011010111" (SYNC)
MIC (Bit 1)	When this bit is "1", the MIC input is enabled and the AMP1 (DEMODIN) input is disabled. When this bit is "0", the AMP1 (DEMODIN) input is enabled and the MIC input is disabled.
B/W (Bit 0)	When this bit is "1", the bandwidth of the audio path is set wide for 20kHz/25kHz RF channel spacing. When this bit is "0", the bandwidth of the audio path is set narrow for 12.5kHz RF channel spacing.

5.2.3 CONTROL 2 Register (Hex address $11)

This register is used to control the functions of the device as described below:

CHKSUM (Bit 7)	In the Tx mode, when this bit is "1", the checksum generator is enabled. All complete bytes that are transmitted after this time are used in the checksum calculation. When this bit goes from "1" to "0", the checksum generator will complete its calculations on the current byte and the result will be sent as the next two bytes of transmitted data. In the Rx mode, the "0" to "1" transition of the CHKSUM bit is used at the start of the next byte received at DEMODIN to manually reset the Rx checksum calculation, see Figure 4. The calculation can also be reset automatically by a SYNC, SYNT, or RX SYNC WORD detection - see section 5.2.5. In this case, the Rx checksum calculation starts with the first data byte after the 2-byte sync word has been detected. The CHKSUM bit can be reset to "0" at any time. The result of the checksum is made available in the STATUS Register after the reception of every complete byte (See section 5.3.1). Note that the device is designed to work with any message length, and as a consequence it is not aware of the position of the checksum within the incoming data message. It thus performs a checksum assessment after every received byte. The controlling software should use its knowledge of the system message length in order to determine which RXSUMF reading is valid, i.e. after the second of the two checksum bytes has been received. The timing of data bytes relative to the checksum bit is shown in Figure 3 and Figure 4.

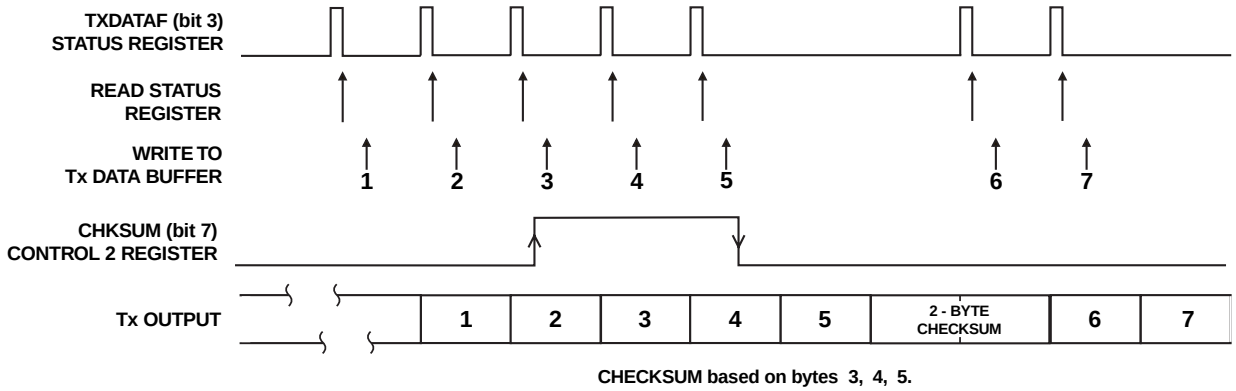

Figure 3: Checksum Generation in Tx Mode

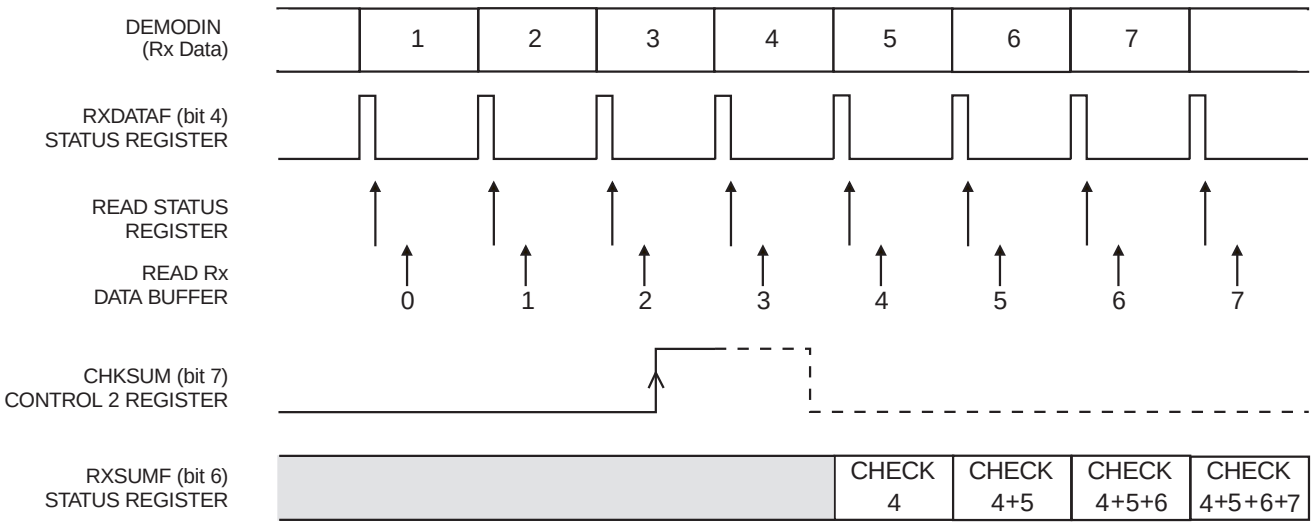

Figure 4: Checksum Calculation in Rx Mode

DTMFEN (Bit 6)	When this bit is "1", the DTMF output is enabled. When this bit is "0", the DTMF output is disabled. As the powersave of the DTMF is performed in the DTMFHI and DTMFLO registers, this bit allows a fast start up time for the tones.

Note: The DTMF Encoder and MSK Tx cannot both be enabled at the same time. If both DTMFEN and MSKTX are "1", then both will be disabled.

DTMFHI (Bit 5)	When this bit is "1", the DTMF high frequency tone generator is enabled. It will not appear on the output pin unless or until the DTMFEN is "1". When this bit is "0", the DTMF high frequency tone generator is disabled (i.e. powersaved).
DTMFLO (Bit 4)	When this bit is "1", the DTMF low frequency tone generator is enabled. It will not appear on the output pin unless or until the DTMFEN is "1". When this bit is "0", the DTMF low frequency tone generator is disabled (i.e. powersaved).
DTMF3, DTMF2, DTMF1, DTMF0 (Bit 3, Bit 2, Bit 1, Bit 0)	These four bits define the DTMF tones according to the table below:

Bit 3	Bit 2	Bit 1	Bit 0	DTMF Tones	DTMF 'Digit'
0	0	0	0	1209Hz + 697Hz	1
0	0	0	1	1209Hz + 770Hz	4
0	0	1	0	1209Hz + 852Hz	7
0	0	1	1	1209Hz + 941Hz	*
0	1	0	0	1337Hz + 697Hz	2
0	1	0	1	1337Hz + 770Hz	5
0	1	1	0	1337Hz + 852Hz	8
0	1	1	1	1337Hz + 941Hz	0
1	0	0	0	1478Hz + 697Hz	3
1	0	0	1	1478Hz + 770Hz	6
1	0	1	0	1478Hz + 852Hz	9
1	0	1	1	1478Hz + 941Hz	#
1	1	0	0	1634Hz + 697Hz	A
1	1	0	1	1634Hz + 770Hz	B
1	1	1	0	1634Hz + 852Hz	C
1	1	1	1	1634Hz + 941Hz	D

5.2.4 AUDIO ATTENUATION Register (Hex Address $13)

The five least significant bits in this register are used to set the attenuation of the audio volume control according to the table below:

4	3	2	1	0		Audio Attenuation
0	0	0	0	0		Off
0	0	0	0	1		48.0dB
0	0	0	1	0		46.4dB
0	0	0	1	1		44.8dB
0	0	1	0	0		43.2dB
0	0	1	0	1		41.6dB
0	0	1	1	0		40.0dB
0	0	1	1	1		38.4dB
0	1	0	0	0		36.8dB
0	1	0	0	1		35.2dB
0	1	0	1	0		33.6dB
0	1	0	1	1		32.0dB
0	1	1	0	0		30.4dB
0	1	1	0	1		28.8dB
0	1	1	1	0		27.2dB
0	1	1	1	1		25.6dB
1	0	0	0	0		24.0dB
1	0	0	0	1		22.4dB
1	0	0	1	0		20.8dB
1	0	0	1	1		19.2dB
1	0	1	0	0		17.6dB
1	0	1	0	1		16.0dB
1	0	1	1	0		14.4dB
1	0	1	1	1		12.8dB
1	1	0	0	0		11.2dB
1	1	0	0	1		9.6dB
1	1	0	1	0		8.0dB
1	1	0	1	1		6.4dB
1	1	1	0	0		4.8dB
1	1	1	0	1		3.2dB
1	1	1	1	0		1.6dB
1	1	1	1	1		0dB

Note: Bits 5, 6 and 7 should always be set to "0".

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5.2.5 CONTROL 3 / IRQ ENABLE Register (Hex address $40)

This register is a mixture of control bits and interrupt mask bits, as detailed below:

Bit 7	Not used, set to zero.
1200/2400 (Bit 6)	When this bit is "1", the MSK Rx and Tx are set to operate at 1200 baud. When this bit it "0", the MSK Rx and Tx are set to operate at 2400 baud.
TXIDLEM (Bit 5)	When this bit is "1", the TXIDLE interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the TXIDLE interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
RXDATAM (Bit 4)	When this bit is "1", the RXDATA interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the RXDATA interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
TXDATAM (Bit 3)	When this bit is "1", the TXDATA interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the TXDATA interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
RX SYNC WORD PRIME (Bit 2)	When this bit is set to "1", it enables the RX SYNC WORD detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.
SYNT PRIME (Bit 1)	When this bit is set to "1", it enables the SYNT detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.
SYNC PRIME (Bit 0)	When this bit is set to "1", it enables the SYNC detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.

5.2.6 TXDATA Register (Hex Address $43)

This is the Tx data output register. It is double buffered, thus giving the user up to 8 bit periods to load in the next 8 bits. MSK data is transmitted immediately it is loaded if the transmitter is idle. Data is transmitted in 8-bit bytes, bit 7 (MSB) will be transmitted first.

5.2.7 MOD LEVELS Register **(Hex address $12)**

The six least significant bits of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and the five least significant bits of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

5	4	3	2	1	0		Mod. 1 Attenuation
0	X	X	X	X	X		Disabled (V_{BIAS})
1	0	0	0	0	0		>40dB
1	0	0	0	0	1		12.0dB
1	0	0	0	1	0		11.6dB
1	0	0	0	1	1		11.2dB
1	0	0	1	0	0		10.8dB
1	0	0	1	0	1		10.4dB
1	0	0	1	1	0		10.0dB
1	0	0	1	1	1		9.6dB
1	0	1	0	0	0		9.2dB
1	0	1	0	0	1		8.8dB
1	0	1	0	1	0		8.4dB
1	0	1	0	1	1		8.0dB
1	0	1	1	0	0		7.6dB
1	0	1	1	0	1		7.2dB
1	0	1	1	1	0		6.8dB
1	0	1	1	1	1		6.4dB
1	1	0	0	0	0		6.0dB
1	1	0	0	0	1		5.6dB
1	1	0	0	1	0		5.2dB
1	1	0	0	1	1		4.8dB
1	1	0	1	0	0		4.4dB
1	1	0	1	0	1		4.0dB
1	1	0	1	1	0		3.6dB
1	1	0	1	1	1		3.2dB
1	1	1	0	0	0		2.8dB
1	1	1	0	0	1		2.4dB
1	1	1	0	1	0		2.0dB
1	1	1	0	1	1		1.6dB
1	1	1	1	0	0		1.2dB
1	1	1	1	0	1		0.8dB
1	1	1	1	1	0		0.4dB
1	1	1	1	1	1		0dB

4	3	2	1	0		Mod. 2 Attenuation
0	0	0	0	0		>40dB
0	0	0	0	1		6.0dB
0	0	0	1	0		5.8dB
0	0	0	1	1		5.6dB
0	0	1	0	0		5.4dB
0	0	1	0	1		5.2dB
0	0	1	1	0		5.0dB
0	0	1	1	1		4.8dB
0	1	0	0	0		4.6dB
0	1	0	0	1		4.4dB
0	1	0	1	0		4.2dB
0	1	0	1	1		4.0dB
0	1	1	0	0		3.8dB
0	1	1	0	1		3.6dB
0	1	1	1	0		3.4dB
0	1	1	1	1		3.2dB
1	0	0	0	0		3.0dB
1	0	0	0	1		2.8dB
1	0	0	1	0		2.6dB
1	0	0	1	1		2.4dB
1	0	1	0	0		2.2dB
1	0	1	0	1		2.0dB
1	0	1	1	0		1.8dB
1	0	1	1	1		1.6dB
1	1	0	0	0		1.4dB
1	1	0	0	1		1.2dB
1	1	0	1	0		1.0dB
1	1	0	1	1		0.8dB
1	1	1	0	0		0.6dB
1	1	1	0	1		0.4dB
1	1	1	1	0		0.2dB
1	1	1	1	1		0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is "1" the MOD1 attenuator is enabled. When this bit is "0" the MOD1 attenuator is disabled (i.e. powersaved). Bits 6 and 7 in the first byte and bits 5, 6 and 7 in the second byte should always be set to "0". MOD LEVELS (1) register is loaded first.

Note: The MOD2 attenuator is enabled by the AMP2 ENABLE signal (bit 6 of CONTROL1 register).

5.2.8 RX SYNC WORD Register (Hex $44)

This is a two byte register that defines the 16-bit programmable synchronization word. This word is compared with the incoming Rx data and, if a match is found, it is indicated in the STATUS register and an interrupt is generated. Bit 15, the MSB of the first byte, is loaded first.

8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$41	STATUS	0	RXSUMF	TXIDLEF	RXDATAF	TXDATAF	RX SYNC WORDF	SYNTF	SYNCF
$42	RXDATA	<---------- RXDATA ---------->							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

5.3 Read Only Register Description

5.3.1 STATUS Register (Hex address $41)

This register is used to indicate the status of the device as described below:

Note: After reading the contents of the Status Register, all bits in the Status Register are reset to a zero state and the IRQ, externally generated by the MX829, is cleared.

Bit 7	Not used, always set to zero.
RXSUMF (Bit 6)	When this bit is "1", the Rx checksum is correct. When this bit is "0", the Rx checksum is incorrect. This bit is updated and latched in, after reception of every eight bits (see section 5.2.3).
TXIDLEF (Bit 5)	When all the Tx data and any checksum and one "hang-bit" have been transmitted, this bit will be set to "1" to indicate that the transmitter is idle. This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt may be generated depending on the state of the TXIDLEM bit in the CONTROL 3 / IRQ ENABLE register.
RXDATAF (Bit 4)	When a full byte of data is received and is available in the RXDATA register, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1" an interrupt may be generated depending on the state of the RXDATAM bit in the CONTROL 3 / IRQ ENABLE register.
TXDATAF (Bit 3)	When the Tx data buffer is empty this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt may be generated depending on the state of the TXDATAM bit in the CONTROL 3 / IRQ ENABLE register.
RX SYNC WORDF (Bit 2)	This bit is only defined when RX SYNC WORD PRIME is enabled. When the data sequence specified in the RX SYNC WORD register has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.
SYNTF (Bit 1)	This bit is only defined when SYNT PRIME is enabled. When the data sequence specified by SYNT has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.
SYNCF (Bit 0)	This bit is only defined when SYNC PRIME is enabled. When the data sequence specified by SYNC has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.

5.3.2 RXDATA Register **(Hex address $42)**

This register contains the last byte of data received. It is updated every 8 bits at the same time as the RXSUMF bit in the STATUS register is updated.

The RXDATA register is double buffered, thus giving the user up to 8 bit periods to read the data before it is overwritten by the next byte.

5.4 MSK Checksum Generation and Checking

5.4.1 Generation

The checksum generator takes the m x 8 bits from the m bytes of information, sequentially loaded into the TXDATA register and divides them modulo-2, by the generating polynomial:

$$X15 + X14 + X13 + X11 + X4 + X2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial m x 8 bits and the 15-bit remainder (with the last bit inverted).

This 16-bit word is used as the "CHECKSUM". See Figure 5.

(m = the number of bytes in the information to be sent)

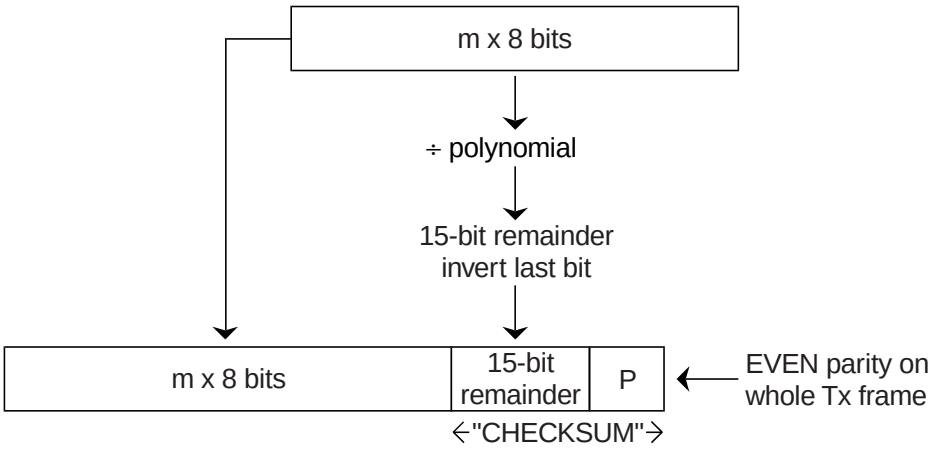

Figure 5: Checksum Generation

5.4.2 Checking

The checksum checker performs two tasks:

It takes the first n-1 bits of a received (n = 8m + 16 bits) message, inverts bit n-1, and divides them modulo-2, by the generating polynomial:

X15 + X14 + X13 + X11 + X4 + X2 + 1

The 15 bits remaining in the polynomial divider are checked for all zero.

Secondly, it generates an EVEN parity bit from the first n-1 bits of a received message and compares this bit with the received parity bit (bit n). See Figure 6.

If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the RXSUMF bit (STATUS register bit 6) is set. This is updated and latched every 8 bits, starting at the bit immediately after the initialization of the bit counter. This initialization takes place on detection of frame synchronization, i.e. the matching of received data to the SYNC, SYNT or RX SYNC WORD.

Note that the checksum is calculated on the received data before it is double buffered (see Figure 4).

n = the number of bits in the received message

m = the number of bytes of transmitted data, excluding checksum

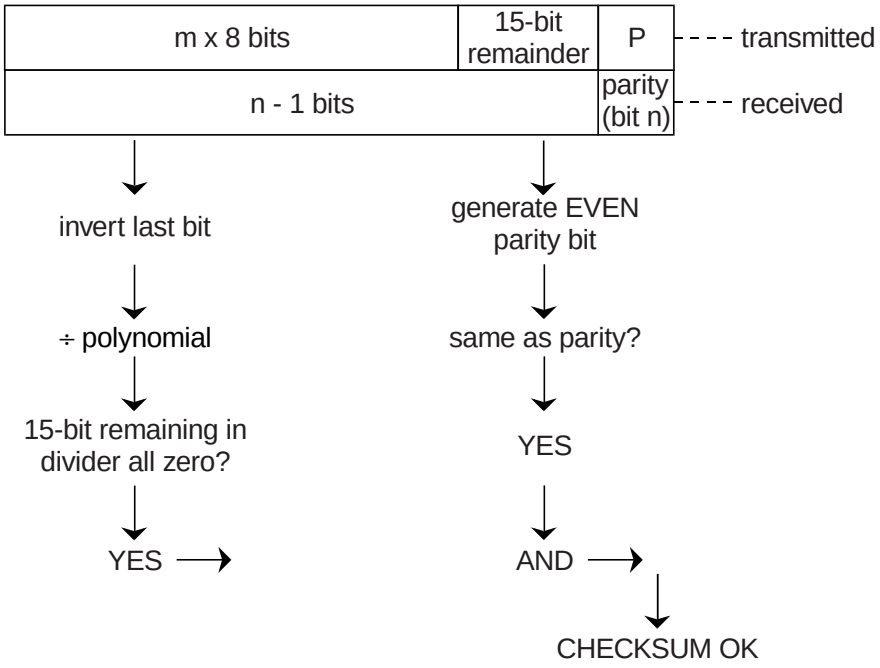

Figure 6: Checksum Checking

6. Application

The following block diagrams show the possible arrangements for the pre- and de-emphasis required by PAA1382 and MPT1327 specifications.

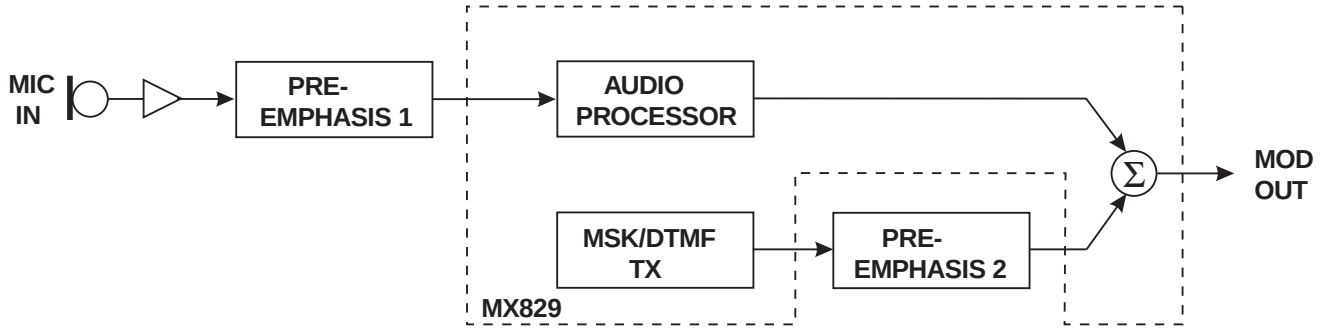

Figure 7: Transmitter Pre-emphasis

Note: Both pre-emphasis positions shown, as required by the PAA1382 specification. Remove pre-emphasis 2 for the MPT1327 specification requirement.

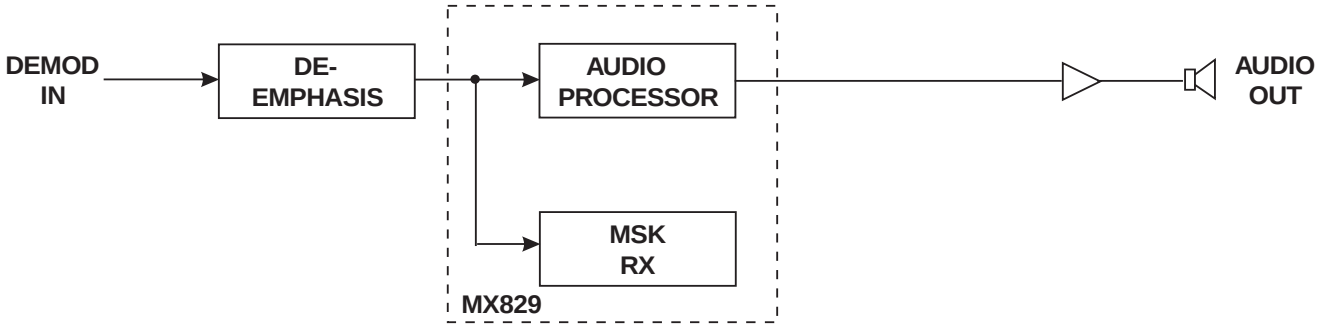

Figure 8: PAA1382 Receiver De-emphasis

Note: De-emphasis shown in all paths, as required by the PAA1382 specification.

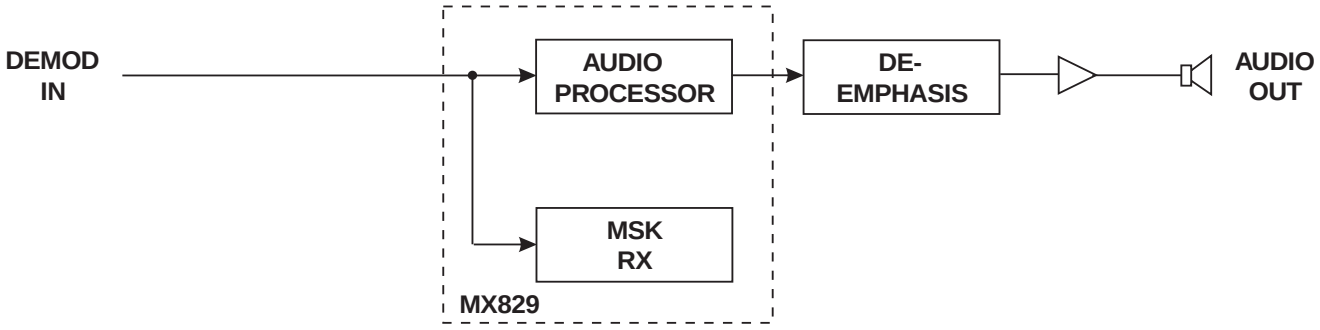

Figure 9: MPT1327 Receiver De-emphasis

Note: De-emphasis shown in audio path only, as required by the MPT1327 specification.

6.1 Programming the MX829

The MX829 should be programmed in the following manner:

1. Perform a General Reset when first applying power to the MX829.
2. Program the MX829 configuration while in powersave.
   e.g. UK/F, MIC, B/W, 1200/2400, DTMF0-3, DTMFHI, DTMFLO, TXIDLEM, RXDATAM, TXDATAM, RX SYNC WORD PRIME, SYNT PRIME, SYNC PRIME, MOD1, MOD2, RX SYNC WORD and AUDIO ATTENUATOR.
3. Take the appropriate parts of the MX829 out of powersave by enabling:
   AMP1, AMP2, MOD1, MOD2, AUDIO and (DTMFEN or MSKTX or MSKRX).
4. In DTMF Tx mode, a DTMF tone will be generated for the duration that DTMFEN is set to "1".
5. In MSK Rx mode, wait for an interrupt ($\overline{IRQ}$ = "0") or poll the STATUS register. Remember that all status flags are reset after reading the STATUS register.
   A. If RXSYNCWORDF, SYNTF or SYNCF become set to "1", the corresponding synchronization word has been detected. This indicates the start of valid Rx data. The checksum calculation will be automatically reset. Note that the timing of RXDATAF will be re-aligned by the generation of a SYNC, SYNT or RX SYNC WORD interrupt.
   B. When RXDATAF subsequently becomes set to "1", read the Rx data from the RXDATA register. (Note that RXDATAF will be set every 8 bits regardless of whether valid Rx data is being received or not. Sync and checksum patterns should be considered for validating the data).
   C. If RXSUMF becomes set to "1", then all of the Rx data sent (starting after the synchronization word and terminating with a checksum) will have been correctly received. Note that it is necessary to know in advance what message length is expected, in order to determine at which point RXSUMF is valid (i.e. after the interrupt for the second checksum data byte being received has occurred). The RXSUMF bit is invalid at all other times. When RXSUMF becomes set to "1", the last two bytes of Rx data received will represent the two-byte checksum transmitted. The first checksum byte will already have been read from the RXDATA register, the last byte is available to be read, as the RXDATAF bit will also have been set to "1".
6. In MSK Tx mode, wait for an interrupt ($\overline{IRQ}$ = "0") or poll the STATUS register. Remember that all status flags are reset after reading the STATUS register.
   A. Do not send Tx data until the TXDATAF bit has been set to "1". When the TXDATAF bit is next set to "1", write the first byte of Tx data to the TXDATA register. If the transmit buffer is empty, this data will be transmitted immediately, causing the TXDATAF bit to be set to "1" approximately one MSK bit-period after the TXDATA register has been loaded with data. (Any TXIDLEF bit set upon entering MSK Tx mode should be ignored).
   B. The next byte of Tx data should be written to the TXDATA register as soon as the TXDATAF bit has been set to "1". Once this has been done, the TXDATAF bit will again be set to "1" eight MSK bit-periods after the TXDATA register was loaded with the second byte of data.
   C. Subsequent bytes of Tx data should be written to the TXDATA register as soon as the TXDATAF bit has been set to"1". After the last byte of Tx data has been loaded, the TXDATAF bit will be set after both 8 and 16 MSK bit-periods followed by the TXIDLEF bit which will be set approximately one MSK bit-period later, to indicate that the final bit has been transmitted.
   D. The TXDATAF bit will continue to be set every 8 MSK bit-periods, regardless of whether Tx data is written to the TXDATA register or not, providing the transmitter is enabled (MSK Tx mode = MSKTX bit set to "1"). Note that while the 2-byte checksum is being generated and transmitted, the TXDATAF bit will not be set for approximately 24 MSK bit-periods.

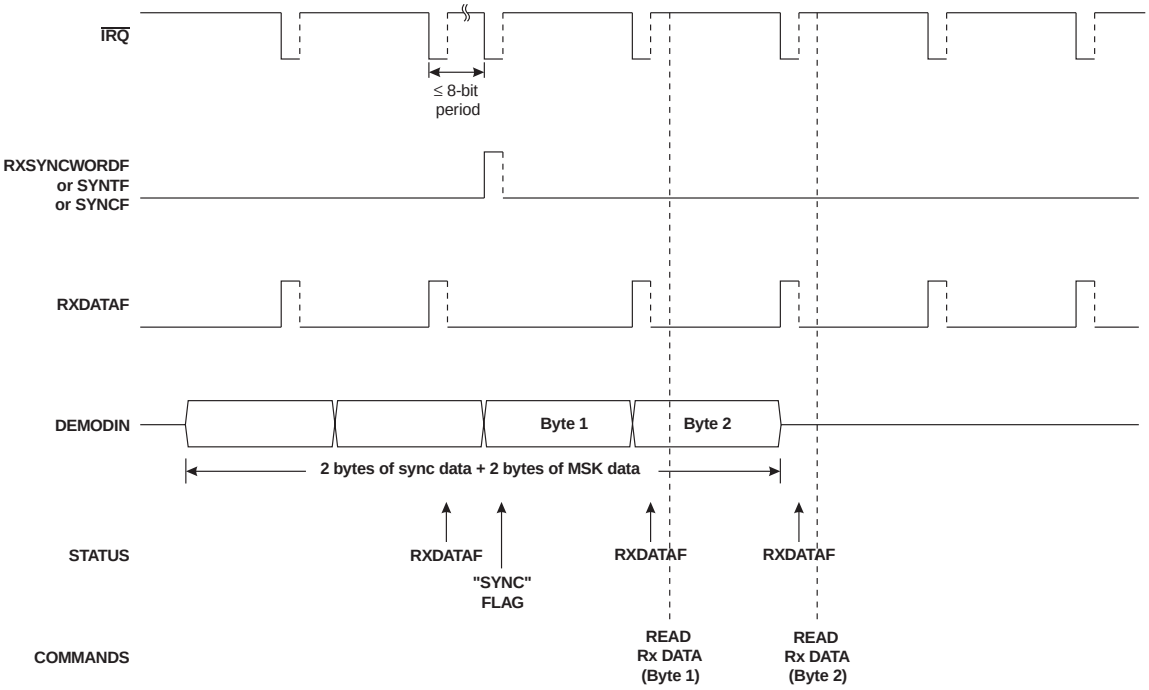

Figure 10: Reception of 2 Bytes of Data

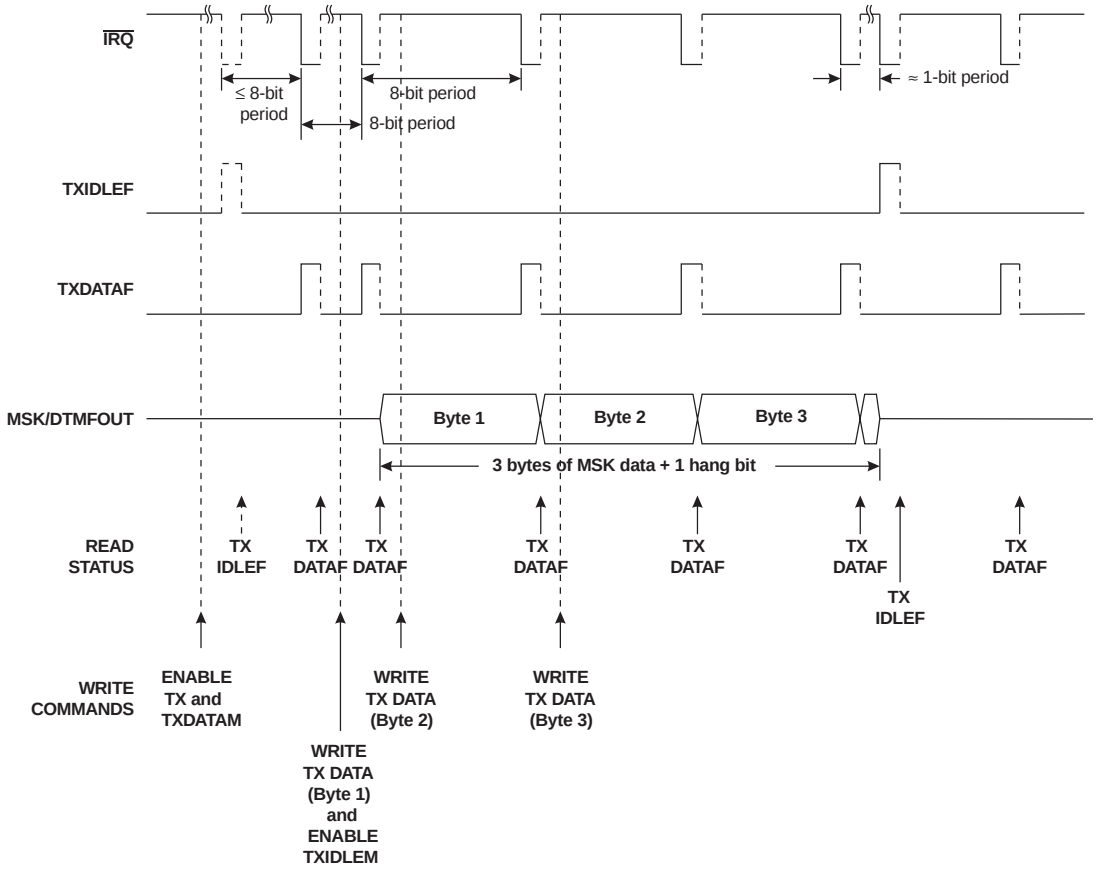

Figure 11: Transmission of 3 Bytes of Data

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

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7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, Bit Rate = 1.2k bits/sec, Noise Bandwidth = Bit Rate,
Audio Level 0dB ref. = 308mVrms at 1kHz, V_{DD} = 5.0V, T_{AMB} = 25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (Tx or Rx) (V_{DD} = 3.3V)	2		2.7	4.0	mA
I_{DD} (DTMF encode off for either Tx or Rx) (V_{DD} = 5.0V)	2		5.0	8.0	mA
I_{DD} (DTMF encode on for either Tx or Rx) (V_{DD} = 5.0V)	2			9	mA
I_{DD} (Powersaved) (V_{DD} = 3.3V)	2		0.3	1.0	mA
I_{DD} (Powersaved) (V_{DD} = 5.0V)	2		0.6	1.5	mA
"C-BUS" Interface					
Input Logic "1"		70%			V_{DD}
Input Logic "0"				30%	V_{DD}
Input Leakage Current (logic "1" or "0")		-1.0		1.0	µA
Input Capacitance				7.5	pF
Output Logic "1" (I_{OH} = 120µA)		90%			V_{DD}
Output Logic "0" (I_{OL} = 360µA)				10%	V_{DD}
"Off" State Leakage Current (V_{OUT} = V_{DD})	9			10	µA
AC Parameters					
Input Sensitivity (for 0dB output)					
Tx Audio Input (MIC)	8		308		mV_{RMS}
Rx Audio Input (DEMODFB)	8		308		mV_{RMS}
Output Drive Level					
For 60% Deviation	1, 6, 8	291	308	326	mV_{RMS}
For 100% Deviation	1, 6, 7, 8		1440		mV_{P-P}
Audio Filters					
Gain at 1kHz	5		0		dB
Passband Ripple	5	-2.0		0.5	dB
SINAD	5, 14		59		dBp
Signal Path Noise	5		-55		dB
Narrow Audio Bandwidth Setting					
Passband Frequencies	5	300		2550	Hz
Stopband Attenuation					
(f = 100Hz)	5		3.0		dB
(f = 3400Hz)	5		5.5		dB
(f = 6000Hz)	5	10.5	24		dB
(f = 12500Hz)	5	25	49		dB
Wide Audio Bandwidth Setting					
Passband Frequencies	5	300		3000	Hz
Stopband Attenuation:					
(f = 100Hz)	5		3.0		dB
(f = 3400Hz)	5		3.0		dB
(f = 6000Hz)	5	10.5	19		dB
(f = 25000Hz)	5	39.5	68		dB

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	Notes	Min.	Typ.	Max.	Units
Amp 1 and Amp 2					
Open Loop Gain (INPUT = 1mV at 100Hz)			70		dB
Unity Gain Bandwidth			5.0		MHz
Input Impedance (at 100Hz)		10			MΩ
Output Impedance					
Open Loop			6.0		kΩ
Closed Loop			600		Ω
Distortion (DTMF)			2	5	%
MSK/DTMF TX OUT					
Tx output impedance (not powersaved)	3		1.0	2.5	kΩ
Tx output impedance (powersaved)	3	300	500		kΩ
Signal Level					
MSK	1	-1	0	1	dB
DTMF High Tone	1		2.0		dB
DTMF Low Tone	1		0		dB
Distortion (DTMF)			2	5	%
MSK TX OUT					
Isochronous Distortion:					
(1200Hz - 1800Hz)			25	40	µs
(1800Hz - 1200Hz)			25	40	µs
(1200Hz - 2400Hz)			20	30	µs
(2400Hz - 1200Hz)			20	30	µs
Third Harmonic Distortion			2	3	%
Deviation Limiter					
Threshold	1		1300		mV_{P-P}
Gain		-0.5		0.5	dB
Transmitter Modulator Drives					
Input Impedance (MOD1 IN, VOLUME IN at 100Hz)			15.0		kΩ
Mod.1 Attenuator					
Nominal Adjustment Range		0		12.0	dB
Attenuation Accuracy		-1.0		1.0	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance	3		600		Ω
Mod.2 Attenuator					
Nominal Adjustment Range		0		6.0	dB
Attenuation Accuracy		-0.6		0.6	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance	3		600		Ω
Audio Output Attenuator					
Nominal Adjustment Range		0		48.0	dB
Attenuation Accuracy		-1.5		1.5	dB
Step Size			1.6		dB
Output Impedance	3		600		Ω

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	Notes	Min.	Typ.	Max.	Units
MSK Receiver					
Signal Input Dynamic Range (SNR = 50dB)	10, 11	100	230	1000	mV_{RMS}
Bit Error Rate					
SNR = 12dB at 1200 Baud	11		2.5		10^{-4}
SNR = 12dB at 2400 Baud	11		1.5		10^{-3}
SNR = 20dB at 1200/2400 Baud	11		1.0		10^{-8}
Receiver Synchronization (SNR = 12dB)	12				
Probability of Bit 16 being correct			0.995		%
Carrier Detect					
Sensitivity	12, 13			150	mV_{RMS}
Probability of Carrier Detection					
After Bit 16 (SNR = 12dB)			0.995		%
With 230mV_{RMS} Noise (No Signal)			0.05		%
Miscellaneous Impedance					
FILTER OUT			600		Ω
Tx Audio Input (MIC) (at 100Hz)		10			MΩ
Xtal/Clock Input					
'High' pulse width	4	40			ns
'Low' pulse width	4	40			ns
Input Impedance (at 100Hz)		10			MΩ
Gain (INPUT = 1mV_{RMS} at 100Hz)		20			dB

Operating Characteristics Notes:

1. Signal levels are proportional to VDD.
2. Not including any current drawn from the modem pins by external circuitry.
   A. Powersaved = all functions disabled.
   B. Tx or Rx = device configured into any half-duplex operating mode.
3. Small signal impedance. A minimum load resistance of 6kΩ is suggested.
4. Timing for an external input to the XTAL/CLOCK pin.
5. Between MIC or AMP1 inputs to Modulator and Audio outputs, see Figure 12 and Figure 13.
6. It is recommended that these output levels are used to produce 60% or 100% deviation in the transmitter.
7. With the Tx Audio input level 20dB above the level required to produce 0dB at the Output Drives.
8. With output gains set to 0dB.
9. $\overline{IRQ}$ pin.
10. See Figure 16 (variation of BER with Input Signal Level).
11. SNR = Signal to Noise Ratio in the Bit Rate Bandwidth.
12. For a "10101010101 ...01" pattern.
13. Measured with a 150mVRMS input signal (no noise).
14. dBp represents a psophometrically weighted measurement.

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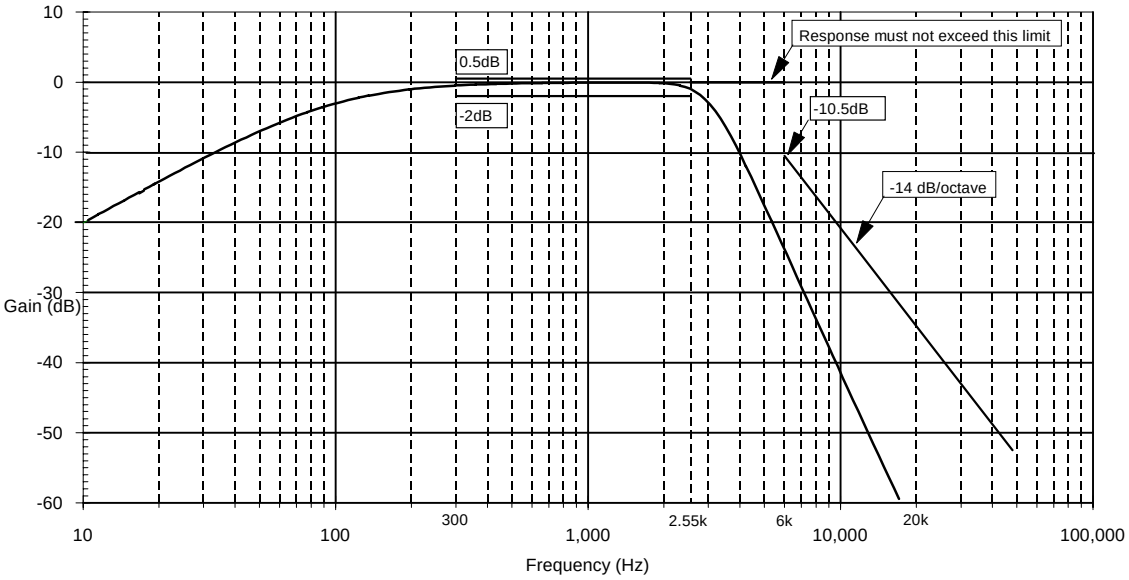


Figure 12: Overall Audio Frequency Response for 12.5kHz Channel Separation

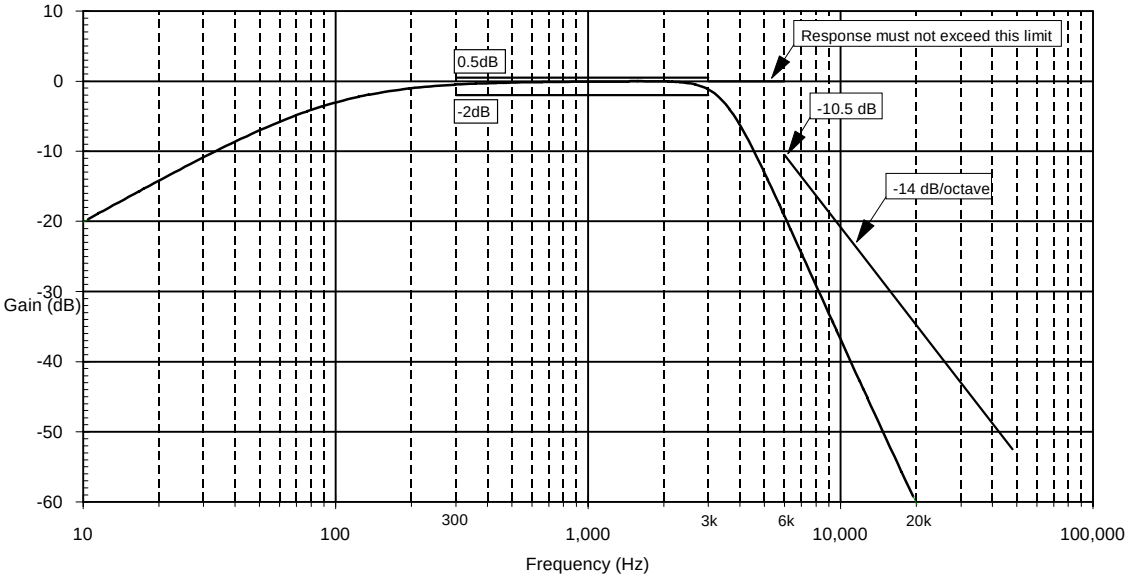


Figure 13: Overall Audio Frequency Response for 20kHz/25kHz Channel Separation

7.1.4 Timing

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 5.0V, T_{AMB} = 25°C.

	Parameter	Notes	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"		2.0			µs
t_{CSH}	Last "Clock-High to CS-High"		4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"				2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0			µs
t_{NXT}	"Inter-Byte" Time		4.0			µs
t_{CK}	"Clock-Cycle" time		2.0			µs

Timing Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. REPLY DATA is read from the peripheral MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

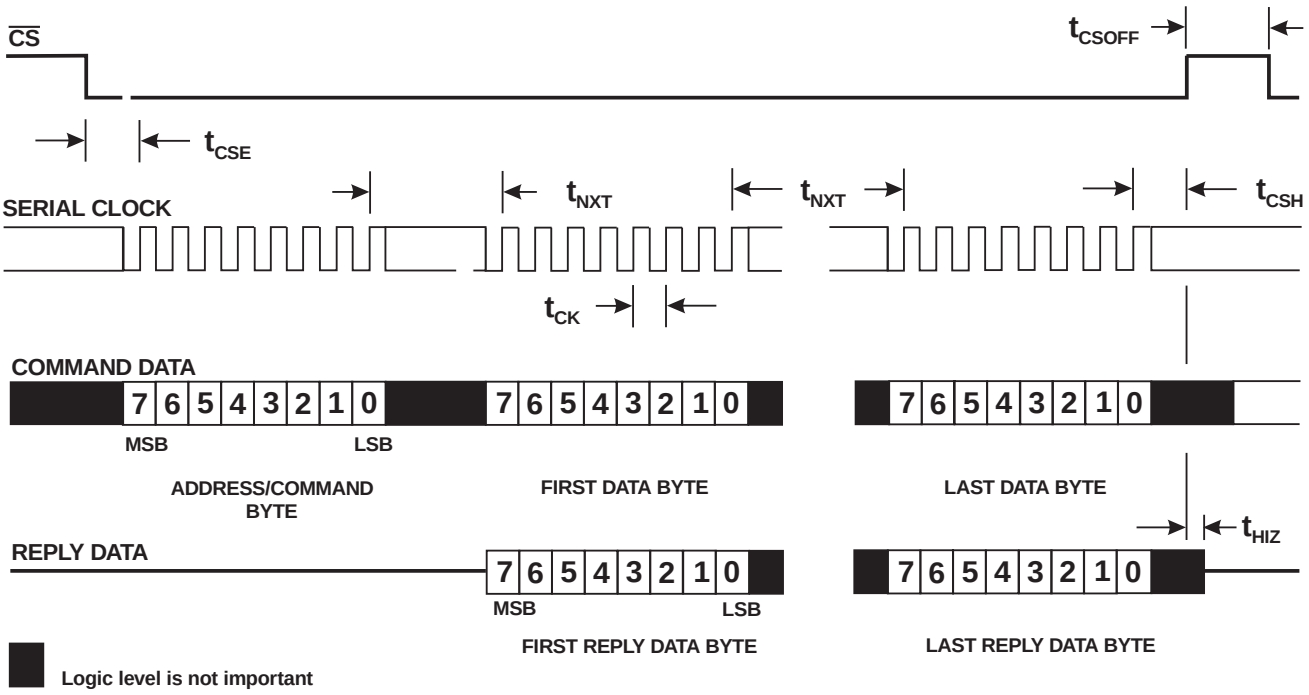


Figure 14: "C-BUS" Timing

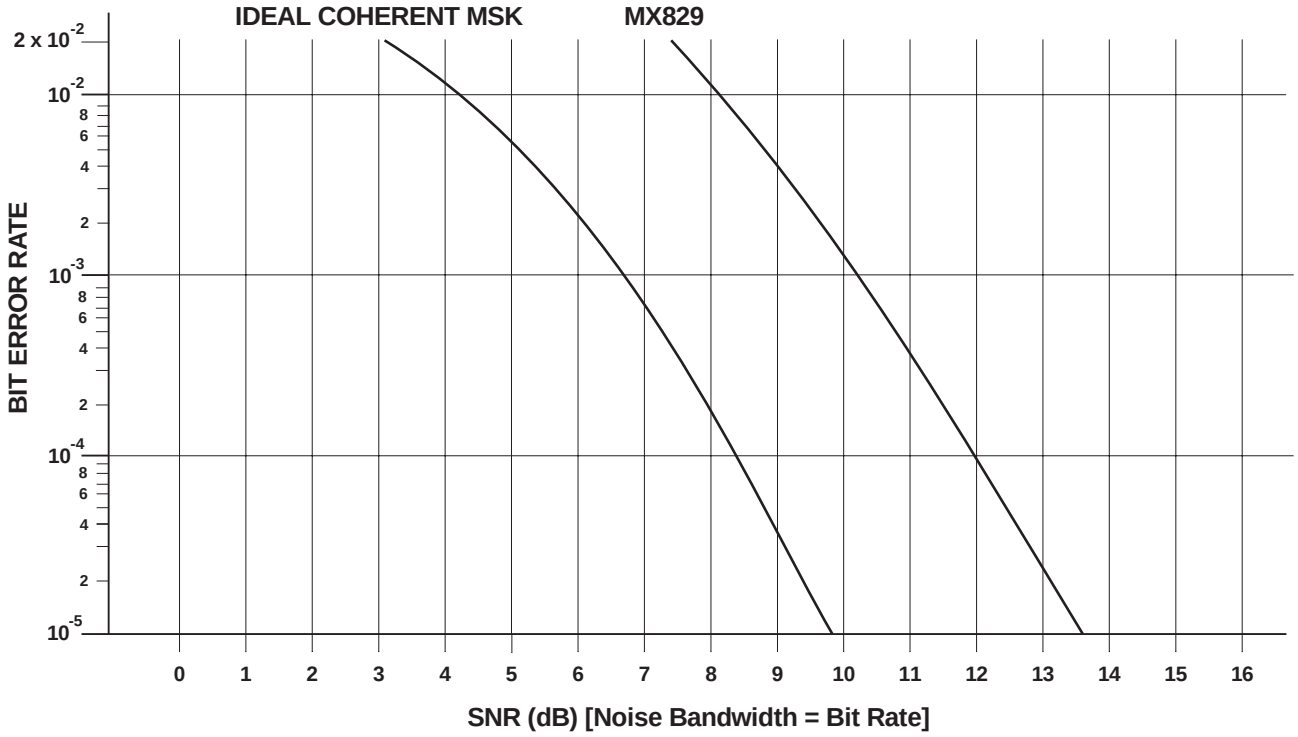


Figure 15: Bit Error Rate Graph

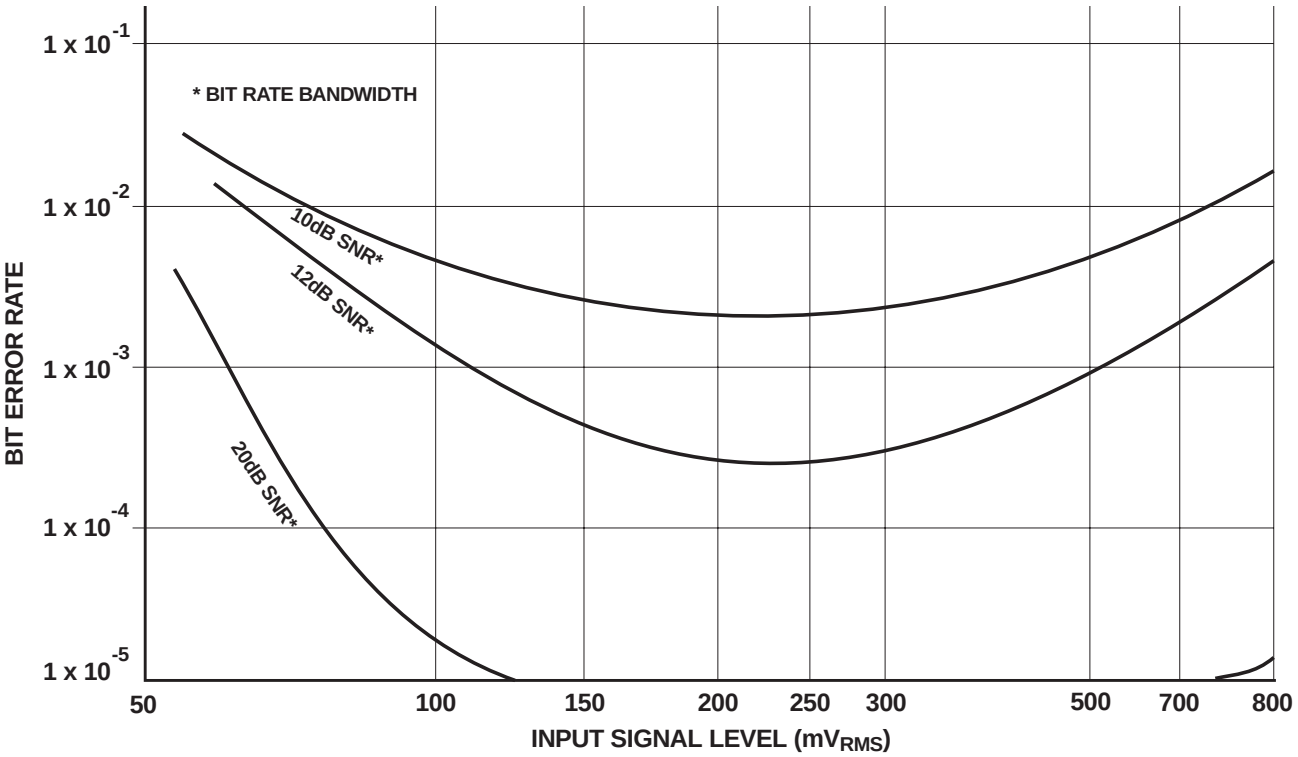
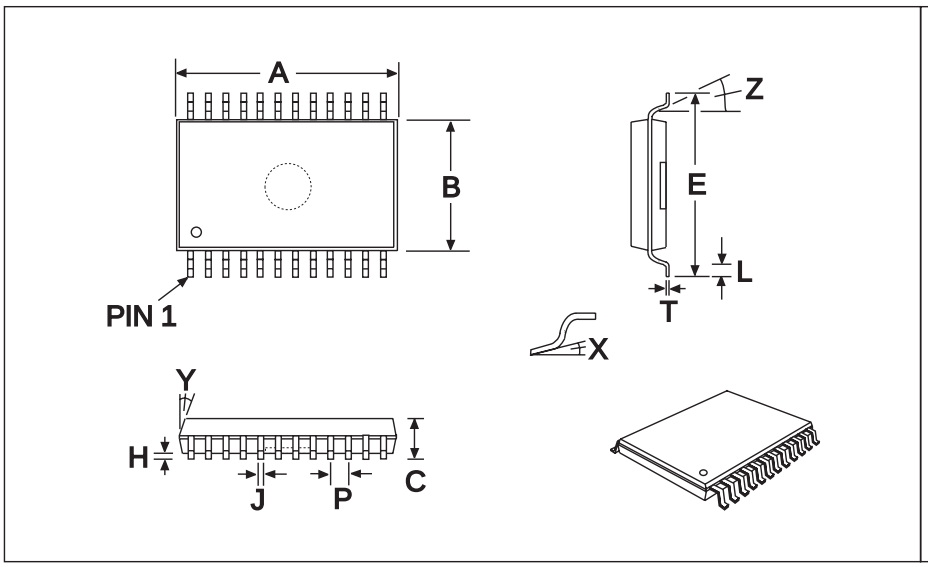


Figure 16: Typical Variation of Bit Error Rate with Input Signal Level

7.2 Packaging

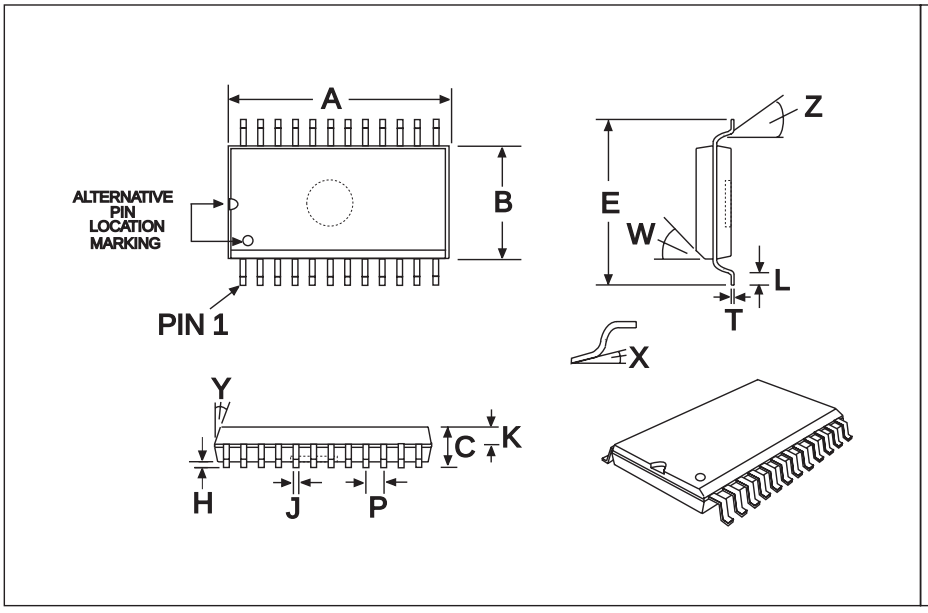


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 24-pin SSOP Mechanical Outline: *Order as part no. MX829DS*

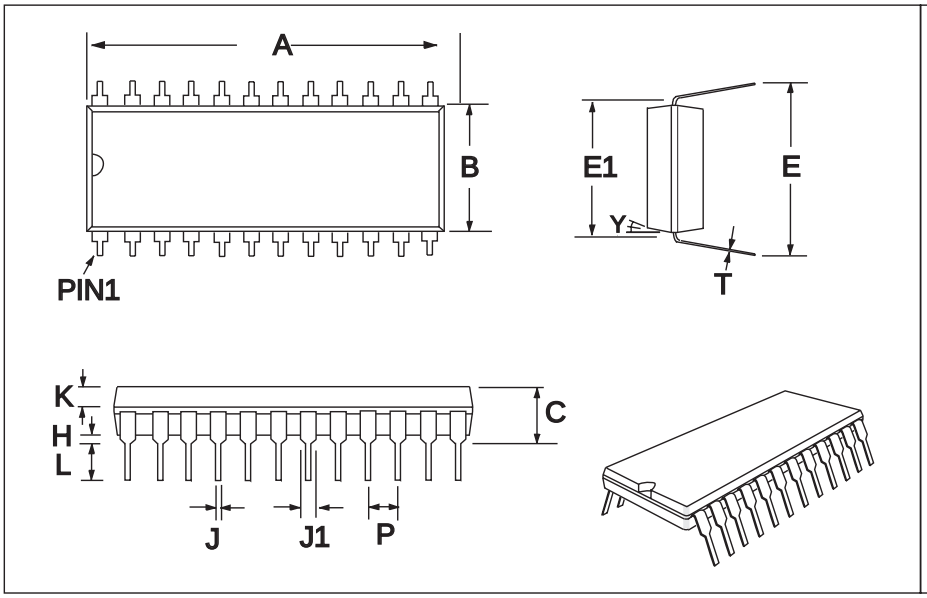


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 18: 24-pin SOIC Mechanical Outline: Order as part no. MX829DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 19: 24-pin PDIP Mechanical Outline: *Order as part no. MX829P*