MX•COM, INC.
COMMUNICATION ICs

CMX867

DATA BULLETIN

Low Power V.22 Modem

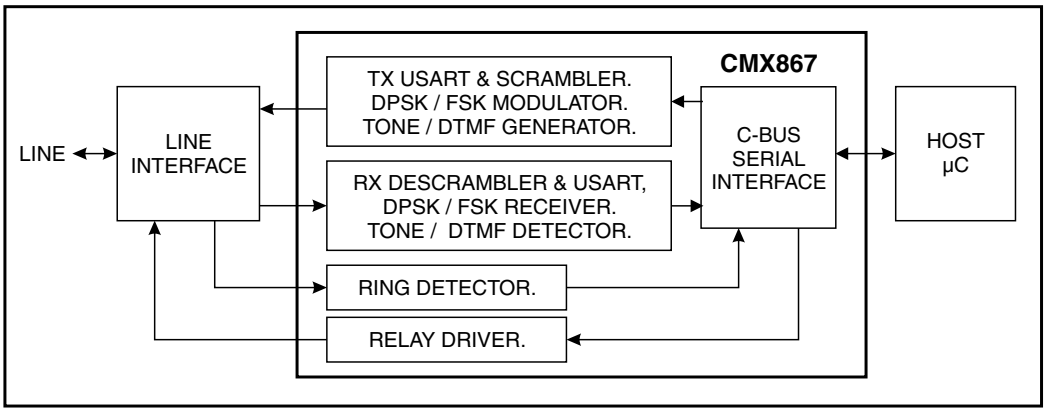
ADVANCE INFORMATION

Features

- **V.22, Bell 212A 1200/1200 or 600/600bps DPSK**
- **V.23 1200/75, 1200/1200, 75, 1200bps FSK**
- **Bell 202 1200/150, 1200/1200, 150, 1200bps FSK**
- **V.21 or Bell 103 300/300bps FSK**
- **DTMF/Tones Transmit and Receive**
- **Extremely Low Power: 3.5mA/3V, 6.5mA/5V typ.**
- **Powersave Standby Mode**
- **Upward Compatible to CMX868 2400bps V.22bis Modem**

Applications

- **Phone Line Powered Devices**
- **Payphones**
- **Remote Utility Meter Reading**
- **POS Terminals**
- **Cable TV Set Top Box (STB)**
- **Telephone Telemetry Systems**
- **Security Systems**
- **Industrial Control Systems**
- **Modem Links with Caller ID**



The CMX867 is a multi-standard modem for use in telephone based information and telemetry systems.

Control of the device is via a simple high speed serial bus, compatible with most types of µC serial interfaces. The data transmitted and received by the modem is also transferred over the same serial bus. On-chip programmable Tx and Rx USARTs meeting the requirements of V.14 are provided for use with asynchronous data and allow unformatted synchronous data to be received or transmitted as 8-bit words.

The CMX867 can transmit and detect standard DTMF and modem calling and answer signals or user-specific programmed single or dual tone signals. A general purpose Call Progress signal detector is also included.

Flexible line driver and receive hybrid circuits are integrated on chip, requiring only passive external components to create a 2 or 4-wire line interface.

The device also features a Hook Switch Relay Drive output and a Ring Detector circuit which continues to function when the device is in the Powersave mode, providing an interrupt which can be used to wake up the host µController when line voltage reversal or ringing is detected.

The CMX867 operates from a single 2.7 to 5.5V supply over a temperature range of -40°C to +85°C and is available in 24-pin TSSOP, SOIC and DIP packages.

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1 Block Diagram

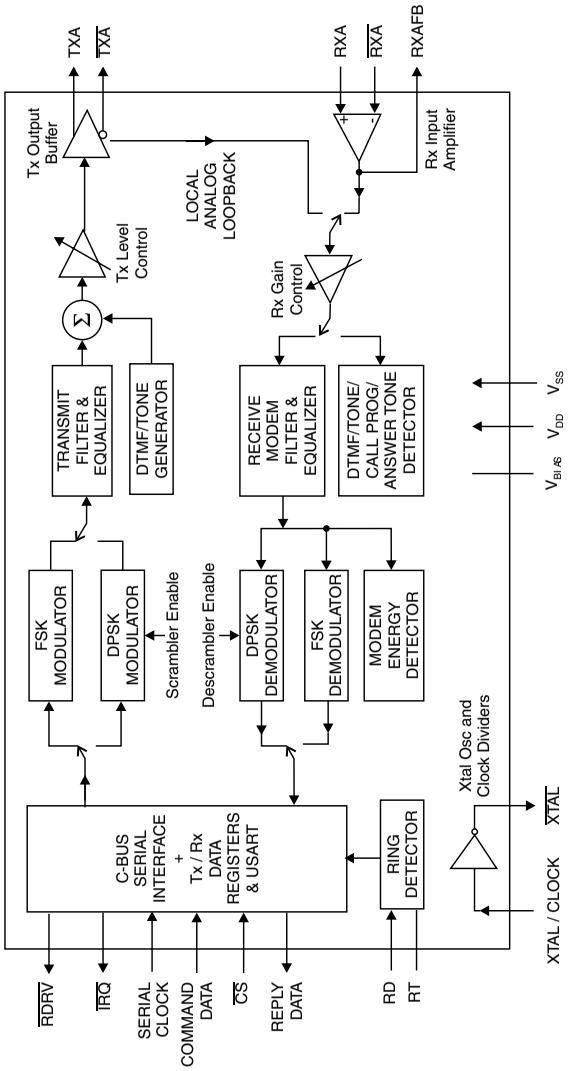


Figure 1: Block Diagram

2 Signal List

D2/E2/P4	Signal		Description
Pin No.	Name	Type	
1	$\overline{XTAL}$	output	The output of the on-chip Xtal oscillator inverter.
2	XTAL/CLOCK	input	The input to the oscillator inverter from the Xtal circuit or external clock source.
3	$\overline{RDRV}$	output	Relay drive output, low resistance pull down to V_{SS} when active and medium resistance pull up to V_{DD} when inactive.
4, 8, 12, 17, 21	V_{SS}	Power	The negative supply rail (ground).
5	RD	input	Schmitt trigger input to the Ring signal detector. Connect to V_{SS} if Ring Detector not used.
6	RT	bi-directional	Open drain output and Schmitt trigger input forming part of the Ring signal detector. Connect to V_{DD} if Ring Detector not used.
7, 16, 24	V_{DD}	Power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage.
9	RXAFB	output	The output of the Rx Input Amplifier.
10	$\overline{RXA}$	input	The inverting input to the Rx Input Amplifier
11	RXA	input	The non-inverting input to the Rx Input Amplifier
13	V_{BIAS}	output	Internally generated bias voltage of approximately $V_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to V_{SS}. Should be de-coupled to V_{SS} by a capacitor mounted close to the device pins.
14	$\overline{TXA}$	output	The inverted output of the Tx Output Buffer.
15	TXA	output	The non-inverted output of the Tx Output Buffer.
18	$\overline{CS}$	input	The C-BUS chip select input from the µC.
19	COMMAND DATA	input	The C-BUS serial data input from the µC.
20	SERIAL CLOCK	input	The C-BUS serial clock input from the µC.
22	REPLY DATA	tri-state	A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
23	$\overline{IRQ}$	output	A 'wire-ORable' output for connection to a µC Interrupt Request input. This output is pulled down to V_{SS} when active and is high impedance when inactive. An external pull-up resistor is required i.e. R1 of Figure 2.

Table 1: Signal List

3 External Components

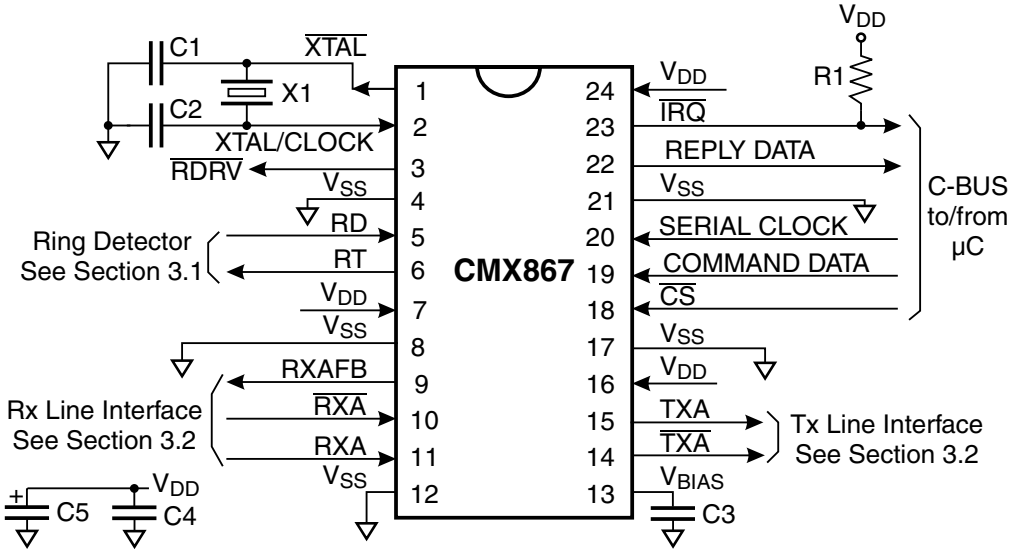


Figure 2: Recommended External Components for Typical Applciation

R1	100kΩ		C5	10uF
C1, C2	22pF		X1	11.0592MHz or 12.288MHz
C3, C4	100nF			

Resistors ±5%, capacitors ±20% unless otherwise stated.

Table 2: Recommended External Components for typical Application

Note:

1. This device is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} and V_{BIAS} should be decoupled and the receive path protected from extraneous in-band signals. It is recommended that the printed circuit board be laid out with a V_{SS} ground plane in the CMX867 area to provide a low impedance connection between the V_{SS} pins and the V_{DD} and V_{BIAS} decoupling capacitors. The V_{SS} connections to the Xtal oscillator capacitors C1 and C2 should also be low impedance and preferably be part of the V_{SS} ground plane to ensure reliable start up of the oscillator.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult your crystal manufacturer.

3.1 Ring Detector Interface

Figure 3 shows how the CMX867 may be used to detect the large amplitude Ringing signal voltage present on the 2-wire line at the start of an incoming telephone call.

The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C20 and R20 or C21 and R21 to appear at the top end of R22 (point X in Figure 3) in a rectified and attenuated form.

The signal at point X is further attenuated by the potential divider formed by R22 and R23 before being applied to the CMX867 RD input. If the amplitude of the signal appearing at RD is greater than the input threshold (Vt_{HI}) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C22. The output of the Schmitt trigger 'B' will then go high, setting bit 14 (Ring Detect) of the Status Register.

The minimum amplitude ringing signal that is certain to be detected is:

$$\left(0.7 + Vt_{HI}\frac{(R20 + R22 + R23)}{R23}\right)(0.707V_{RMS})$$

where Vt_{HI} is the high-going threshold voltage of the Schmitt trigger A (see Section 6.1).

With R20-22 all 470kΩ as Figure 3, then setting R23 to 68kΩ will guarantee detection of ringing signals of $40V_{RMS}$ and above for V_{DD} over the range 3 to 5V.

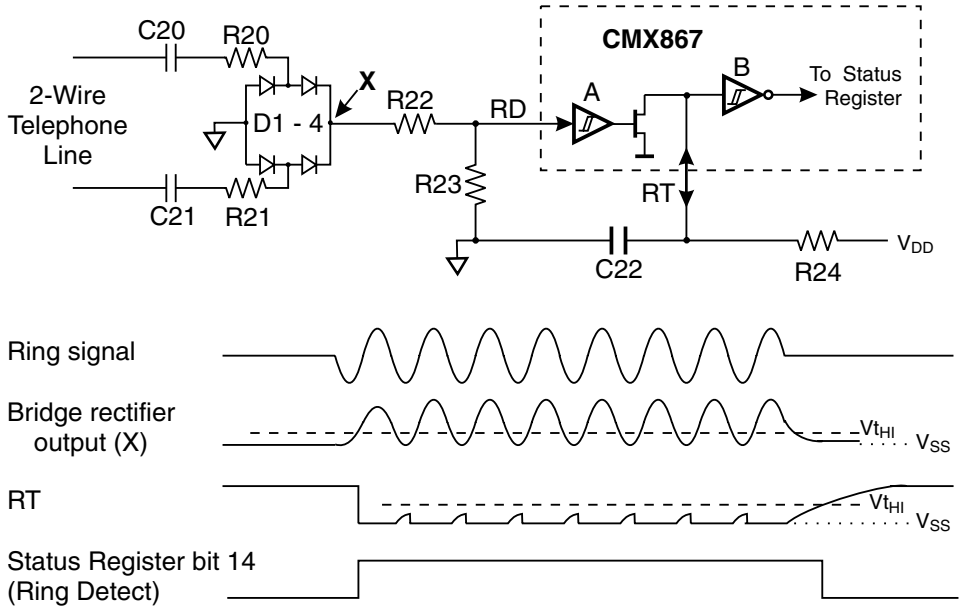


Figure 3: Ring Signal Interface Circuit

R20, 21, 22	470kΩ		C20, 21	0.1µF
R23	See text		C22	0.33µF
R24	470kΩ		D1-4	1N4004

Resistors ±5%, capacitors ±20%

Table 3: Ring Signal Detector Interface Circuit External Components

If the time constant of R24 and C22 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger for the duration of a ring cycle.

The time for the voltage on RT to charge from V_{SS} towards V_{DD} can be derived from the formula

$$V_{RT} = V_{DD}\left[1 - e^{\left(\frac{-t}{R24 \times C22}\right)}\right]$$

As the Schmitt trigger high-going input threshold voltage (Vt_{HI}) has a minimum value of 0.56 x V_{DD}, then the Schmitt trigger B output will remain high for a time of at least 0.821 x R24 x C22 following a pulse at RD.

The values of R24 and C22 given in Figure 3 (470kΩ and 0.33µF) give a minimum RT charge time of 100ms, which is adequate for ring frequencies of 10Hz or above.

Note: The circuit will also respond to a telephone line voltage reversal. If necessary the µC can distinguish between a Ring signal and a line voltage reversal by measuring the time that bit 14 of the Status Register (Ring Detect) is high.

If the Ring detect function is not used then pin RD should be connected to V_{SS} and RT to V_{DD}.

3.2 Line Interface

A line interface circuit is needed to provide dc isolation and to terminate the line.

3.2.1 2-Wire Line Interface

Figure 4 shows an interface for use with a 600Ω 2-wire line. The complex line termination is provided by R13 and C10, high frequency noise is attenuated by C10 and C11, while R11 and R12 set the receive signal level into the modem. For clarity, 2-wire line protection circuits have not been shown.

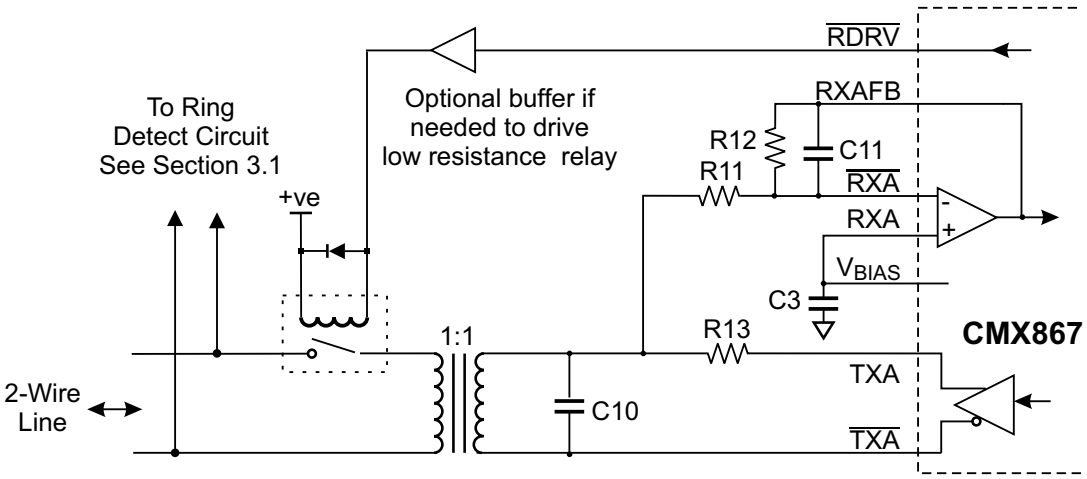


Figure 4: 2-Wireline Interface Circuit

R11	See text		C3	See Figure 2
R12	100kΩ		C10	33nF
R13	600Ω		C11	100pF

Resistors ±5%, capacitors ±20%

Table 4: 2-Wireline Interface Circuit External Components

The transmit line signal level is determined by the voltage swing between the TXA and $\overline{TXA}$ pins, less 6dB due to the line termination resistor R13, and less the loss in the line coupling transformer.

Allowing for 1dB loss in the transformer, then with the Tx Mode Register set for a Tx Level Control gain of 0dB the nominal transmit line levels will be:

	V_{DD} = 3.0V	V_{DD} = 5.0V
DPSK and FSK Tx modes (no guard tone)	-10dBm	-5.5dBm
Single tone transmit mode	-10dBm	-5.5dBm
DTMF transmit mode	-6 and -8 dBm	-1.5 and -3.5 dBm

For a line impedance of 600Ω, 0dBm = 775mV_{RMS}. See also Section 6.1.3.

In the receive direction, the signal detection thresholds within the CMX867 are proportional to V_{DD} and are affected by the Rx Gain Control gain setting in the Rx Mode Register. The signal level into the CMX867 is affected by the line coupling transformer loss and the values of R11 and R12 of Figure 4.

Assuming 1dB transformer loss, the Rx Gain Control programmed to 0dB and R12 = 100kΩ, then for correct operation (see Section 6.1.3) the value of R11 should be equal to 500 / V_{DD} kΩ i.e. 160kΩ at 3.0V, falling to 100kΩ at 5.0V

3.2.2 4-Wire Line Interface

Figure 5 shows an interface for use with a 600Ω 4-wire line. The line terminations are provided by R10 and R13, high frequency noise is attenuated by C11 while R11 and R12 set the receive signal level into the modem.

Transmit and receive line level settings and the value of R11 are as for the 2-wire circuit.

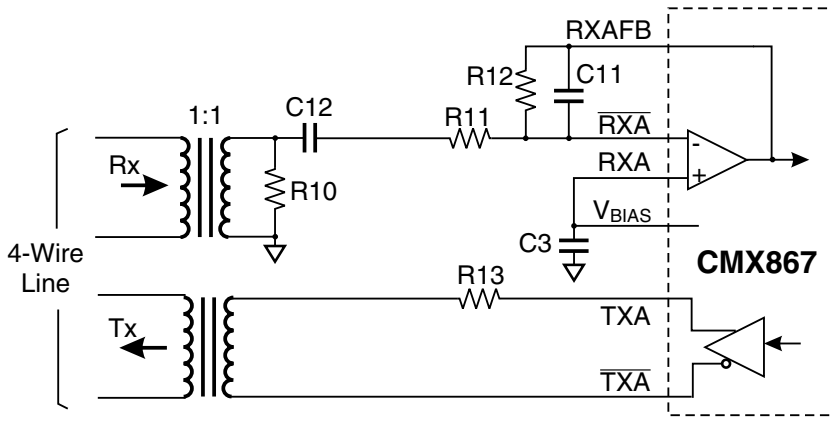


Figure 5: 4-Wireline Interface Circuit

R10, 13	600Ω	1	C3	See Figure 2
R11	See text		C11	100pF
R12	100kΩ		C12	33nF

Resistors ±5%, capacitors ±20%

Table 5: 4-Wireline Interface Circuit External Components

4 General Description

The CMX867 transmit and receive operating modes are independently programmable.

The transmit mode can be set to any one of the following:

- V.22 and Bell 212A modem. 1200 or 600bps DPSK (Differential Phase Shift Keying).
- V.21 modem. 300bps FSK (Frequency Shift Keying).
- Bell 103 modem. 300bps FSK.
- V.23 modem. 1200 or 75bps FSK.
- Bell 202 modem. 1200 or 150bps FSK.
- DTMF transmit.
- Single tone transmit (from a range of modem calling, answer and other tone frequencies)
- User programmed tone or tone pair transmit (programmable frequencies and levels)
- Disabled.

The receive mode can be set to any one of the following:

- V.22 and Bell 212A modem. 1200 or 600bps DPSK.
- V.21 modem. 300bps FSK.
- Bell 103 modem. 300bps FSK.
- V.23 modem. 1200 or 75bps FSK.
- Bell 202 modem. 1200 or 150bps FSK.
- DTMF detect.
- 2100Hz and 2225Hz answer tone detect.
- Call progress signal detect.
- User programmed tone or tone pair detect.
- Disabled.

The CMX867 may also be set into a Powersave mode that disables all circuitry except for the C-BUS interface and the Ring Detector.

4.1 Tx USART

A flexible Tx USART is provided for all modem modes, meeting the requirements of V.14 for DPSK modems.

It can be programmed to transmit continuous patterns, Start-Stop characters or Synchronous Data.

In both Synchronous Data and Start-Stop modes the data to be transmitted is written by the µC into the 8-bit C-BUS Tx Data Register from which it is transferred to the Tx Data Buffer.

If Synchronous Data mode has been selected the 8 data bits in the Tx Data Buffer are transmitted serially, b0 being sent first.

In Start-Stop mode a single Start bit is transmitted, followed by 5, 6, 7 or 8 data bits from the Tx Data Buffer - b0 first - followed by an optional Parity bit then - normally - one or two Stop bits. The Start, Parity and Stop bits are generated by the USART as determined by the Tx Mode Register settings and are not taken from the Tx Data Register.

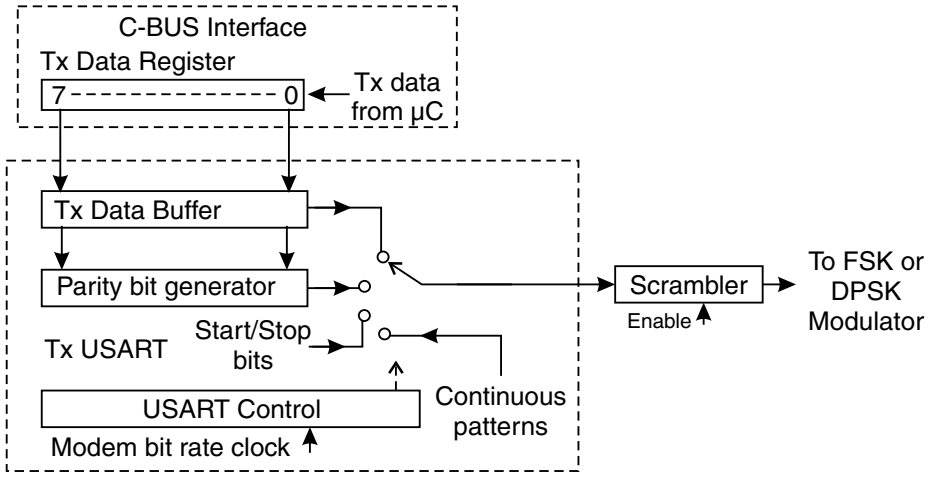


Figure 6: Tx USART

Every time the contents of the C-BUS Tx Data Register are transferred to the Tx Data Buffer the Tx Data Ready flag bit of the Status Register is set to 1 to indicate that a new value should be loaded into the C-BUS Tx Data Register. This flag bit is cleared to 0 when a new value is loaded into the Tx Data Register.

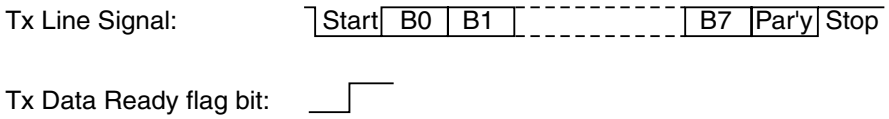


Figure 7: Tx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If a new value is not loaded into the Tx Data Register in time for the next Tx Data Register to Tx Data Buffer transfer then the Status Register Tx Data Underflow bit will be set to 1. In this event the contents of the Tx Data Buffer will be re-transmitted if Synchronous Data mode has been selected, or if the Tx modem is in Start-Stop mode then a continuous Stop signal (1) will be transmitted until a new value is loaded into the Tx Data Register.

In all modes the transmitted bit and baud rates are the nominal rates for the selected modem type, with an accuracy determined by the XTAL frequency accuracy, however for DPSK modes V.14 requires that Start-Stop characters can be transmitted at up to 1% overspeed (basic signaling rate range) or 2.3% overspeed (extended signaling rate range) by deleting a Stop bit from no more than one out of every 8 (basic range) or 4 (extended range) consecutive transmitted characters.

To accommodate the V.14 requirement the Tx Data Register has been given two C-BUS addresses, $E3 and $E4. Data should normally be written to $E3.

In DPSK Start-Stop modes if data is written to $E4 then the programmed number of Stop bits will be reduced by one for that character. In this way the µC can delete transmitted Stop bits as needed.

In FSK Start-Stop modes, data written to $E4 will be transmitted with a 12.5% reduction in the length of the Stop bit at the end of that character.

In all Synchronous Data modes data written to $E4 will be treated as though it had been written to $E3.

The underspeed transmission requirement of V.14 is automatically met by the CMX867. As in Start-Stop mode it automatically inserts extra Stop bit(s) if it has to wait for new data to be loaded into the C-BUS Tx Data Register.

The optional V.22 compatible data scrambler can be programmed to invert the next input bit in the event of 64 consecutive ones appearing at its input. It uses the generating polynomial:

$$1 + x^{-14} + x^{-17}$$

4.2 FSK and DPSK Modulators

Serial data from the USART is fed via the optional scrambler to the FSK modulator if V.21, V.23, Bell 103 or Bell 202 mode has been selected or to the DPSK modulator for V.22 and Bell 212A modes.

The FSK modulator generates one of two frequencies according to the transmit mode and the value of current transmit data bit.

The DPSK modulator generates a carrier of 1200Hz (Low Band, Calling modem) or 2400Hz (High Band, Answering modem) which is modulated at 600 symbols/sec as described below:

600bps V.22 signals are transmitted as a +90° carrier phase change for a '0' bit, +270° for '1'.

For V.22 and Bell 212A 1200bps DPSK the transmit data stream is divided into groups of two consecutive bits (dibits) which are encoded as a carrier phase change:

Dibit (left-hand bit is the first of the pair)	Phase change
00	+90°
01	0°
11	+270°
10	+180°

4.3 Tx Filter and Equalizer

The FSK or DPSK modulator output signal is fed through the Transmit Filter and Equalizer block which limits the out-of-band signal energy to acceptable limits. In 600 and 1200bps FSK and DPSK modes this block includes a fixed compromise line equalizer which is automatically set for the particular modulation type and frequency band being employed. This fixed compromise line equalizer may be enabled or disabled by bit 10 of the General Control Register. The amount of Tx equalization provided compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1 over the frequency band used.

4.4 DTMF/Tone Generator

In DTMF/Tones mode this block generates DTMF signals or single or dual frequency tones. In DPSK modem modes, it is used to generate the optional 550 or 1800Hz guard tone.

4.5 Tx Level Control and Output Buffer

The outputs (if present) of the Transmit Filter and DTMF/Tone Generator are summed then passed through the programmable Tx Level Control and Tx Output Buffer to the pins TXA and $\overline{\text{TXA}}$. The Tx Output Buffer has symmetrical outputs to provide sufficient line voltage swing at low values of V_{DD} and to reduce harmonic distortion of the signal.

4.6 Rx DTMF/Tones Detectors

In Rx Tones Detect mode the received signal, after passing through the Rx Gain Control block, is fed to the DTMF / Tones / Call Progress / Answer Tone detector. The user may select any of four separate detectors:

The DTMF detector detects standard DTMF signals. A valid DTMF signal will set bit 5 of the Status Register to 1 for as long as the signal is detected.

The programmable tone pair detector includes two separate tone detectors (see Figure 19). The first detector will set bit 6 of the Status Register for as long as a valid signal is detected, the second detector sets bit 7, and bit 10 of the Status Register will be set when both tones are detected.

The Call Progress detector measures the amplitude of the signal at the output of a 275 - 665Hz bandpass filter and sets bit 10 of the Status Register to 1 when the signal level exceeds the measurement threshold.

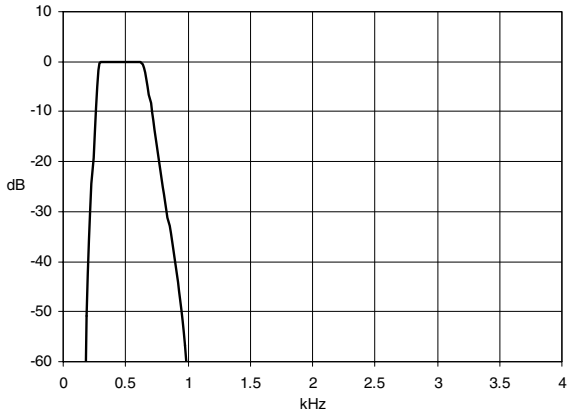


Figure 8: Response of Call Progress Filter

The Answer Tone detector measures both amplitude and frequency of the received signal and sets bit 6 or bit 7 of the Status Register when a valid 2225Hz or 2100Hz signal is received.

4.7 Rx Modem Filtering and Demodulation

When the receive part of the CMX867 is operating as a modem, the received signal is fed to a bandpass filter to attenuate unwanted signals and to provide fixed compromise line equalization for 600 and 1200bps FSK and DPSK modes. The characteristics of the bandpass filter and equalizer are determined by the chosen receive modem type and frequency band. The line equalizer may be enabled or disabled by bit 10 of the General Control Register and compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1.

The responses of these filters, including the line equalizer and the effect of external components used in Figure 4 and Figure 5, are shown in Figure 9, Figure 10, Figure 11, and Figure 12:

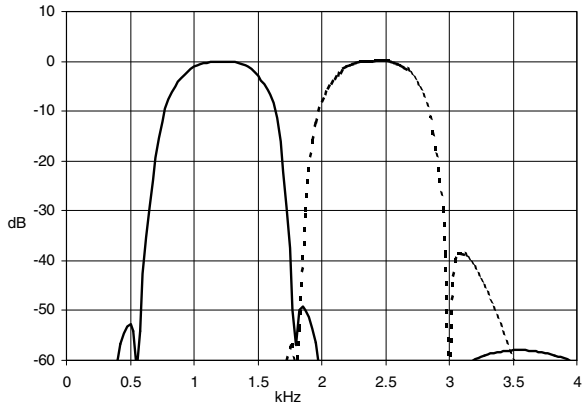


Figure 9: DPSK Rx Filters

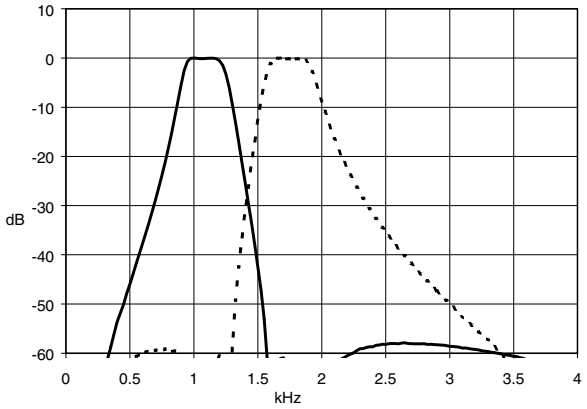


Figure 10: V.21 Rx Filters

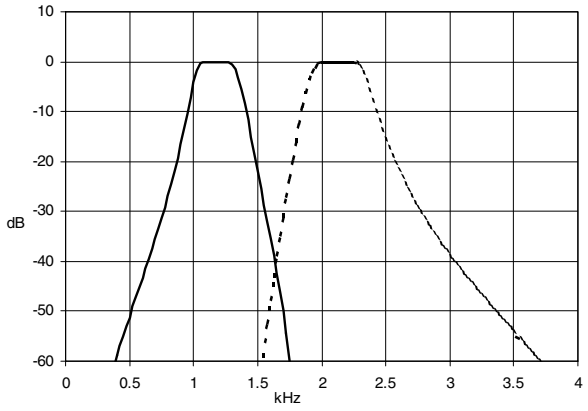


Figure 11: Bell 103 Rx Filters

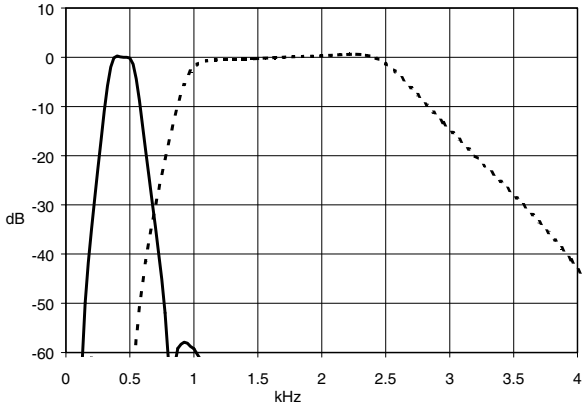


Figure 12: Bell 202 / V.23 Rx Filters

The signal level at the output of the Receive Modem Filter and Equalizer is measured in the Modem Energy Detector block, compared to a threshold value, and the result controls bit 10 of the Status Register.

The output of the Receive Modem Filter and Equalizer is also fed to the FSK or DPSK demodulator depending on the selected modem type.

The FSK demodulator recognizes individual frequencies as representing received ‘1’ or ‘0’ data bits:

The DPSK demodulator decodes DPSK modulation of a 1200Hz or 2400Hz carrier and is used for V.22 and Bell 212A modes. It includes an adaptive receive signal equalizer (auto-equalizer) that will automatically compensate for a wide range of line conditions in DPSK modes. The auto-equalizer can provide a useful improvement in performance in 600 or 1200bps DPSK modes so, although it must be disabled at the start of a handshake sequence, it can be enabled as soon as scrambled 1200bps 1s have been detected.

Both FSK and DPSK demodulators produce a serial data bit stream that is fed to the Rx pattern detector, descrambler and USART block. See Figure 13. The demodulator input is also monitored for continuous dibits ’00,11’ in 1200bps DPSK mode and continuous alternating 1s and 0s in all other modes.

The DPSK demodulator also estimates the received bit error rate by comparing the actual received signal against an ideal waveform. This estimate is placed in bits 2-0 of the Status Register. See Figure 18.

4.8 Rx Modem Pattern Detectors and Descrambler

Reference Figure 13.

The 1010.. pattern detector operates only in FSK modes and will set bit 9 of the Status Register when 32 bits of alternating 1’s and 0’s have been received.

The ‘Continuous Unscrambled 1’s’ detector operates in all modem modes and sets bits 8 and 7 of the Status Register to ‘01’ when 32 consecutive 1’s have been received.

The descrambler operates only in DPSK modes and is enabled by setting bit 7 of the Rx Mode Register.

The ‘Continuous Scrambled 1’s’ detector operates only in DPSK modes when the descrambler is enabled and sets bits 8 and 7 of the Status Register to ‘11’ when 32 consecutive 1’s appear at the output of the descrambler. To avoid possible ambiguity, the ‘Scrambled 1’s’ detector is disabled when continuous unscrambled 1’s are detected.

The ‘Continuous 0’s’ detector sets bits 8 and 7 of the Status Register to ‘10’ when NX consecutive 0’s have been received, NX being 32 except when DPSK Start-Stop mode has been selected, in which case NX = 2N + 4 where N is the number of bits per character including the Start, Stop and any Parity bits.

All of these pattern detectors will hold the ‘detect’ output for 12 bit times after the end of the detected pattern unless the received bit rate or operating mode is changed, in which case the detectors are reset within 2ms.

4.9 Rx Data Register and USART

A flexible Rx USART is provided for all modem modes, meeting the requirements of V.14 for DPSK modems. It can be programmed to treat the received data bit stream as Synchronous data or as Start-Stop characters.

In Synchronous mode the received data bits are all fed into the Rx Data Buffer which is copied into the C-BUS Rx Data Register after every 8 bits.

In Start-Stop mode the USART Control logic looks for the start of each character, then feeds only the required number of data bits (not parity) into the Rx Data Buffer. The parity bit (if used) and the presence of a Stop bit are then checked and the data bits in the Rx Data Buffer copied to the C-BUS Rx Data Register.

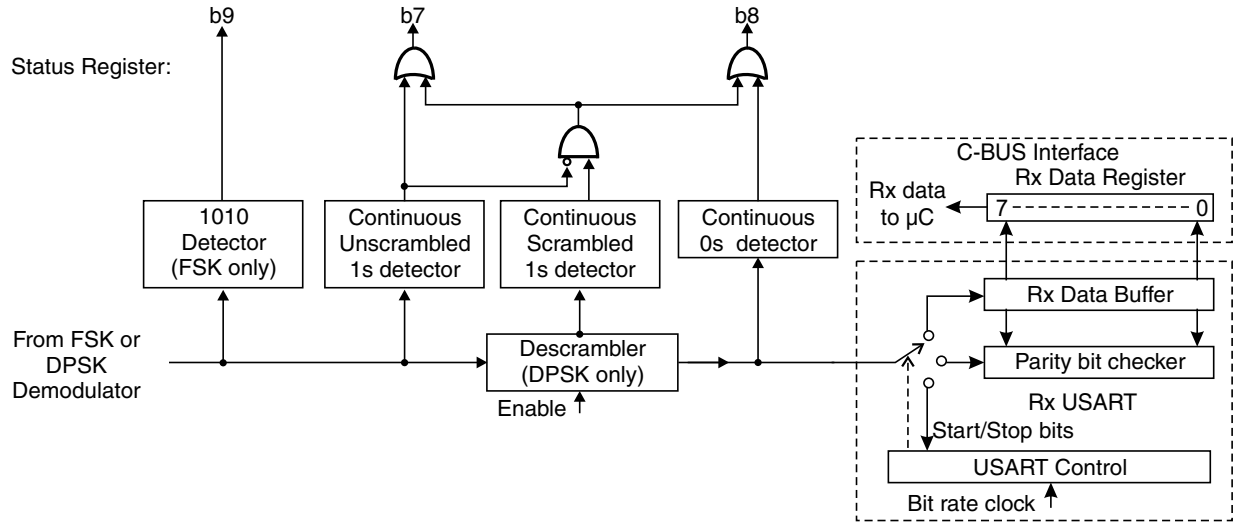


Figure 13: Rx Modem Data Paths

Whenever a new character is copied into the C-BUS Rx Data Register, the Rx Data Ready flag bit of the Status Register is set to '1' to prompt the µC to read the new data; and in Start-Stop mode, the Even Rx Parity flag bit of the Status Register is updated.

In Start-Stop mode, if the Stop bit is missing (received as a '0' instead of a '1') the received character will still be placed into the Rx Data Register and the Rx Data Ready flag bit set, but, unless allowed by the V.14 overspeed option described below, the Status Register Rx Framing Error bit will also be set to '1' and the USART will re-synchronize onto the next '1' – '0' (Stop – Start) transition. The Rx Framing Error bit will remain set until the next character has been received.

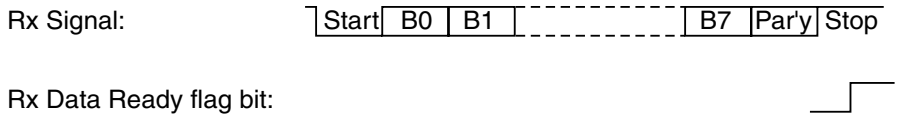


Figure 14: Rx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If the µC has not read the previous data from the Rx Data Register by the time that new data is copied to it from the Rx Data Buffer then the Rx Data Overflow flag bit of the Status Register will be set to 1.

The Rx Data Ready flag and Rx Data Overflow bits are cleared to 0 when the Rx Data Register is read by the µC.

For DPSK Start-Stop modes, V.14 requires that the receive USART be able to cope with missing Stop bits; up to 1 missing Stop bit in every 8 consecutive received characters being allowed for the +1% overspeed (basic signaling rate) V.14 mode and 1 in 4 for the +2.3% overspeed (extended signaling rate) mode.

To accommodate the requirements of V.14, the CMX867 Rx Mode Register can be set for 0, +1% or +2.3% overspeed operation in DPSK Start-Stop modes. Missing Stop bits beyond those allowed by the selected overspeed option will set the Rx Framing Error flag bit of the Status Register.

In order that received Break signals can be handled correctly in V.14 Rx overspeed mode, a received character which has all bits '0', including the Stop and any Parity bits, will always cause the Rx Framing Error bit to be set and the USART to re-synchronize onto the next '1' – '0' transition. Additionally the received Continuous 0s detector will respond when more than 2M + 3 consecutive '0's are received, where 'M' is the selected total number of bits per character including Stop and any Parity bits.

4.10 C-BUS Interface

This block provides for the transfer of data and control or status information between the CMX867's internal registers and the µC over the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the µC which may be followed by a one or more data byte(s) sent from the µC to be written into one of the CMX867's Write Only Registers, or a one or more byte(s) of data read out from one of the CMX867's Read Only Registers, as illustrated in Figure 15.

Data sent from the µC on the Command Data line is clocked into the CMX867 on the rising edge of the Serial Clock input. Reply Data sent from the CMX867 to the µC is valid when the Serial Clock is high. The $\overline{CS}$ line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general-purpose µC I/O pins controlled by a simple software routine. Figure 23 gives detailed C-BUS timing requirements.

The following C-BUS addresses and registers are used by the CMX867:

- General Reset Command (address only, no data). Address $01
- General Control Register, 16-bit write-only. Address $E0
- Transmit Mode Register, 16-bit write-only. Address $E1
- Receive Mode Register, 16-bit write-only. Address $E2
- Transmit Data Register, 8-bit write-only. Addresses $E3 and $E4
- Receive Data Register, 8-bit read-only. Address $E5
- Status Register, 16-bit read-only. Address $E6
- Programming Register, 16-bit write-only. Address $E8

Note: The C-BUS addresses $E9, $EA and $EB should not be accessed in normal operation.

4.10.1 General Reset Command (no data) C-BUS address $01

This command resets the device and clears all bits of the General Control, Transmit Mode and Receive Mode Registers and bits 15 and 13-0 of the Status Register.

Whenever power is applied to the CMX867 a General Reset command should be sent to the device, after which the General Control Register should be set as required.

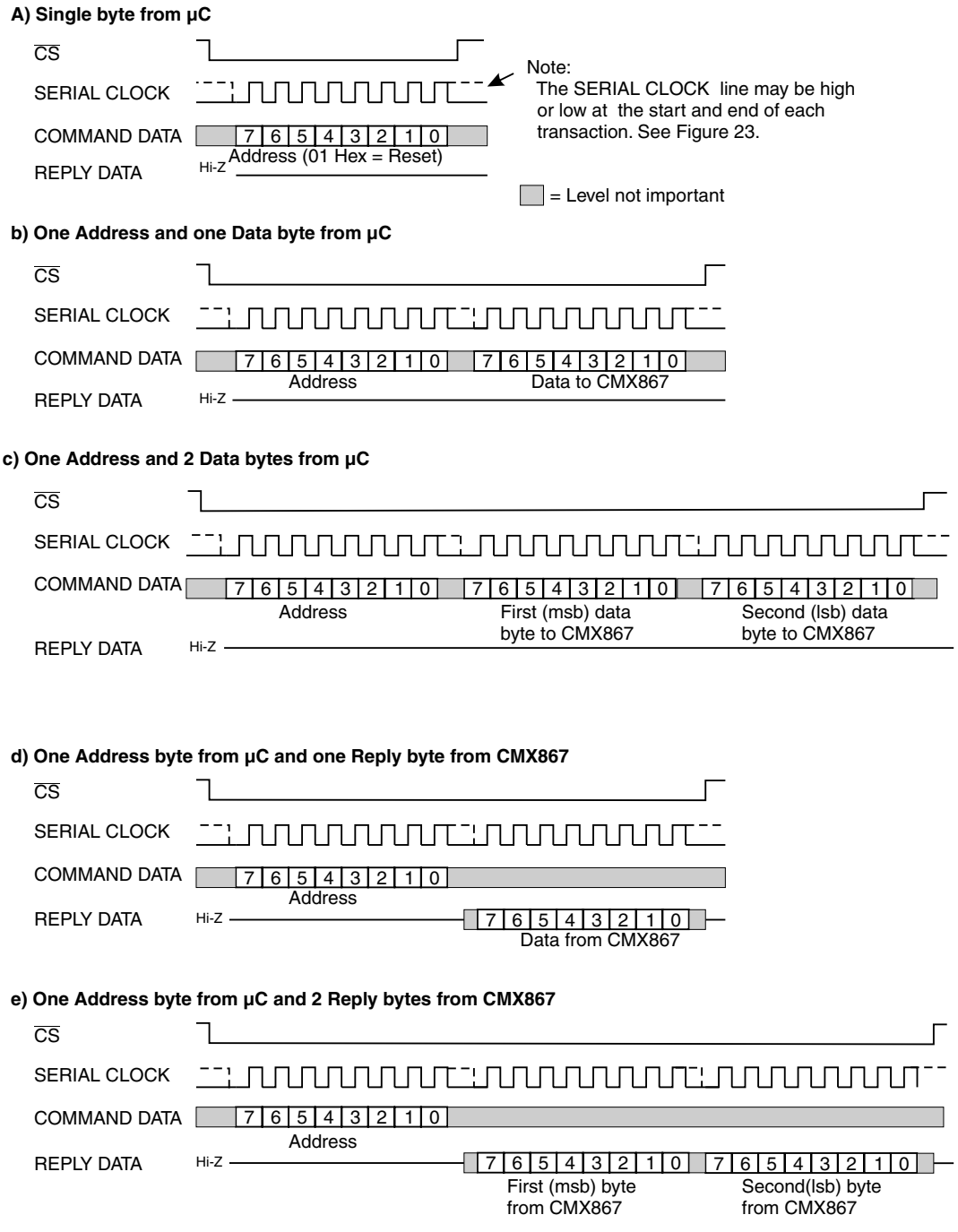


Figure 15: C-BUS Transactions

4.10.2 General Control Register: 16-bit write-only C-BUS address $E0

This register controls general features of the CMX867 such as the Powersave and Loopback modes, the IRQ mask bits and the Relay Drive output. It also allows the fixed compromise equalizers in the Tx and Rx signal paths to be disabled if desired, and sets the internal clock dividers to use either a 11.0592 or a 12.288 MHz XTAL frequency.

All bits of this register are cleared to 0 by a General Reset command.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	Xtal freq	LB	Equ	Rlydrv	Pwr	Rst	$\overline{\text{Irq}}$en	IRQ Mask Bits					

General Control Register b15-13: Reserved, set to 000

General Control Register b12: Xtal frequency

This bit should be set according to the Xtal frequency.

b12 = 1	11.0592MHz
b12 = 0	12.2880MHz

General Control Register b11: Analog Loopback test mode

This bit controls the analogue loopback test mode. Note that in loopback test mode both Transmit and Receive Mode Registers should be set to the same modem type and band or bit rate.

b11 = 1	Local analog loopback mode enabled
b11 = 0	No loopback (normal modem operation)

General Control Register b10: Tx and Rx Fixed Compromise Equalizers

This bit allows the Tx and Rx fixed compromise equalizers in the modem transmit and receive filter blocks to be disabled.

b10 = 1	Disable equalizers
b10 = 0	Enable equalizers (600 or 1200bps modem modes)

General Control Register b9: Relay Drive

This bit directly controls the $\overline{\text{RDRV}}$ output pin.

b9 = 1	$\overline{\text{RDRV}}$ output pin pulled to V_{SS}
b9 = 0	$\overline{\text{RDRV}}$ output pin pulled to V_{DD}

General Control Register b8: Power-up

This bit controls the internal power supply to most of the internal circuits, including the Xtal oscillator and V_{BIAS} supply. Note that the General Reset command clears this bit, putting the device into Powersave mode.

When the device is switched from Powersave mode to normal operation by setting the Powerup bit to 1, about 20ms should be allowed for the internal circuits, Xtal oscillator and V_{BIAS} to stabilize before starting to use the transmitter or receiver.

Changing the Powerup bit from 0 to 1 clears all bits of the Transmit Mode and Receive Mode Registers and clears b15 and b13-0 of the Status Register.

b8 = 1	Device powered up normally
b8 = 0	Powersave mode (all circuits except Ring Detect, $\overline{\text{RDRV}}$ and C-BUS interface disabled)

General Control Register b7: Reset

Setting this bit to 1 resets the CMX867's internal circuitry, clearing all bits of the Transmit and Receive Mode Registers and b15 and b13-0 of the Status Register.

b7 = 1	Internal circuitry in a reset condition.
b7 = 0	Normal operation

General Control Register b6: $\overline{\text{IRQ}}$ EN ($\overline{\text{IRQ}}$ Output Enable)

Setting this bit to 1 enables the $\overline{\text{IRQ}}$ output pin.

b6 = 1	$\overline{\text{IRQ}}$ pin driven low (to V_{SS}) if the IRQ bit of the Status Register = 1
b6 = 0	$\overline{\text{IRQ}}$ pin disabled (high impedance)

General Control Register b5-0: IRQ Mask bits

These bits affect the operation of the IRQ bit of the Status Register as described in Section 4.10.7.

4.10.3 Transmit Mode Register: 16-bit write-only C-BUS address $E1

This register controls the CMX867 transmit signal type and level. All bits of this register are cleared to 0 by a General Reset command, in Powersave mode, or when Bit 7 (Reset) of the General Control Register is 1.

Bit:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx mode = modem				Tx level			Guard tone		Scrambler		Start-stop / synch data		# data bits / synch data source		
Tx mode = DTMF/Tones				Tx level			Unused, set to 0000				DTMF or Tone select				
Tx mode = Disabled				Set to 0000 0000 0000											

Tx Mode Register Bits 15-12: Tx mode

These 4 bits select the transmit operating mode.

b15	b14	b13	b12		
1	1	1	1	Transmitter disabled	(Reserved for future use)
1	1	1	0	Transmitter disabled	(Reserved for future use)
1	1	0	1	V.22/Bell 212A 1200bps DPSK	High band (Answering modem)
1	1	0	0	"	Low band (Calling modem)
1	0	1	1	V.22 600bps DPSK	High band (Answering modem)
1	0	1	0	"	Low band (Calling modem)
1	0	0	1	V.21 300bps FSK	High band (Answering modem)
1	0	0	0	"	Low band (Calling modem)
0	1	1	1	Bell 103 300bps FSK	High band (Answering modem)
0	1	1	0	"	Low band (Calling modem)
0	1	0	1	V.23 FSK	1200bps
0	1	0	0	"	75bps
0	0	1	1	Bell 202 FSK	1200bps
0	0	1	0	"	150bps
0	0	0	1	DTMF / Tones	
0	0	0	0	Transmitter disabled	

Tx Mode Register Bits 11-9: Tx level

These 3 bits set the gain of the Tx Level Control block.

Bit 11	Bit 10	Bit 9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Tx Mode Register b8-7: Tx Guard tone (DPSK modes)

These 2 bits select the guard tone to be transmitted together with highband DPSK. Set both bits to 0 in FSK modes.

Bit 8	Bit 7	
1	1	Tx 550Hz guard tone
1	0	Tx 1800Hz guard tone
0	x	No Tx guard tone

Tx Mode Register b6-5: Tx Scrambler (DPSK modes)

These 2 bits control the operation of the Tx scrambler used in DPSK modes. Set both bits to 0 in FSK modes.

Bit 6	Bit 5	
1	1	Scrambler enabled, 64 ones detect circuit enabled (normal use)
1	0	Scrambler enabled, 64 ones detect circuit disabled
0	x	Scrambler disabled

Tx Mode Register b4-3: Tx Data Format (DPSK and FSK modes)

These two bits select Synchronous or Start-stop mode and the addition of a parity bit to transmitted characters in Start-stop mode.

Bit 4	Bit 3	
1	1	Synchronous mode
1	0	Start-stop mode, no parity
0	1	Start-stop mode, even parity bit added to data bits
0	0	Start-stop mode, odd parity bit added to data bits

Tx Mode Register b2-0: Tx Data and Stop bits (DPSK and FSK: Start-Stop modes)

In Start-stop mode these three bits select the number of Tx data and stop bits.

b2	b1	b0	
1	1	1	8 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
0	1	0	6 data bits, 1 stop bit
0	0	1	5 data bits, 2 stop bits
0	0	0	5 data bits, 1 stop bit

Tx Mode Register b2-0: Tx Data source (DPSK and FSK: Synchronous mode)

In Synchronous mode (b4-3 = 11) these three bits select the source of the data fed to the Tx FSK or DPSK scrambler and modulator.

b2	b1	b0	
1	x	x	Data bytes from Tx Data Buffer
0	1	1	Continuous 1s
0	1	0	Continuous 0s
0	0	x	Continuous dibits '00,11' in 1200bps DPSK mode, continuous alternating 1s and 0s in all other modes.

Tx Mode Register b8-0: DTMF/Tones mode

If DTMF/Tones transmit mode has been selected (Tx Mode Register b15-12 = 0001) then b8-5 should be set to 0000 and b4-0 will select a DTMF signal or a fixed tone or one of four programmed tones or tone pairs for transmission.

b4 = 0: Tx fixed tone or programmed tone pair

Bit 3	Bit 2	Bit 1	Bit 0	Tone frequency (Hz)	
0	0	0	0	No tone	
0	0	0	1	697	
0	0	1	0	770	
0	0	1	1	852	
0	1	0	0	941	
0	1	0	1	1209	
0	1	1	0	1336	
0	1	1	1	1477	
1	0	0	0	1633	
1	0	0	1	1300	(Calling tone)
1	0	1	0	2100	(Answer tone)
1	0	1	1	2225	(Answer tone)
1	1	0	0	Tone pair TA	Programmed Tx tone or tone pair, see 1.5.10.8
1	1	0	1	Tone pair TB	“
1	1	1	0	Tone pair TC	“
1	1	1	1	Tone pair TD	“

b4 = 1: Tx DTMF

Bit 3	Bit 2	Bit 1	Bit 0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

4.10.4 Receive Mode Register

Receive Mode Register: 16-bit write-only. C-BUS address $E2

This register controls the CMX867 receive signal type and level.

All bits of this register are cleared to 0 by a General Reset command, in Powersave mode or when b7 (Reset) of the General Control Register is 1.

Bit:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rx mode = modem				Rx level			Eq	Descramble		Start-stop/Synch			No. of bits and parity		
Rx mode = Tones detect				Rx level			DTMF/Tones/Call Progress select								
Rx mode = Disabled				Set to 0000 0000 0000											

Rx Mode Register Bits 15-12: Rx mode

These 4 bits select the receive operating mode.

Bit 15	Bit 14	Bit 13	Bit 12		
1	1	1	1	Receiver disabled	(Reserved for future use)
1	1	1	0	Receiver disabled	(Reserved for future use)
1	1	0	1	V.22/Bell 212A 1200bps DPSK	High band (Calling modem)
1	1	0	0	“	Low band (Answering modem)
1	0	1	1	V.22 600bps DPSK	High band (Calling modem)
1	0	1	0	“	Low band (Answering modem)
1	0	0	1	V.21 300bps FSK	High band (Calling modem)
1	0	0	0	“	Low band (Answering modem)
0	1	1	1	Bell 103 300bps FSK	High band (Calling modem)
0	1	1	0	“	Low band (Answering modem)
0	1	0	1	V.23 FSK	1200bps
0	1	0	0	“	75bps
0	0	1	1	Bell 202 FSK	1200bps
0	0	1	0	“	150bps
0	0	0	1	DTMF, Programmed tone pair, Answer Tone, Call Progress detect	
0	0	0	0	Receiver disabled	

Rx Mode Register b11-9: Rx level

These three bits set the gain of the Rx Gain Control block.

Bit 11	Bit 10	Bit 9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Rx Mode Register b8: Rx Auto-equalize (DPSK modes)

This bit controls the operation of the receive DPSK auto-equalizer. Set to 0 in FSK modes.

Bit 8 = 1	Enable auto-equalizer
Bit 8 = 0	DPSK mode: Auto-equalizer disabled

Rx Mode Register b7-6: Rx Scrambler (DPSK modes)

These 2 bits control the operation of the Rx de-scrambler used in DPSK modes. Set both bits to 0 in FSK modes.

Bit 7	Bit 6	
1	1	De-scrambler enabled, 64 ones detect circuit enabled (normal use)
1	0	De-scrambler enabled, 64 ones detect circuit disabled
0	x	De-scrambler disabled

Rx Mode Register b5-3: Rx USART Setting (DPSK and FSK modes)

These three bits select the Rx USART operating mode. The 1% and 2.3% overspeed options apply to DPSK modes only.

b5	b4	b3	
1	1	1	Rx Synchronous mode
1	1	0	Rx Start-stop mode, no overspeed
1	0	1	Rx Start-stop mode, +1% overspeed (1 in 8 missing Stop bits allowed)
1	0	0	Rx Start-stop mode, +2.3% overspeed (1 in 4 missing Stop bits allowed)
0	x	x	Rx USART function disabled

Rx Mode Register b2-0: Rx Data bits and parity (DPSK and FSK: Start-Stop modes)

In Start-stop mode these three bits select the number of data bits (plus any parity bit) in each received character. These bits are ignored in Synchronous mode.

Bit 2	Bit 1	Bit 0	
1	1	1	8 data bits + parity
1	1	0	8 data bits
1	0	1	7 data bits + parity
1	0	0	7 data bits
0	1	1	6 data bits + parity
0	1	0	6 data bits
0	0	1	5 data bits + parity
0	0	0	5 data bits

Rx Mode Register b2-0: Tones Detect mode

In Tones Detect Mode (Rx Mode Register b15-12 = 0001) b8-3 should be set to 000000

Bits 2-0 select the detector type.

Bit 2	Bit 1	Bit 0	
1	0	0	Programmable Tone Pair Detect
0	1	1	Call Progress Detect
0	1	0	2100, 2225Hz Answer Tone Detect
0	0	1	DTMF Detect
0	0	0	Disabled

4.10.5 Tx Data Register

Tx Data Register: 8-bit write-only. C-BUS addresses $E3 and $E4

Bit:	7	6	5	4	3	2	1	0
	Data bits to be transmitted							

In Synchronous Tx data mode this register contains the next 8 data bits to be transmitted. Bit 0 is transmitted first.

In Tx Start-Stop mode the specified number of data bits will be transmitted from this register (b0 first). A Start bit, a Parity bit (if required) and Stop bit(s) will be added automatically.

This register should only be written to when the Tx Data Ready bit of the Status Register is 1.

C-BUS address $E3 should normally be used, $E4 is for implementing the V.14 overspeed transmission requirement in Start-Stop mode, see Section 4.1.

4.10.6 Rx Data Register

Rx Data Register: 8-bit read-only. C-BUS address $E5

Bit:	7	6	5	4	3	2	1	0
	Received data bits							

In unformatted Rx data mode this register contains 8 received data bits, b0 of the register holding the earliest received bit, b7 the latest.

In Rx Start-Stop data mode this register contains the specified number of data bits from a received character, b0 holding the first received bit.

4.10.7 Status Register: 16-bit read-only C-BUS address $E6

Bits 15 and 13-0 of this register are cleared to 0 by a General Reset command, in Powersave mode, or when b7 (Reset) of the General Control Register is 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ	RD	PF	See below for uses of these bits												

The meanings of the Status Register bits 12-0 depend on whether the receive circuitry is in Modem or Tones Detect mode.

Status Register bits:			
	Rx Modem modes	**Rx Tones Detect modes**	**** IRQ Mask bit**
Bit 15	IRQ		
Bit 14	Set to 1 on Ring Detect		Bit 5
Bit 13	Programming Flag bit. See 1.5.10.8		Bit 4
Bit 12	Set to 1 on Tx data ready. Cleared by write to Tx Data Register		Bit 3
Bit 11	Set to 1 on Tx data underflow. Cleared by write to Tx Data Register		Bit 3
Bit 10	1 when energy is detected in Rx modem signal band	1 when energy is detected in Call Progress band or when both programmable tones are detected	Bit 2
b9	1 when double DPSK dibit 00,11 is detected in 1200bps DPSK mode, or when '1010..' pattern is detected in all other modes	0	b1
b8	See following table	0	b1
b7	See following table	1 when 2100Hz answer tone or the second programmable tone is detected	b1
b6	Set to 1 on Rx data ready. Cleared by read from Rx Data Register	1 when 2225Hz answer tone or the first programmable tone is detected	b0
b5	Set to 1 on Rx data overflow. Cleared by read from Rx Data Register	1 when DTMFcode is detected	b0
b4	Set to 1 on Rx framing error	0	-
b3	Set to 1 on even Rx parity	Rx DTMF code b3, see table	-
b2	DPSK Rx signal quality b2	Rx DTMF code b2	-
b1	DPSK Rx signal quality b1	Rx DTMF code b1	-
b0	DPSK Rx signal quality b0 or FSK frequency demodulator output	Rx DTMF code b0	-

Notes:

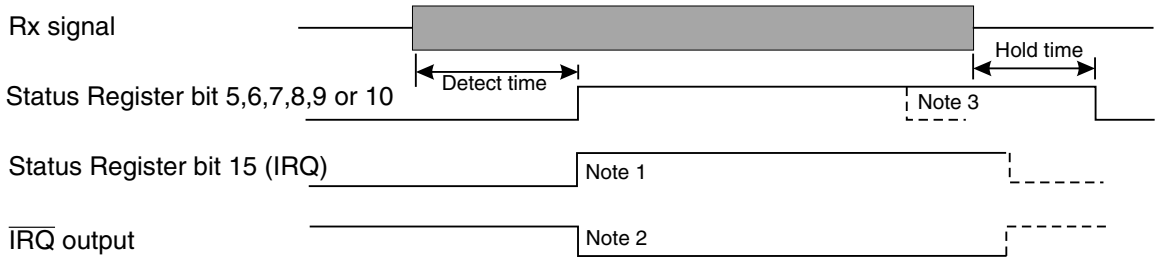
** This column shows the corresponding IRQ Mask bits in the General Control Register. A 0 to 1 transition on any of the Status Register bits 14-5 will cause the IRQ bit b15 to be set to 1 if the corresponding IRQ Mask bit is 1. The IRQ bit is cleared by a read of the Status Register or a General Reset command or by setting b7 or b8 of the General Control Register to 1.

The operation of the data demodulator and pattern detector circuits within the CMX867 does not depend on the state of the Rx energy detect function.

Decoding of Status Register b8,7 in Rx Modem Modes, see also Figure 13.

b8	b7	De-scrambler disabled	De-scrambler enabled (DPSK modes only)
1	1	-	Scrambled 1s
1	0	Unscrambled 0s	Scrambled 0s
0	1	Unscrambled 1s	Unscrambled 1s
0	0	-	-

When the descrambler is enabled then detection of continuous unscrambled 1s will inhibit the continuous scrambled 1s detector.



Notes:
1. IRQ will go high only if appropriate IRQ Mask bit in General Control Register is set. The IRQ bit is cleared by a read of the Status Register.
2. $\overline{IRQ}$ output will go low when IRQ bit high if $\overline{IRQ}$EN bit of General Control Register is set
3. In Rx Modem modes Status Register bits 5 and 6 are set by a Rx Data Ready or Rx Data Underflow event and cleared by a read of the Rx Data Register

Figure 16: Operation of Status Register bits 5-10

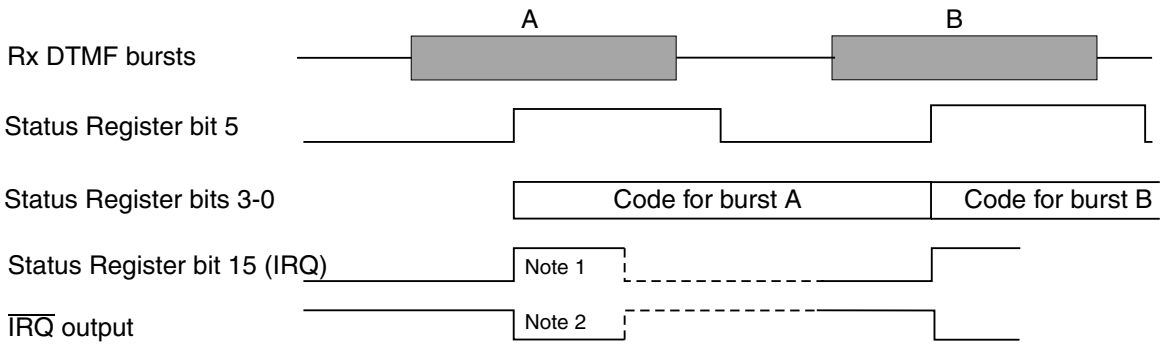
The $\overline{IRQ}$ output pin will be pulled low (to V_{SS}) when the IRQ bit of the Status Register and the $\overline{IRQ}$EN bit (b6) of the General Control Register are both 1.

Changes to Status Register bits caused by a change of Tx or Rx operating mode can take up to 150µs to take effect.

In Powersave mode or when the Reset bit (b7) of the General Control Register is 1 the Ring Detect bit (b14) continues to operate but all other bits will be 0.

The 'continuous 0' and 'continuous 1' detectors monitor the Rx signal after the DPSK descrambler, (see Figure 13) and hence will detect continuous 1s or 0s if the descrambler is disabled, or continuous scrambled 1s or 0s if the descrambler is enabled.

In DPSK Rx modem modes b2-0 of the Status Register contain a value indicative of the received signal BER, see Figure 18. In Rx FSK modem modes bits 2 and 1 will be zero and b0 will show the output of the frequency demodulator, updated at 8 times the nominal data rate.



Notes: 1. IRQ will go high only if the IRQ Mask bit b0 in the General Control Register is set. The IRQ bit is cleared by a read of the Status Register.
2. $\overline{IRQ}$ output will go low when IRQ bit high if $\overline{IRQ}$EN bit of General Control Register is set

Figure 17: Operation of Status Register in DTMF Rx Mode

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

Table 6: Received DTMF Code: b3-0 of Status Register

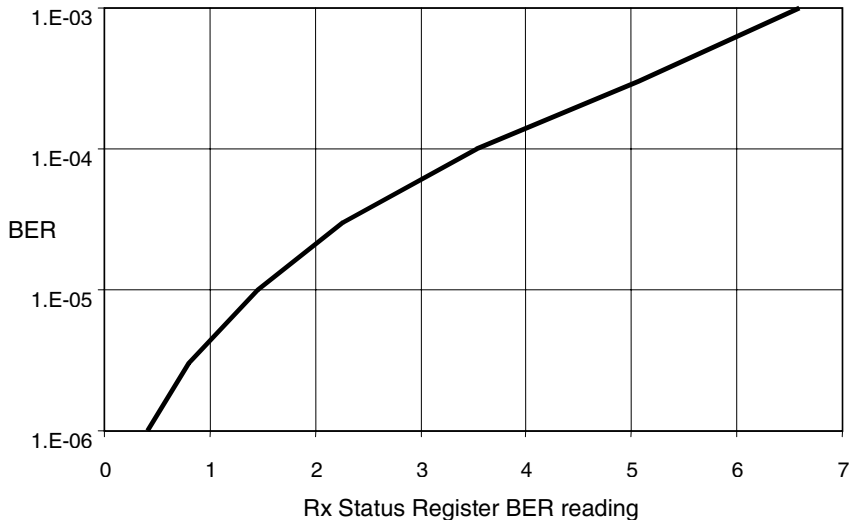


Figure 18: Typical Rx BER vs. Average Status Register BER Reading (b2-0)

4.10.8 Programming Register

Programming Register : 16-bit write-only. C-BUS address $E8

This register is used to program the transmit and receive programmed tone pairs by writing appropriate values to RAM locations within the CMX867. Note that these RAM locations are cleared by Powersave or Reset.

The Programming Register should only be written to when the Programming Flag bit (b13) of the Status Register is 1. The act of writing to the Programming Register clears the Programming Flag bit. When the programming action has been completed (normally within 150µs) the CMX867 will set the bit back to 1.

When programming Transmit or Receive Tone Pairs, do not change the Transmit or Receive Mode Registers until programming is complete and the Programming Flag bit has returned to 1.

Transmit Tone Pair Programming

4 transmit tone pairs (TA to TD) can be programmed.

The frequency (max 3.4kHz) and level must be entered for each tone to be used.

Single tones are programmed by setting both level and frequency values to zero for one of the pair.

Programming is done by writing a sequence of up to seventeen 16-bit words to the Programming Register.

The first word should be 32768 (8000 hex), the following 16-bit words set the frequencies and levels and are in the range 0 to 16383 (0-3FFF hex)

Word	Tone Pair	Value written
1		32768
2	TA	Tone 1 frequency
3	TA	Tone 1 level
4	TA	Tone 2 frequency
5	TA	Tone 2 level
6	TB	Tone 1 frequency
7	TB	Tone 1 level
- - -	- - -	- - - - - - - - - -
- - -	- - -	- - - - - - - - - -
16	TD	Tone 2 frequency
17	TD	Tone 2 level

The Frequency values to be entered are calculated from the formula:

$$\text{Value to be entered} = \text{desired frequency (Hz)} \times 3.414$$

i.e. for 1kHz the value to be entered is 3414 (or 0D56 in Hex).

The Level values to be entered are calculated from the formula:

$$\text{Value to be entered} = \frac{\text{desired } V_{RMS} \times 93780}{V_{DD}}$$

i.e. for $0.5V_{RMS}$ at V_{DD} = 3.0V, the value to be entered is 15630 (3D0E in Hex)

Note that allowance should be made for the transmit signal filtering in the CMX867 which attenuates the output signal for frequencies above 2kHz by 0.25dB at 2.5kHz, by 1dB at 3kHz and by 2.2dB at 3.4kHz.

On power-up or after a reset, the tone pairs TA-TC are set to notone, and TD is set to generate 2130Hz + 2750Hz at approximately –20dBm each.

Receive Tone Pair Programming

The programmable tone pair detector is implemented as shown in Figure 19. The filters are 4th order IIR sections. The frequency detectors measure the time taken for a programmable number of complete input signal cycles and compare this time against programmable upper and lower limits.

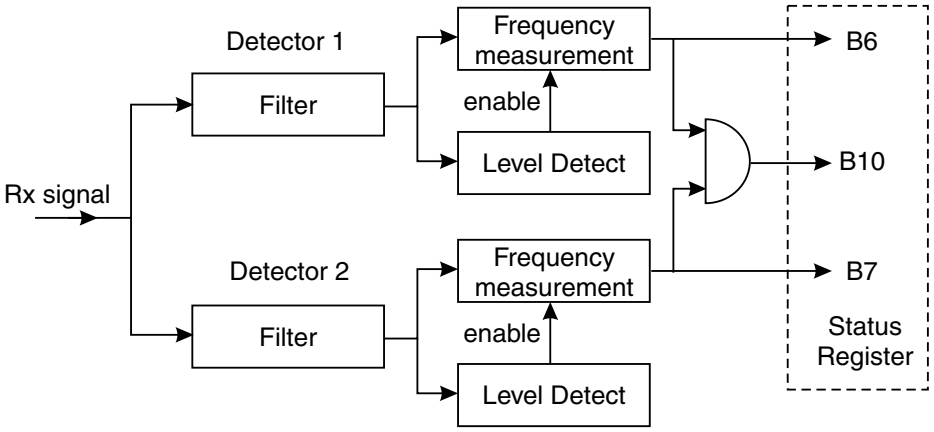


Figure 19: Programmable Tone Detectors

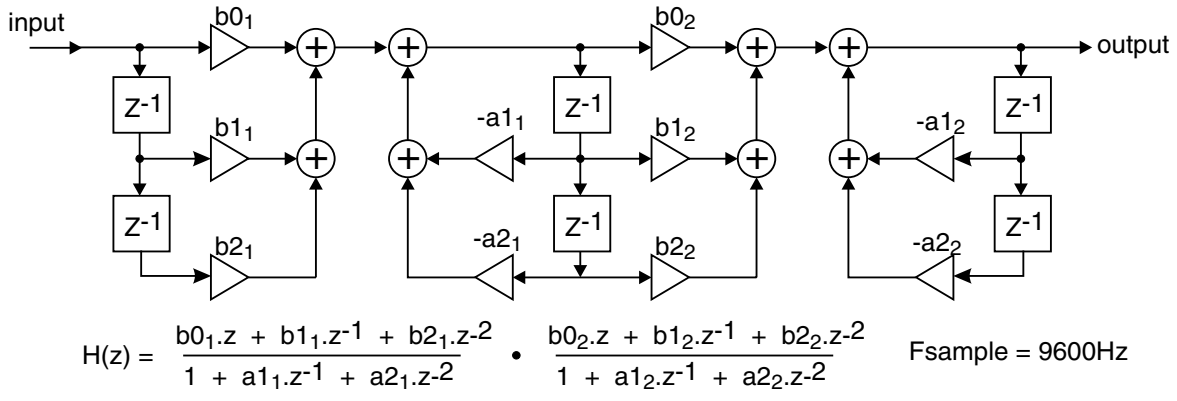


Figure 20: Filter Implementation

Programming is done by writing a sequence of twenty-seven 16-bit words to the Programming Register.

The first word should be 32769 (8001 hex), the following twenty-six 16-bit words set the frequencies and levels and are in the range 0 to 32767 (0000-7FFF hex).

Word	Value written	Word	Value written
1	32769		
2	Filter #1 coefficient $b2_1$	15	Filter #2 coefficient $b2_1$
3	Filter #1 coefficient $b1_1$	16	Filter #2 coefficient $b1_1$
4	Filter #1 coefficient $b0_1$	17	Filter #2 coefficient $b0_1$
5	Filter #1 coefficient $a2_1$	18	Filter #2 coefficient $a2_1$
6	Filter #1 coefficient $a1_1$	19	Filter #2 coefficient $a1_1$
7	Filter #1 coefficient $b2_2$	20	Filter #2 coefficient $b2_2$
8	Filter #1 coefficient $b1_2$	21	Filter #2 coefficient $b1_2$
9	Filter #1 coefficient $b0_2$	22	Filter #2 coefficient $b0_2$
10	Filter #1 coefficient $a2_2$	23	Filter #2 coefficient $a2_2$
11	Filter #1 coefficient $a1_2$	24	Filter #2 coefficient $a1_2$
12	Freq measurement #1 ncycles	25	Freq measurement #2 ncycles
13	Freq measurement #1 mintime	26	Freq measurement #2 mintime
14	Freq measurement #1 maxtime	27	Freq measurement #2 maxtime

The coefficients are entered as 15-bit signed (two's complement) integer values (the most significant bit of the 16-bit word entered should be zero) calculated as 8192 * coefficient value from the user's filter design program (i.e. this allows for filter design values of -1.9999 to +1.9999).

The design of the IIR filters should make allowance for the fixed receive signal filtering in the CMX867 which has a low pass characteristic above 1.5kHz of 0.4dB at 2kHz, 1.2dB at 2.5kHz, 2.6dB at 3kHz and 4.1dB at 3.4kHz.

'ncycles' is the number of signal cycles for the frequency measurement.

'mintime' is the smallest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'mintime' = 9600 * ncycles / high frequency limit

'maxtime' is the highest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'maxtime' = 9600 * ncycles / low frequency limit

The level detectors include hysteresis. The threshold levels - measured at the 2 or 4-wire line with unity gain filters, using the line interface circuits described in Section 3.2, 1.0 dB line coupling transformer loss and with the Rx Gain Control block set to 0dB - are nominally:

'Off' to 'On' -44.5dBm

'On' to 'Off' -47.0dBm

Note: If any changes are made to the programmed values while the CMX867 is running in Programmed Tone Detect mode they will not take effect until the CMX867 is next switched into Programmed Tone Detect mode.

On power-up or after a reset, the programmable tone pair detector is set to act as a simple 2130Hz + 2750Hz detector.

5 Application Notes

5.1 V.22 Calling Modem Application

This section describes how the CMX867 can be used in a V.22 Calling modem application, employing V.25 automatic answering and the V.22 recommended handshake sequence. This attempts to establish a 1200bps connection.

1. Ensure that the CMX867 is powered up. Set the Tx Mode Register to DTMF/Tones mode (set to 'No Tone' at this time), and the Rx Mode Register to Call Progress Detect mode.
2. Connect the line (go off hook) then dial the required number using the DTMF generator, monitoring for call progress signals (dial tone, busy, etc). Change to Answer Tone Detect mode.
3. On detection of the 2100Hz answer tone wait for it to end then wait for the 2225Hz answer tone detector to respond. (The '2225Hz' answer tone detector will recognize unscrambled binary 1s at 1200bps High Band as well as 2225Hz). When unscrambled binary 1s or 2225Hz have been received for 155ms set a 456ms timer.
4. When the 456ms timer expires check that the 2225Hz or unscrambled 1s is still being received, then set the Tx Mode Register for V.22 1200bps Low Band transmission of scrambled 1s (continuous 1s with the scrambler enabled). Also set the Rx Mode register to V.22 1200bps High Band receive, descrambler enabled and Rx USART disabled.
5. When scrambled 1s (at 1200bps) have been received for 270ms enable the Rx USART, set a 765ms timer and load the Tx Data Register with the first data to be transmitted.
6. When the timer expires set the Tx Mode Register for Start-Stop or Synchronous transmission of data from the Tx Data Buffer. This will start transmission of the data loaded in step 5.
7. A 1200bps data connection has now been established.

5.2 V.22 Answering Modem Application

This section describes how the CMX867 can be used in a V.22 Answering modem application, employing V.25 automatic answering and the V.22 recommended handshake sequence. This attempts to establish a 1200 bps connection.

1. It is assumed that the CMX867 will be in Powersave mode, with the Ring Detector circuits monitoring the line.
2. When a ring signal is detected connect the line (go off hook), set a 2150ms timer and power up the CMX867, setting the Tx Mode Register to DTMF/Tones mode (set for 'no tone' at this time) and the Rx Mode Register to V.22 1200bps Low Band receive, descrambler enabled, Rx USART disabled.
3. When the 2150ms timer expires set the Tx Mode Register to transmit the 2100Hz answer tone and set a 3300ms timer.
4. When the 3300ms timer expires set the Tx Mode Register to no tone and set a 75ms timer.
5. When the 75ms timer expires set the Tx Mode Register for V.22 High Band 1200bps transmission of unscrambled 1s. Monitor the received signal for scrambled 1s.
6. When scrambled 1s have been detected for 270ms, set the Tx Mode Register to V.22 High Band 1200bps scrambled 1s transmission and set a 765ms timer and enable the Rx USART.
7. Load the Tx Data Buffer with the first data to be transmitted.
8. When the 765ms timer expires set the Tx Mode Register for Start-Stop or Synchronous transmission of data from the Tx Data Buffer. This will start transmission of the data loaded in step 7.
9. A 1200bps data connection has now been established.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-50	+50	mA
Current into $\overline{RDRV}$ pin ($\overline{RDRV}$ pin low)		+50	mA
Current into or out of any other pin	-20	+20	mA
D2 / P4 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		1000	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C
E2 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		400	mW
Derating above 25°C		5.3	mW/°C above 25°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	+85	°C

6.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

V_{DD} = 2.7V to 5.5V at T_{AMB} = -40 to +85°C,
Xtal Frequency = 11.0592 or 12.288MHz ± 0.01% (100ppm)
0dBm corresponds to 775mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (Powersave mode)	1, 2	-	-	TBD	µA
(Reset but not powersave, V_{DD} = 3.0V)	1, 3	-	2.0	TBD	mA
(Reset but not powersave, V_{DD} = 5.0V)	1, 3	-	3.5	TBD	mA
(Running, V_{DD} = 3.0V)	1	-	3.5	TBD	mA
(Running, V_{DD} = 5.0V)	1	-	6.5	TBD	mA
Logic '1' Input Level	4	70%	-	-	V_{DD}
Logic '0' Input Level	4	-	-	30%	V_{DD}
Logic Input Leakage Current (V_{IN} = 0 to V_{DD}), (excluding XTAL/CLOCK input)		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 2 mA)		80%	-	-	V_{DD}
Output Logic '0' Level (I_{OL} = -3 mA)		-	-	0.4	V
$\overline{IRQ}$ output 'Off' State Current (V_{OUT} = V_{DD})		-	-	1.0	µA
RD and RT pin Schmitt trigger input high-goingthreshold (Vt_{HI}) (see Figure 21)		0.56V_{DD}	-	0.56V_{DD} + 0.6V	V
RD and RT pin Schmitt trigger input low-going threshold (Vt_{LO}) (see Figure 21)		0.44V_{DD} - 0.6V	-	0.44V_{DD}	V
$\overline{RDRV}$ 'ON' resistance to V_{SS} (V_{DD}= 3.0V)		-	-	TBD	Ω
$\overline{RDRV}$ 'OFF' resistance to V_{DD} (V_{DD}= 3.0V)		-	-	TBD	Ω
XTAL/CLOCK Input (timings for an external clock input)					
'High' Pulse Width		30	-	-	ns
'Low' Pulse Width		30	-	-	ns
Transmit DPSK Modes (V.22, Bell 212A)					
Carrier frequency, high band	5	-	2400	-	Hz
Carrier frequency, low band	5	-	1200	-	Hz
Baud rate	6	-	600	-	Baud
Bit rate	6	-	1200/600	-	bps
550Hz guard tone frequency		548	550	552	Hz
550Hz guard tone level with respect to data signal		-4.0	-3.0	-2.0	dB
1800Hz guard tone frequency		1797	1800	1803	Hz
1800Hz guard tone level with respect to data signal		-7.0	-6.0	-5.0	dB

	Notes	Min.	Typ.	Max.	Units
Transmit V.21 FSK Mode					
Baud rate	6	-	300	-	Baud
Mark (logical 1) frequency, high band		1647	1650	1653	Hz
Space (logical 0) frequency, high band		1847	1850	1853	Hz
Mark (logical 1) frequency, low band		978	980	982	Hz
Space (logical 0) frequency, low band		1178	1180	1182	Hz
Transmit Bell 103 FSK Mode					
Baud rate	6	-	300	-	Baud
Mark (logical 1) frequency, high band		2222	2225	2228	Hz
Space (logical 0) frequency, high band		2022	2025	2028	Hz
Mark (logical 1) frequency, low band		1268	1270	1272	Hz
Space (logical 0) frequency, low band		1068	1070	1072	Hz
Transmit V.23 FSK Mode					
Baud rate	6	-	1200/75	-	Baud
Mark (logical 1) frequency, 1200 baud		1298	1300	1302	Hz
Space (logical 0) frequency, 1200 baud		2097	2100	2103	Hz
Mark (logical 1) frequency, 75 baud		389	390	391	Hz
Space (logical 0) frequency, 75 baud		449	450	451	Hz
Transmit Bell 202 FSK Mode					
Baud rate	6	-	1200/150	-	Baud
Mark (logical 1) frequency, 1200 baud		1198	1200	1202	Hz
Space (logical 0) frequency, 1200 baud		2197	2200	2203	Hz
Mark (logical 1) frequency, 150 baud		386	387	388	Hz
Space (logical 0) frequency, 150 baud		486	487	488	Hz
DTMF/Single Tone Transmit					
Tone frequency accuracy		-0.2	-	+0.2	%
Distortion	7	-	1.0	2.0	%
Transmit Output Level					
Modem and Single Tone modes	7	-4.0	-3.0	-2.0	dBm
DTMF mode, Low Group tones	7	-2.0	-1.0	0.0	dBm
DTMF: level of High Group tones with respect to Low Group	7	+1.0	+2.0	+3.0	dB
Tx output buffer gain control accuracy	7	-0.25	-	+0.25	dB
Receive DPSK Modes (V.22, Bell 212A)					
Carrier frequency (high band)		2392	2400	2408	Hz
Carrier frequency (low band)		1192	1200	1208	Hz
Baud rate	9	-	600	-	Baud
Bit rate	9	-	1200/600	-	bps
Receive V.21 FSK Mode					
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		1638	1650	1662	Hz
Space (logical 0) frequency, high band		1838	1850	1862	Hz
Mark (logical 1) frequency, low band		968	980	992	Hz
Space (logical 0) frequency, low band		1168	1180	1192	Hz
Receive Bell 103 FSK Mode					
Acceptable baud rate		297	300	303	Baud

	Notes	Min.	Typ.	Max.	Units
Mark (logical 1) frequency, high band		2213	2225	2237	Hz
Space (logical 0) frequency, high band		2013	2025	2037	Hz
Mark (logical 1) frequency, low band		1258	1270	1282	Hz
Space (logical 0) frequency, low band		1058	1070	1082	Hz
Receive V.23 FSK Mode					
1200 baud					
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1280	1300	1320	Hz
Space (logical 0) frequency		2080	2100	2120	Hz
75 baud					
Acceptable baud rate		74	75	76	Baud
Mark (logical 1) frequency		382	390	398	Hz
Space (logical 0) frequency		442	450	458	Hz
Receive Bell 202 FSK Mode					
1200 baud					
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1180	1200	1220	Hz
Space (logical 0) frequency		2180	2200	2220	Hz
150 baud					
Acceptable baud rate		148	150	152	Baud
Mark (logical 1) frequency		377	387	397	Hz
Space (logical 0) frequency		477	487	497	Hz
Rx Modem Signal (FSK and DPSK Modes)					
Signal level	10	-45	-	-9	dBm
Signal to Noise Ratio (noise flat 300-3400Hz)		20	-	-	dB
Rx Modem '0011' Dibit Pattern Detector (1200bps DPSK mode)					
Will detect pattern lasting for		90.0	-		ms
Will not detect pattern lasting for				72.0	ms
Hold time (minimum detector 'On' time)		5.0	-		ms
Rx Modem Energy Detector					
Detect threshold ('Off' to 'On)	10,11	-	-	-43.0	dBm
Undetect threshold ('On' to 'Off')	10,11	-48.0	-	-	dBm
Hysteresis	10,11	2.0	-	-	dB
Detect ('Off' to 'On') response time					
DPSK modes	10,11	10.0	-	35.0	ms
300 and 1200 baud FSK modes	10,11	8.0	-	30.0	ms
150 and 75 baud FSK modes	10,11	16.0	-	60.0	ms
Undetect ('On' to 'Off') response time					
DPSK modes	10,11	10.0	-	55.0	ms
300 and 1200 baud FSK modes	10,11	10.0	-	40.0	ms
150 and 75 baud FSK modes	10,11	20.0	-	80.0	ms
Rx Answer Tone Detectors					
Detect threshold ('Off' to 'On)	10,12	-	-	-43.0	dBm
Undetect threshold ('On' to 'Off')	10,12	-48.0	-	-	dBm

	Notes	Min.	Typ.	Max.	Units
Hysteresis	10,12	2.0	-	-	dB
Detect ('Off' to 'On') response time	10,12	30.0	33.0	45.0	ms
Undetect ('On' to 'Off') response time	10,12	7.0	18.0	25.0	ms
2100Hz detector					
'Will detect' frequency		2050	-	2160	Hz
'Will not detect' frequency		-	-	2000	Hz
2225Hz detector					
'Will detect' frequency		2160	-	2285	Hz
'Will not detect' frequency		2335	-	-	Hz
Rx Call Progress Energy Detector					
Bandwidth (-3dB points) See Figure 8		275	-	665	Hz
Detect threshold ('Off' to 'On)	10,13	-	-	-37.0	dBm
Undetect threshold ('On' to 'Off')	10,13	-42.0	-	-	dBm
Hysteresis	10,13	2.0	-	-	dB
Detect ('Off' to 'On') response time	10,13	30.0	36.0	45.0	ms
Undetect ('On' to 'Off') response time	10,13	6.0	8.0	50.0	ms
DTMF Decoder					
Valid input signal levels (each tone of composite signal)	10	-30.0	-	0.0	dBm
Not decode level (either tone of composite signal)	10	-	-	-36.0	dBm
Twist = High Tone/Low Tone		-10.0	-	6.0	dB
Frequency Detect Bandwidth		±1.8	-		%
Frequency Not Detect Bandwidth				±3.5	%
Max level of low frequency noise (i.e. dial tone)					
Interfering signal frequency <= 550Hz	14	-	-	0.0	dB
Interfering signal frequency <= 450Hz	14	-	-	10.0	dB
Interfering signal frequency <= 200Hz	14	-	-	20.0	dB
Max. noise level with respect to signal	14,15	-	-	-10.0	dB
DTMF detect response time		-	-	40.0	ms
DTMF de-response time		-	-	30.0	ms
Status Register b5 high time		14.0	-	-	ms
'Will Detect' DTMF signal duration		40.0	-	-	ms
'Will Not Detect' DTMF signal duration		-	25.0	-	ms
Pause length detected		30.0	-	-	ms
Pause length ignored		-	-	15.0	ms
Receive Input Amplifier					
Input impedance (at 100Hz)		10.0			MΩ
Open loop gain (at 100Hz)			10000		V/V
Rx Gain Control Block accuracy		-0.25		+0.25	dB

Operating Characteristics Notes:

1. At 25°C, not including any current drawn from the CMX867 pins by external circuitry other than X1, C1 and C2.
2. All logic inputs at V_{SS} except for RT and $\overline{CS}$ inputs which are at V_{DD}.
3. General Mode Register b8 and b7 both set to 1.
4. Excluding RD and RT pins.

5. % carrier frequency accuracy is the same as XTAL/CLOCK % frequency accuracy.
6. Tx signal % baud or bit rate accuracy is the same as XTAL/CLOCK % frequency accuracy.
7. Measured between TXA and $\overline{TXA}$ pins with Tx Level Control gain set to 0dB, 1k2Ω load between TXA and $\overline{TXA}$, at V_{DD} = 3.0V (levels are proportional to V_{DD} - see Section 3.2). Level measurements for all modem modes are performed with random transmitted data and without any guard tone. 0dBm = 775mV_{RMS}.
8. Measured on the 2 or 4-wire line using the line interface circuits described in Section 3.2 with the Tx line signal level set to -10dBm for DPSK, FSK or single tones, -6dBm and -8dBm for DTMF tones. Excludes any distortion due to external components such as the line coupling transformer.
9. These are the bit and baud rates of the line signal; the acceptable tolerance is ±0.01%.
10. Rx 2 or 4-wire line signal level assuming 1dB loss in line coupling transformer with Rx Gain Control block set to 0dB and external components as Section 3.2.
11. Thresholds and times measured with random data for DPSK modes, continuous binary '1' for all FSK modes. Fixed compromise line equalizer enabled. Signal switched between off and -33dBm.
12. 'Typical' value refers to 2100Hz or 2225Hz signal switched between off and -33dBm. Times measured with respect to received line signal.
13. 'Typical' values refers to 400Hz signal switched between off and -33dBm.
14. Referenced to DTMF tone of lower amplitude.
15. Flat Gaussian Noise in 300-3400Hz band.

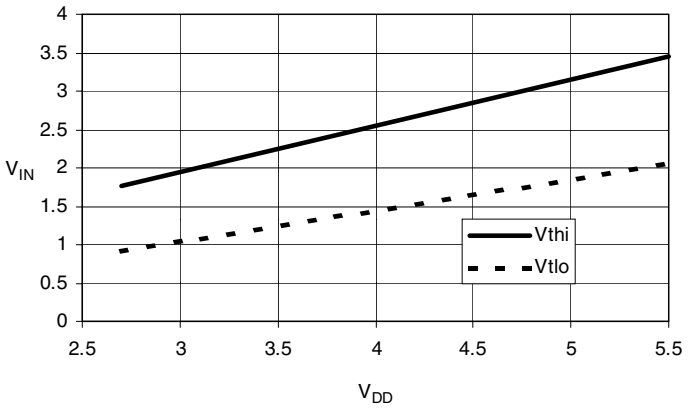


Figure 21: Typical Schmitt Trigger Input Voltage Thresholds vs. V_{DD}

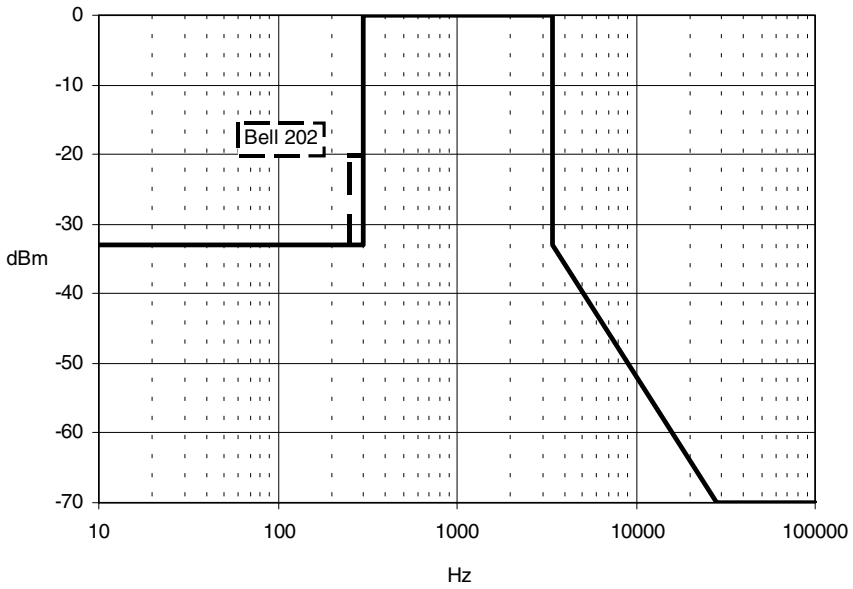


Figure 22: Maximum Out of Band Tx Line Energy Limits (see Operating Characteristics Note 8)

6.1.3.1 Timing

C-BUS Timings (See Figure 23)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	$\overline{CS}$ -Enable to Clock-High time		100	-	-	ns
t_{CSH}	Last Clock-High to $\overline{CS}$ -High time		100	-	-	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	-	-	ns
t_{HIZ}	$\overline{CS}$ -High to Reply Output 3-state time		-	-	1.0	µs
t_{CSOFF}	$\overline{CS}$ -High Time between transactions		1.0	-	-	µs
t_{NXT}	Inter-Byte Time		200	-	-	ns
t_{CK}	Clock-Cycle time		200	-	-	ns
t_{CH}	Serial Clock-High time		100	-	-	ns
t_{CL}	Serial Clock-Low time		100	-	-	ns
t_{CDS}	Command Data Set-Up time		75.0	-	-	ns
t_{CDH}	Command Data Hold time		25.0	-	-	ns
t_{RDS}	Reply Data Set-Up time		50.0	-	-	ns
t_{RDH}	Reply Data Hold time		0.0	-	-	ns

Maximum 30pF load on each C-BUS interface line.

Note: These timings are for the latest version of the C-BUS as embodied in the CMX867, and allow faster transfers than the original C-BUS timings given in CML Publication D/800/Sys/3 July 1994.

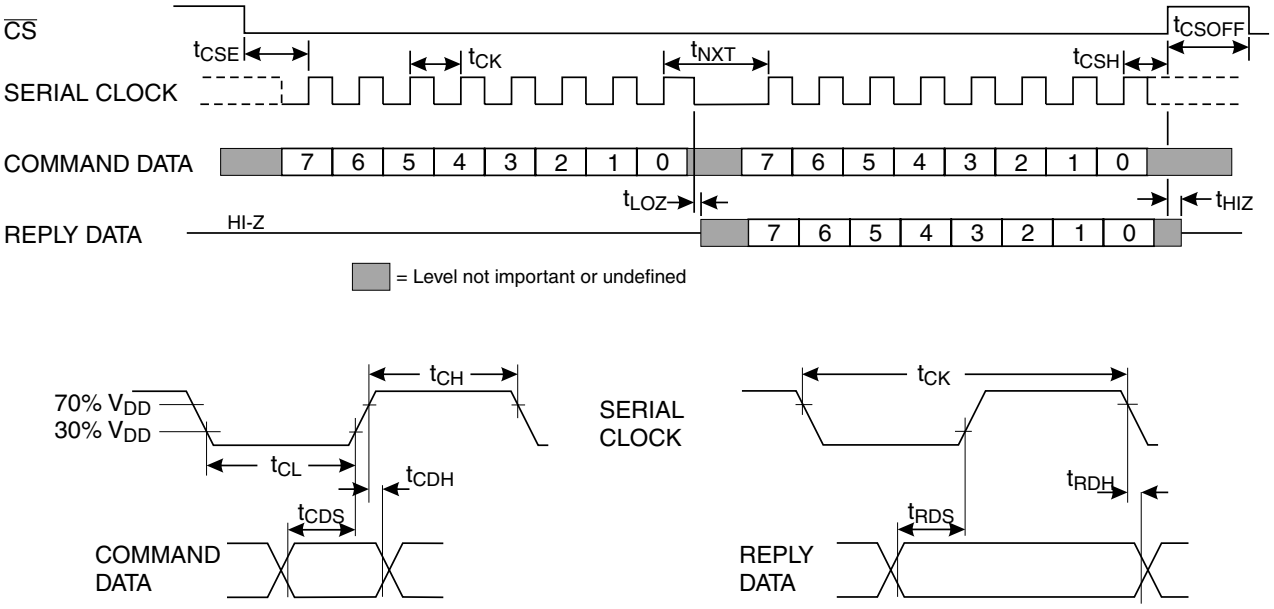
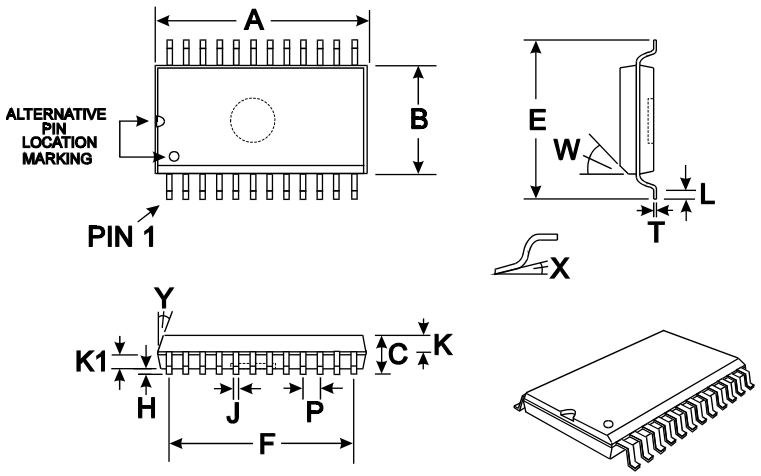


Figure 23: C-BUS Timing

6.2 Packaging



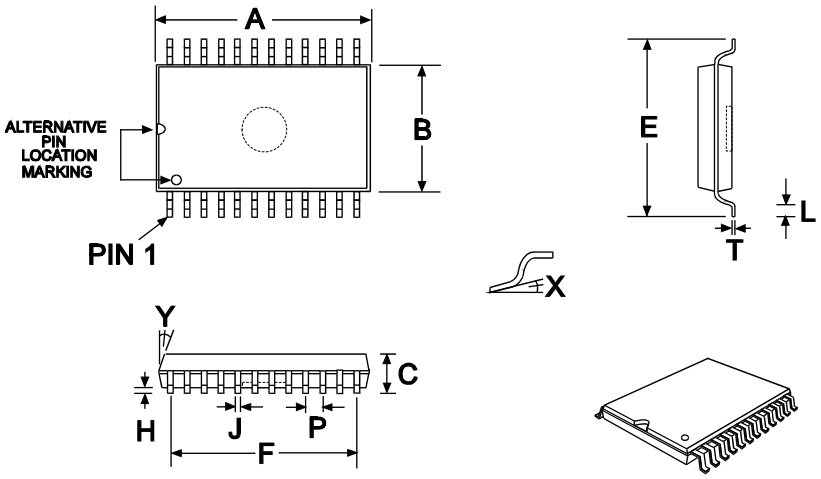
	DIM.	MIN.	TYP.	MAX.
*	A	0.597 (15.16)		0.613 (15.57)
*	B	0.286 (7.26)		0.299 (7.59)
	C	0.093 (2.36)		0.105 (2.67)
	E	0.390 (9.90)		0.419 (10.64)
	F		0.550 (14.1)	
	H	0.003 (0.08)		0.020 (0.51)
	J	0.013 (0.33)		0.020 (0.51)
	K		0.041 (1.04)	
	K1		0.041 (1.04)	
	L	0.016 (0.41)		0.050 (1.27)
	P		0.050 (1.27)	
	T	0.009 (0.23)		0.0125 (0.32)
	W		45°	
	X	0°		10°
	Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 24: 24-pin SOIC (D2) Mechanical Outline: *Order as part no. CMX867D2*



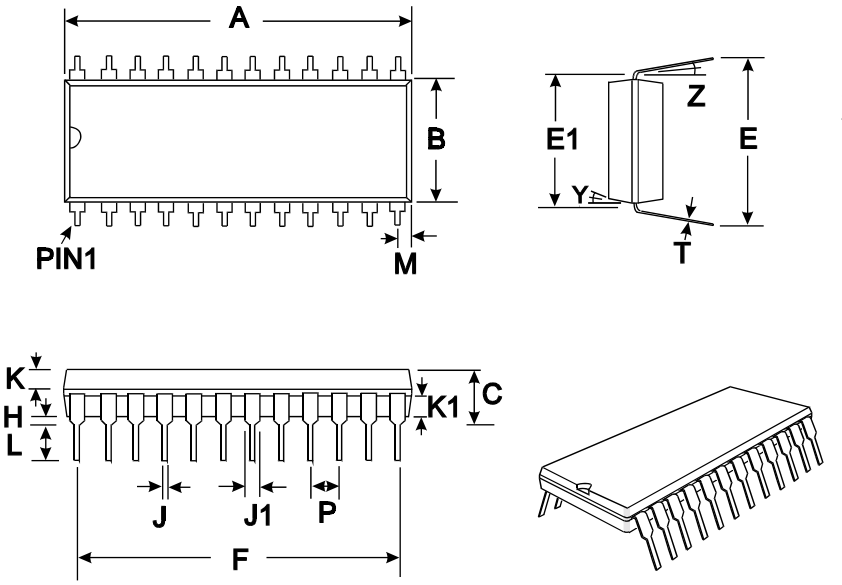
	DIM.	MIN.	TYP.	MAX.
*	A	0.303 (7.70)		0.311 (7.90)
*	B	0.169 (4.30)		0.177 (4.50)
	C	———		0.047 (1.20)
	E	0.248 (6.30)		0.256 (6.50)
	F		0.286 (7.15)	
	H	0.002 (0.05)		0.006 (0.15)
	J	0.007 (0.17)		0.012 (0.30)
	L	0.020 (0.50)		0.030 (0.75)
	P		0.026 (0.65)	
	T	0.003 (0.08)		0.008 (0.20)
	X	0°		7°
	Y		12°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 25: 24-pin TSSOP (E2) Mechanical Outline: *Order as part no. CMX867E2*



DIM.	MIN.	TYP.	MAX.
* A	1.200 (30.48)		1.270 (32.26)
* B	0.500 (12.70)		0.555 (14.10)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 26: 24-pin DIP (P4) Mechanical Outline: *Order as part no. CMX867P4*

