On-Screen Display Shrink Version

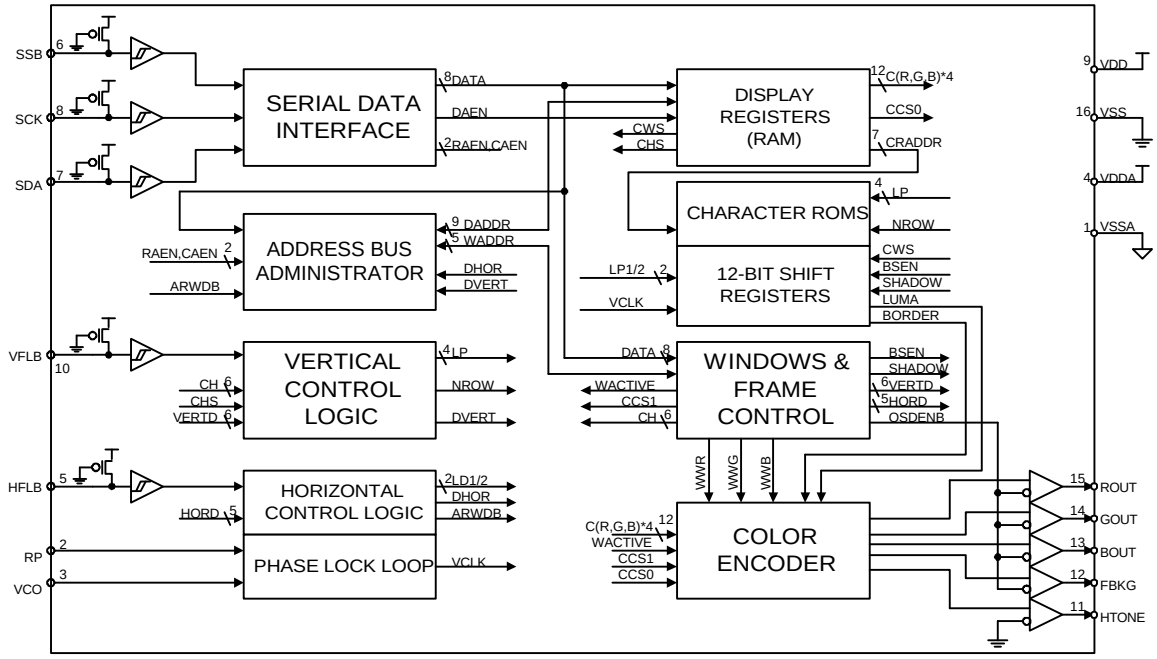
FEATURES

- On-chip phase lock loop circuitry for multi-sync operation.
- Horizontal input up to 100 KHz.
- 273-byte display registers to control full screen display.
- Full screen display consisting of 10 rows by 24 characters.
- 128 alphanumeric characters or graphic symbols built in character ROM.
- 12 x 16 dot matrix per character.
- Character by character color selection.
- 4 color selections in a total of 8 color combinations per row.
- 4-character size options available by doubling character height and/or width.
- Programmable positioning for display screen center.
- Character bordering and shadowing.
- Programmable vertical character height for multi-sync operation.
- Multi-level windowing effect.
- Half tone and fast blanking output.
- Compatible with both SPI bus and I^2C interface through pin selection.
- 16-pin PDIP package.

GENERAL DESCRIPTION

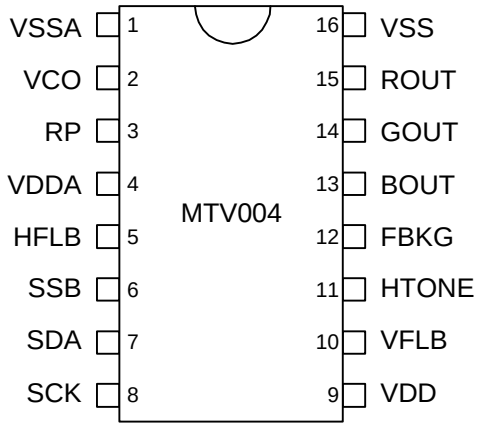
MTV004 is designed for use in monitor applications to display the built-in characters or symbols onto the monitor screen. The display operation is enabled by transferring data and control information in the microcontroller to RAM through a serial data interface. It can execute the full screen display automatically as well as some specific functions such as character bordering, shadowing, double height, double width and color control, frame positioning, vertical display height, and windowing effect.

BLOCK DIAGRAM



1.0 CONNECTION DIAGRAM

(16 pins PDIP 300 mil PACKAGE)



2.0 PIN DESCRIPTIONS

Name	I/O	Pin#	Function
VSSA	-	1	**Analog Ground.**
VCO	I/O	2	**Voltage Control Oscillator.** This pin is used to control the internal oscillator frequency by DC voltage input from an external low pass filter.
RP	I/O	3	**Bias Resistor.** The bias resistor is used to regulate the bias current for the internal oscillator to resonate at the specific dot frequency.
VDDA	-	4	**Analog Power Supply.** Positive 5 V DC supply for internal analog circuitry. A 0.1uF decoupling capacitor should be connected across to VDDA and VSSA as close to the device as possible.
HFLB	I	5	**Horizontal Input.** This pin is used to input the horizontal synchronizing signal. It is triggered by a negative edge and has an internal pull-up resistor.
SSB	I	6	**Serial Interface Enable.** Used to enable the serial data and to select I^2C or SPI bus operation. If this pin is left floating, the I^2C bus is enabled, otherwise the SPI bus is enabled.
SDA	I	7	**Serial Data Input.** The external data transfers through this pin to the internal display and control registers. It has an internal pull-up resistor.
SCK	I	8	**Serial Clock Input.** Clock input pin used to synchronize transferring of data. It has an internal pull-up resistor.
VDD	-	9	**Digital Power Supply.** Positive 5 V DC supply for internal digital circuitry. A 0.1uF decoupling capacitor should be connected across to VDD and VSS as close to the device as possible.
VFLB	I	10	**Vertical Input.** This pin is used to input the vertical synchronizing signal. It is negatively triggered and has an internal pull-up resistor.
HTONE	O	11	**Half Tone Output.** This pin is used to attenuate external R,G,B amplifiers for a transparent windowing effect.
FBKG	O	12	**Fast Blanking Output.** Used to cut off external R,G,B signals while the chip is displaying characters or windows.
BOUT	O	13	**Blue Color Output.** Blue color video signal output.
GOUT	O	14	**Green Color Output.** Green color video signal output.
ROUT	O	15	**Red Color Output.** Red color video signal output.
VSS	-	16	**Digital Ground.**

3.0 FUNCTIONAL DESCRIPTIONS

3.1 Serial Data Interface

The serial data interface receives data transmitted from an external controller. There are 2 types of bus that can be accessed through the serial data interface: SPI bus and I^2C bus.

3.1.1 SPI Bus

While SSB pin is pulled to "high" or "low" level, the SPI bus operation is selected. A valid transmission should be started by pulling SSB to "low" level, enabling MTV004 in receiving mode, and retaining "low" level until the last cycle for a complete data packet transfer. The protocol is shown in Figure 2:

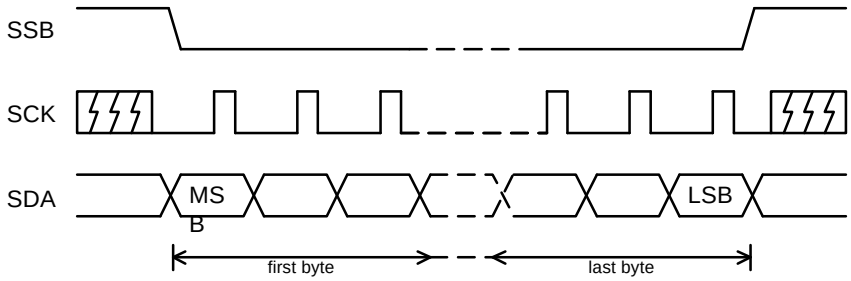


Figure 2. Data Transmission Protocol

There are 3 transmission formats as shown below:

Format (a) R - C - D → R - C - D → R - C - D .....
Format (b) R - C - D → C - D → C - D → C - D .....
Format (c) R - C - D → D → D → D → D → D .....

R=row address, C=column address, D=display data

3.1.2 I^2C Bus

The I^2C bus operation is only selected when the SSB pin is left floating. A valid transmission should begin by writing the slave address 7AH, which is the mask option, to MTV004. The protocol is shown in Figure 3:

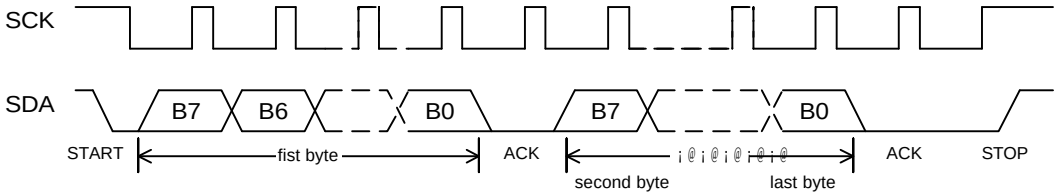


Figure 3. Data Transmission Protocol (I^2C)

There are 3 transmission formats as shown below:

Format (a) S - R - C - D → R - C - D → R - C - D .....
Format (b) S - R - C - D → C - D → C - D → C - D .....
Format (c) S - R - C - D → D → D → D → D → D .....
S=slave address, R=row address, C=column address, D=display data

Each arbitrary length of data packet consists of 3 portions: row address (R), column address (C) and display data (D). Format (a) is suitable for updating small amounts of data that will be allocated with different row and column addresses. Format (b) is recommended for updating data that has the same row address but a different column address. Format (c) should be used for massive data updating or a full-screen data change to increase

transmission efficiency. Row and column addresses are incremented automatically when format (c) is applied. Furthermore, the locations in columns 24-29 should be filled with dummy data.

The MSB (b7) bit is used to distinguish row and column addresses when transferring data from the external controller. The b6 bit is used to differentiate column addresses for formats (a), (b) and (c), respectively. The address configuration is shown in Table 1.

Table 1. Address Configuration in Interface

Address	b7	b6	b5	b4	b3	b2	b1	b0	Format
Row	1	x	x	x	R3	R2	R1	R0	a,b,c
Column$_{ab}$	0	0	x	C4	C3	C2	C1	C0	a,b
Column$_{c}$	0	1	x	C4	C3	C2	C1	C0	c

The data transmission is permitted to change from format (a) to formats (b) and (c), or from format (b) to format (a), but not from format (c) back to formats (a) and (b). The alternation between formats is configured according to the state diagram shown in Figure 4.

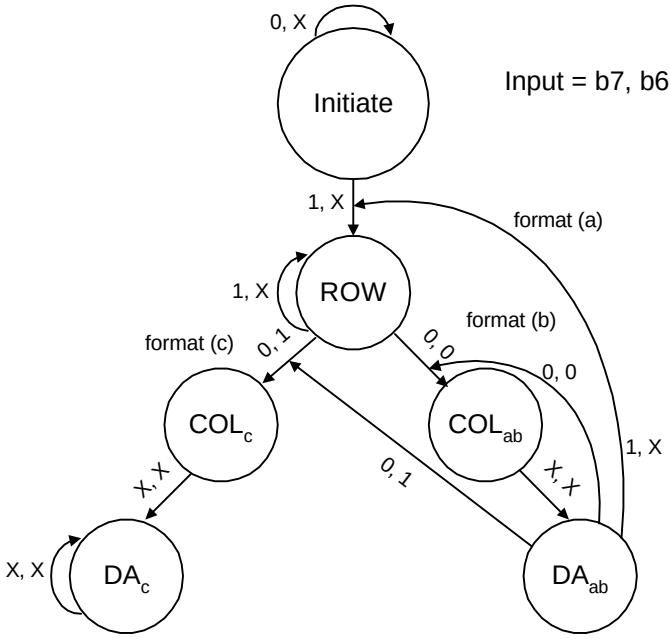


Figure 4. Format State Diagram

3.2 Address Bus Administrator

The administrator manages bus address arbitration of display registers (RAM) during external data writing or internal display control. The external data writing through the serial data interface to RAM must be synchronized by internal display timing. In addition, the administrator also provides automatic incrementing to the address bus when external writing using format (c) and the full-screen display control are applied.

3.3 Vertical Control Logic

The vertical logic generates different vertical display sizes for most display standards in current monitors. The vertical display size is calculated using the information of the double character height bit (CHS) and vertical display height control registers (CH5-CH0). The algorithm of the repeating character line display is shown in Tables 2 and 3. The programmable vertical size range is 160 lines to maximum 1260 lines.

The vertical display center for a full-screen display may be figured out according to the information of the vertical starting position register (VERTD) and VFLB input. The vertical delay, starting from the falling edge of VFLB, is calculated using the following equation:

Vertical delay time = (VERTD * 4 + 1) * H H = 1 horizontal line display time

Table 2. Repeat Line Character Weight

CH5 - CH0	Repeat Line Weight
CH5,CH4=11	(+16)*3
CH5,CH4=10	(+16)*2
CH5,CH4=0x	+16
CH3=1	+8
CH2=1	+4
CH1=1	+2
CH0=1	+1

Table 3. Repeat Line Character Number

Repeat Line Weight	Repeat Line #															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v
+16	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note: " v " means the nth line in the character would be repeated once, while "-" means the nth line in the character would not be repeated.

3.4 Horizontal Control Logic

The horizontal control logic is used to generate control timing for the horizontal display based on the double character width bit (CWS), horizontal positioning register (HORD) and HFLB input. A horizontal display line consists of 384 dots, which include 288 dots for 24 display characters and 96 dots for the remaining blank region. The horizontal delay starting from the HFLB falling edge is calculated using the following equation:

horizontal delay time = (HORD * 6 + 61)* P - phase error detection pulse width
P= 1 pixel display time = 1 horizontal display time / 384

3.5 Phase Lock Loop (PLL)

On-chip PLL generates system clock timing (VCLK) by tracking the input HFLB. The frequency of VCLK is determined using the following equation:

VCLK = HFLB Freq.* 384 ,

The frequency ranges from 3.84MHz to 38.4MHz. See Table 4.

Table 4. Frequency Range

HFLB	VCLK
10KHz to 100KHz	3.84MHz to 38.4MHz

In addition, when HFLB input is not present in MTV004, the PLL will generate a specific system clock (approximately 2.5MHz) by a built-in oscillator to ensure data integrity.

3.6 Display Registers

The internal RAM contains display and row control registers. The display registers have 240 locations, which are allocated between row 0/column 0 and row 9/column 23 as shown in Figure 4. Each display register has a color selection bit and its corresponding character address in ROM. The row control register is allocated between column 30 and column 31 for row 0 to row 9. It is used to set character size and color attribute of each respective row. If double width character is chosen, only even column characters will be displayed on-screen and the odd column characters would be hidden.

ROW #	COLUMN #		
	0 23	24 29	30
0 1 8 9	DISPLAY REGISTERS	RESERVED	ROW CTRL REG

ROW 10	COLUMN #			
	0 2	3 5	6 8	9 12
	WINDOW1	WINDOW2	WINDOW3	FRAME CRTL REG

Figure 4. Memory Map

-Register Descriptions

(i) Display Register

b7	b6	b5	b4	b3	b2	b1	b0
CCS0	←			CRADDR			→

b7 CCS0 - This bit is used to select character color. Color 1 will be selected if CCS0 is set to "0", otherwise color 2 is selected. Colors 1 and 2 are defined in the respective row control register.
b6 - 0 CRADDR - Defines the ROM character address.

(ii) Row Control Registers

COLN 30	b7	b6	b5	b4	b3	b2	b1	b0
	R1	G1	B1	R2	G2	B2	CHS	CWS

b7 - 2 Color 1 is defined by R1, G1, B1 and color 2 by R2, G2, B2.
b1 CHS - Defines double height character to the respective row.
b0 CWS - Defines double width character to the respective row.

COLN 31	b7	b6	b5	b4	b3	b2	b1	b0
	R3	G3	B3	R4	G4	B4	-	-

b7 - 2 Colors 3 and 4 are defined by R3, G3, B3 and R4, G4, B4, respectively. When a window overlaps with the character and the corresponding CCS1 is set to "1", colors 3 and 4 should be chosen.

3.7 Character ROM

The character ROM contains 128 built-in characters and symbols. Each character and symbol consists of 12x16 matrix dots. The detailed pattern structures for each character and symbols are shown in **Section 10.0**. All alphanumeric characters are specially designed by leaving a blank dot space on 4 sides, and this blank space is occupied by the blackedge dots if the bordering or shadowing effect is activated.

3.8 12-Bit Shift Register

There are 2 shift registers included in the design which can shift out luminance and border dots to the color encoder. The bordering and shadowing feature is configured in this block. For a bordering effect, the character will be enveloped with blackedge on 4 sides. For shadowing effect, the character is enveloped with blackedge on right and bottom sides only.

3.9 Window and Frame Control

The display frame position is completely controlled by the contents of VERTD and HORD. The window size and position control are specified in columns 0-8 on row 10 of the memory map, as shown in Figure 4. Window 1 has the highest priority and window 3 has the lowest when 2 windows are overlapping. More detailed information is described below:

- Register Descriptions

(i) Window Control Registers

ROW 10

	b7	b6	b5	b4	b3	b2	b1	b0
Column 0,3 OR 6	ROW START ADDR				ROW END ADDR			
	MSB			LSB	MSB			LSB

	b7	b6	b5	b4	b3	b2	b1	b0
Column 1,4 OR 7	COL START ADDR					WEN	CCS1	-
	MSB				LSB			

	b7	b6	b5	b4	b3	b2	b1	b0
Column 2,5 OR 8	COL END ADDR					R	G	B
	MSB				LSB			

START(END) ADDR - These addresses are used to specify the window size. It should be noted that when the start address is greater than the end address, the window will be disabled.
WEN - Enables the window display.
CCS1 - Extends the character color selection to 4 colors.

(ii) Frame Control Registers

ROW 10

	b7	b6	b5	b4	b3	b2	b1	b0
Column 9	-	-	VERTD					
			MSB					LSB

VERTD - Specifies the starting position for vertical display. There is a total of 64 steps and each step is incremented by 4 horizontal display lines. The initial value is 4 after power-up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column10	-	-	-	HORD				
				MSB				LSB

HORD - Defines the starting position for horizontal display. There is a total of 32 steps and each step is incremented by 6 dots. The initial value is 15 after power-up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column11	-	-	CH5	CH4	CH3	CH2	CH1	CH0

CH5-CH0 - Defines the character vertical height. The height is programmable from 16 to 63 lines.
The character vertical height is at least 16 lines if the contents of CH5-CH0 are less than 16. For example, when CH5~CH0 contents equal 2, the character vertical height is regarded as equal to 18 lines. See Tables 2 and 3 for a detailed description of this operation.

Column12	b7	b6	b5	b4	b3	b2	b1	b0
	OSDEN	BSEN	SHADOW	-	-	-	-	FBKGC

OSDEN - Activates OSD operation when this bit is set to 1.
BSEN - Enables the bordering and shadowing effect.
SHADOW - Activates the shadowing effect if this bit is set, otherwise the bordering is chosen.
FBKGC - Defines the output configuration for the FBKG pin. When it is set to 0, the FBKG outputs High during the display of characters or windows, otherwise it outputs High only during the display of characters.

3.10 Color Encoder

The decoder generates video output to ROUT, GOUT and BOUT by integrating window color, border blacking, luminance output and color selection output (CCS0, CCS1) to form desired video outputs.

4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VDD, VDDA)	-0.3 to +7 V
Voltage with respect to Ground	-0.3 to VDD+0.3 V
Storage Temperature	-65 to +150 ^{o}C
Ambient Operating Temperature	0 to +70 ^{o}C

5.0 OPERATING CONDITIONS

DC Supply Voltage (VDD, VDDA)	+4.75 to +5.25 V
Operating Temperature	0 to +70 ^{o}C

6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Conditions(Notes)	Min.	Max.	Unit
V_{IH}	Input High Voltage	-	3.5	VDD+0.3	V
V_{IL}	Input Low Voltage	-	VSS-0.3	1.5 (1.0 for SSB pin)	V
V_{OH}	Output High Voltage	$I_{OH} \leq$ -5 mA	VDD-0.8	-	V
V_{OL}	Output Low Voltage	$I_{OL} \leq$ 5 mA	-	0.5	V
ICC	Supply Current	Vin = VDD, I_{load} = 0uA	-	25	mA

7.0 SWITCHING CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{HFLB}	HFLB input frequency	10	-	100	KHz
T_r	Output rise time	-	-	10	ns
T_f	Output fall time	-	-	10	ns
t_{BCSU}	SSB to SCK set-up time	200	-	-	ns
t_{BCH}	SSB to SCK hold time	100	-	-	ns
t_{DCSU}	SDA to SCK set-up time	200	-	-	ns
t_{DCH}	SDA to SCK hold time	100	-	-	ns
t_{SCKH}	DCK high time	200	-	-	ns
t_{SCKL}	DCK low time	200	-	-	ns

8.0 TIMING DIAGRAMS

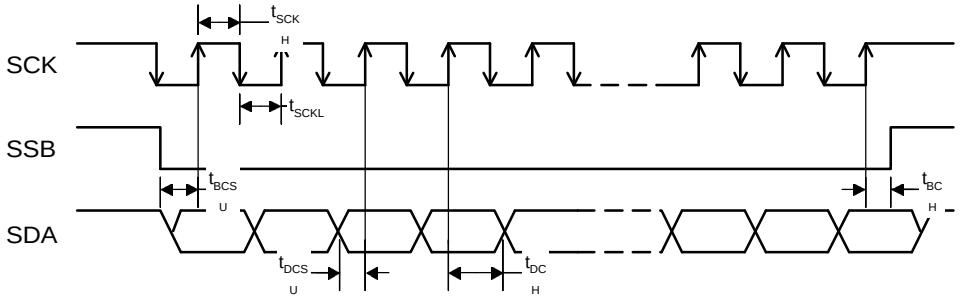
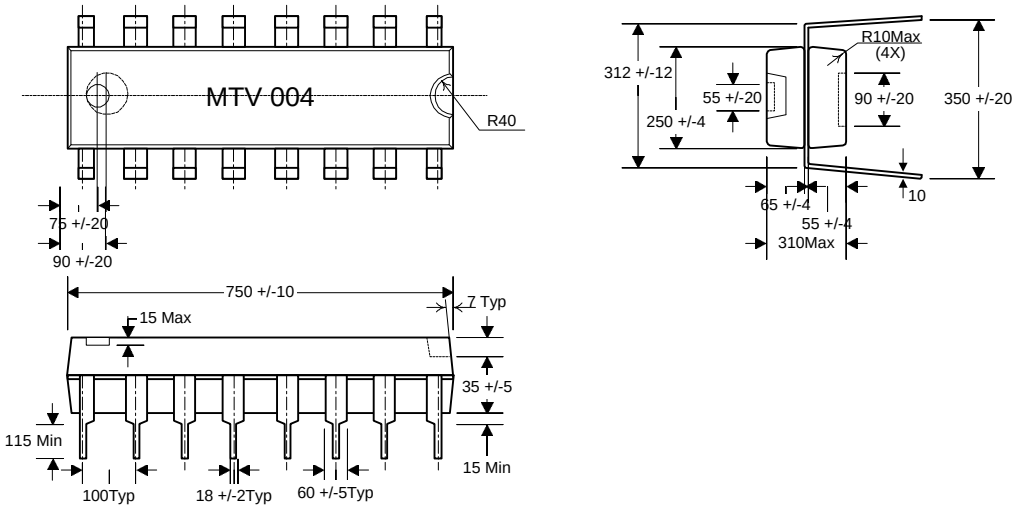


Figure 5. Data Interface Timing

9.0 PACKAGE DIMENSION

16 PIN PDIP
Unit: mil



10.0 CHARACTERS AND SYMBOLS PATTERN

Please see the attachment.