MYSON TECHNOLOGY

MTV112E
(Rev 1.8)

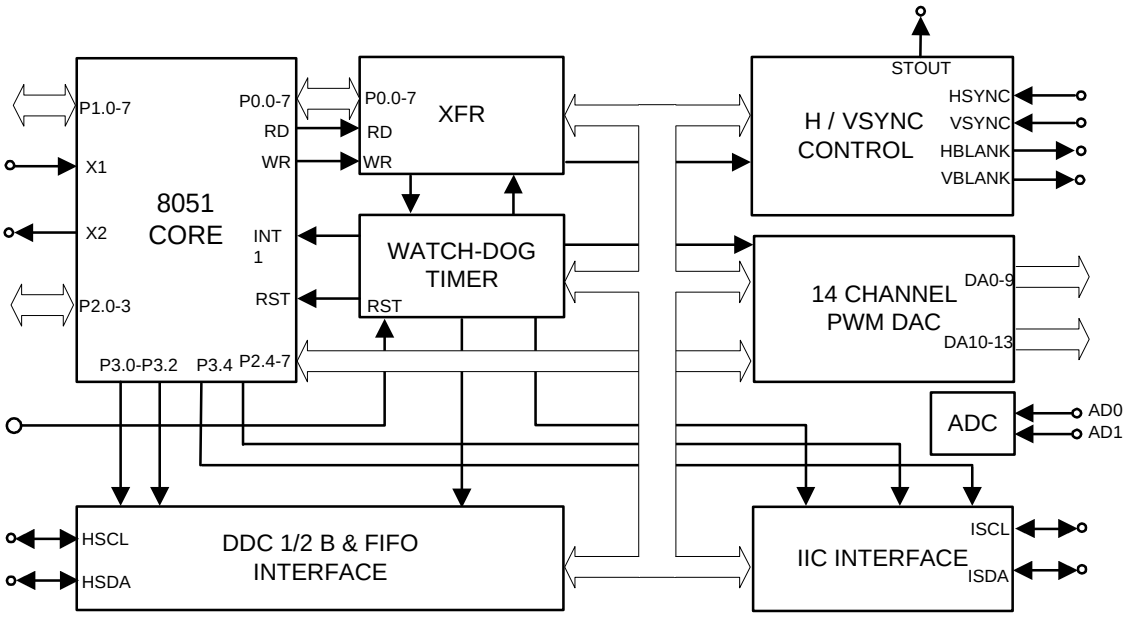
8051 Embedded CRT Monitor Controller OTP Version

FEATURES

8051 core.
384-byte internal RAM.
32K-byte program EPROM.
14-channel 10V open-drain PWM DAC, 10 dedicated channels and 4 channels shared with I/O pin.
MAX, 23 I/O pins.
SYNC processor for composite separation, polarity and frequency check, and polarity adjustment.
Built-in monitor self-test pattern generator.
Built-in low power reset circuit.
One slave mode IIC interface and one master mode IIC interface.
IIC interface for DDC1/DDC2B and EEPROM; only one EEPROM needed to store DDC1/DDC2B and display mode information.
Dual 4-bit ADC.
Watchdog timer with programmable interval.
40-pin PDIP and 44-pin PLCC package.

GENERAL DESCRIPTION

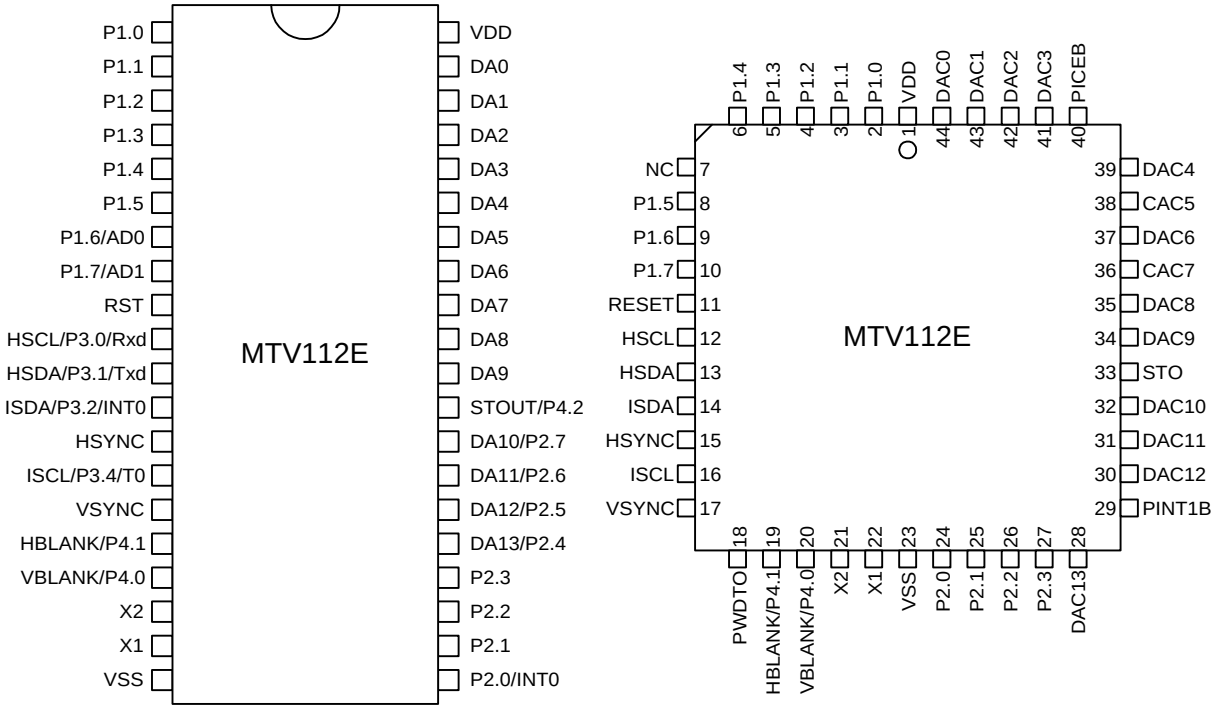
The MTV112E micro-controller is an 8051 CPU core embedded device specially tailored to CRT monitor applications. It includes an 8051 CPU core, 384-byte SRAM, 14 built-in PWM DACs, DDC1/DDC2B interface, 24Cxx series EEPROM interface, A/D converter and a 32K-byte internal program EPROM.



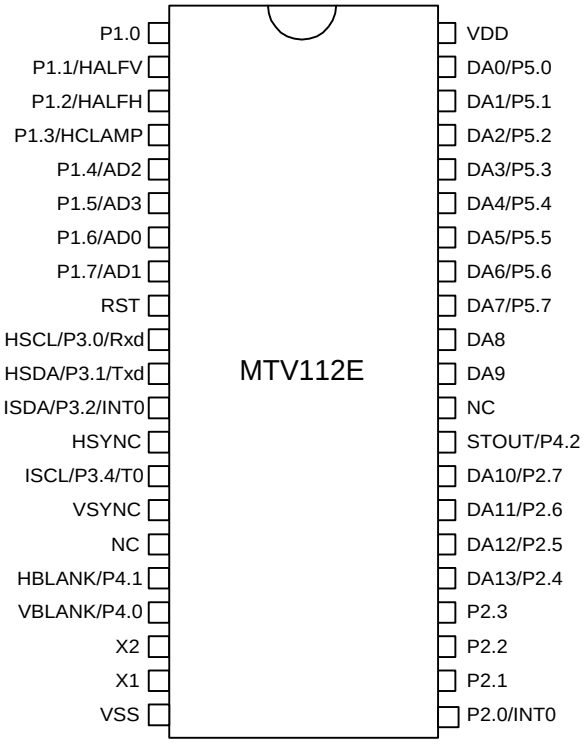
BLOCK DIAGRAM

This datasheet contains new product information. Myson Technology reserves the rights to modify the product specification without notice. No liability is assumed as a result of the use of this product. No rights under any patent accompany the sale of the product.

1.0 PIN CONNECTION



Note: 44-pin PLCC, PICEB, PALE, PWDTO and PINT1B are only for MICE Mode.



2.0 PIN DESCRIPTIONS

Name	Type	Pin#	Description
P1.0	I/O	1	General purpose I/O
P1.1	I/O	2	General purpose I/O
P1.2	I/O	3	General purpose I/O
P1.3	I/O	4	General purpose I/O
P1.4	I/O	5	General purpose I/O
P1.5	I/O	6	General purpose I/O
P1.6/AD0	I/O	7	General purpose I/O / ADC input
P1.7/AD1	I/O	8	General purpose I/O / ADC input
RST	I	9	Active high reset
HSCL/P3.0/Rxd	I/O	10	IIC clock / General purpose I/O / Rxd
HSDA/P3.1/Txd	I/O	11	IIC data / General purpose I/O / Txd
ISDA/P3.2/INT0	I/O	12	IIC data / General purpose I/O / INT0
HSYNC	I	13	Horizontal SYNC or Composite SYNC
ISCL/P3.4/T0	I/O	14	IIC clock / General purpose I/O / T0
VSYNC	I	15	Vertical SYNC
HBLANK/P4.1	O	16	Horizontal blank / General purpose output
VBLANK/P4.0	O	17	Vertical blank / General purpose output
X2	O	18	Oscillator output
X1	I	19	Oscillator input
VSS	-	20	Ground
P2.0/INT0	I/O	21	General purpose I/O / INT0
P2.1	I/O	22	General purpose I/O
P2.2	I/O	23	General purpose I/O
P2.3	I/O	24	General purpose I/O
DA13/P2.4	I/O	25	PWM DAC output / General purpose I/O (open-drain)
DA12/P2.5	I/O	26	PWM DAC output / General purpose I/O (open-drain)
DA11/P2.6	I/O	27	PWM DAC output / General purpose I/O (open-drain)
DA10/P2.7	I/O	28	PWM DAC output / General purpose I/O (open-drain)
STOUT/P4.2	O	29	Self-test video output / General purpose output
DA9	O	30	PWM DAC output (open-drain)
DA8	O	31	PWM DAC output (open-drain)
DA7	O	32	PWM DAC output (open-drain)
DA6	O	33	PWM DAC output (open-drain)
DA5	O	34	PWM DAC output (open-drain)
DA4	O	35	PWM DAC output (open-drain)
DA3	O	36	PWM DAC output (open-drain)
DA2	O	37	PWM DAC output (open-drain)
DA1	O	38	PWM DAC output (open-drain)
DA0	O	39	PWM DAC output (open-drain)
VDD	-	40	Positive power supply

3.0 FUNCTIONAL DESCRIPTION

1. 8051 CPU Core

MTV112E includes all 8051 functions with the following exceptions:

1.1 PSEN, ALE, RD and WR pins are disabled. The external RAM access is restricted to XFRs within MTV112E.

1.2 Port 0, port 3.3, and ports 3.5 ~ 3.7 are not general-purpose I/O ports. They are dedicated to monitor control or DAC pins.
1.3 INT1 and T1 input pins are not provided.
1.4 Ports 2.4 ~ 2.7 are shared with DAC pins; ports 3.0 ~ 3.2, and port3.4 are shared with monitor control pins.

In addition, there are 2 timers, 5 interrupt sources and a serial interface compatible with the standard 8051. The Txd/Rxd (P3.0/P3.1) pins are shared with DDC interface. INT0/T0 pins are shared with IIC interface. An extra option can be used to switch the INT0 source from P3.2 to P2.0. This feature maintains an external interrupt source when IIC interface is enabled.

Note: All registers listed in this document reside in the external RAM area (XFR). For the internal RAM memory map please refer to the 8051 spec.

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PADMOD	30h (w)	SINT0	IICF	DDCE	IICE	DA13E	DA12E	DA11E	DA10E

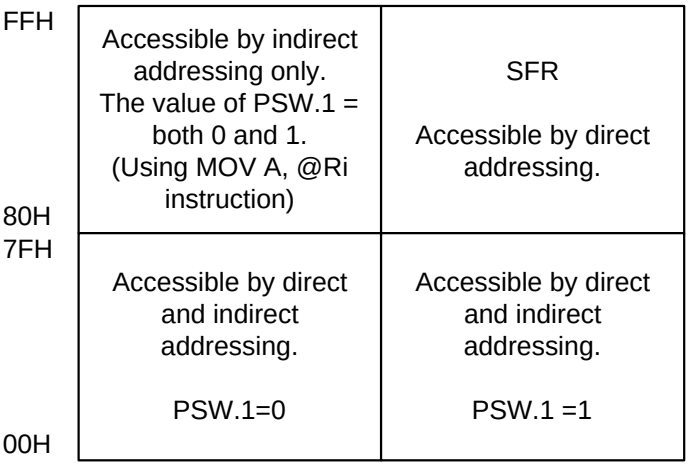
SINT0 = 1 → INT0 source is pin #21.
= 0 → INT0 source is pin #12.
IICF = 1 → Selects 400kHz master IIC speed.
= 0 → Selects 100kHz master IIC speed.
DDCE = 1 → Pin #10 is HSCL; pin #11 is HSDA.
= 0 → Pin #10 is P3.0/Rxd; pin #11 is P3.1/Txd.
IICE = 1 → Pin #12 is ISDA; pin #14 is ISCL.
= 0 → Pin #12 is P3.2/(INT0*); pin #14 is P3.4/T0.
DA13E = 1 → Pin #25 is DA13.
= 0 → Pin #25 is P2.4.
DA12E = 1 → Pin #26 is DA12.
= 0 → Pin #26 is P2.5.
DA11E = 1 → Pin #27 is DA11.
= 0 → Pin #27 is P2.6.
DA10E = 1 → Pin #28 is DA10.
= 0 → Pin #28 is P2.7.
* SINT0 should be 0 in this case.

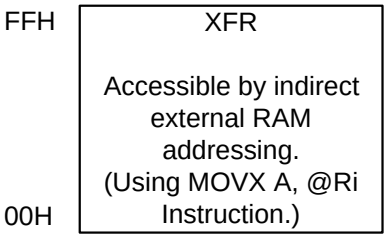
2. Memory Allocation

2.1 Internal Special Function Registers (SFR)
SFR is a group of registers that is the same as standard 8051.

2.2 Internal RAM
There is a 384 bytes RAM in MTV112E. The first portion of the RAM area contains 256 bytes, accessible by setting PSW.1=0; the second portion of the RAM area contains 128 bytes, accessible by setting PSW.1=1.

2.3 External Special Function Registers (XFR)
XFR is a group of registers allocated in the 8051 external RAM area. Most of the registers are used for monitor control or PWM DAC. The program can initialize Ri value and use "MOVX" instruction to access these registers.





3. PWM DAC

Each D/A converter's output pulse width is controlled by an 8-bit register in XFR. The frequency of these outputs is Xtal frequency/253 or Xtal frequency/256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to the DAC register generates stable high output. If DIV253=0, the output will pulse low at least once even if the DAC register's content is FFH. Writing 00H to the DAC register generates stable low output.

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DA0	20h (r/w)	$DA0_{b7}$	$DA0_{b6}$	$DA0_{b5}$	$DA0_{b4}$	$DA0_{b3}$	$DA0_{b2}$	$DA0_{b1}$	$DA0_{b0}$
DA1	21h (r/w)	$DA1_{b7}$	$DA1_{b6}$	$DA1_{b5}$	$DA1_{b4}$	$DA1_{b3}$	$DA1_{b2}$	$DA1_{b1}$	$DA1_{b0}$
DA2	22h (r/w)	$DA2_{b7}$	$DA2_{b6}$	$DA2_{b5}$	$DA2_{b4}$	$DA2_{b3}$	$DA2_{b2}$	$DA2_{b1}$	$DA2_{b0}$
DA3	23h (r/w)	$DA3_{b7}$	$DA3_{b6}$	$DA3_{b5}$	$DA3_{b4}$	$DA3_{b3}$	$DA3_{b2}$	$DA3_{b1}$	$DA3_{b0}$
DA4	24h (r/w)	$DA4_{b7}$	$DA4_{b6}$	$DA4_{b5}$	$DA4_{b4}$	$DA4_{b3}$	$DA4_{b2}$	$DA4_{b1}$	$DA4_{b0}$
DA5	25h (r/w)	$DA5_{b7}$	$DA5_{b6}$	$DA5_{b5}$	$DA5_{b4}$	$DA5_{b3}$	$DA5_{b2}$	$DA5_{b1}$	$DA5_{b0}$
DA6	26h (r/w)	$DA6_{b7}$	$DA6_{b6}$	$DA6_{b5}$	$DA6_{b4}$	$DA6_{b3}$	$DA6_{b2}$	$DA6_{b1}$	$DA6_{b0}$
DA7	27h (r/w)	$DA7_{b7}$	$DA7_{b6}$	$DA7_{b5}$	$DA7_{b4}$	$DA7_{b3}$	$DA7_{b2}$	$DA7_{b1}$	$DA7_{b0}$
DA8	28h (r/w)	$DA8_{b7}$	$DA8_{b6}$	$DA8_{b5}$	$DA8_{b4}$	$DA8_{b3}$	$DA8_{b2}$	$DA8_{b1}$	$DA8_{b0}$
DA9	29h (r/w)	$DA9_{b7}$	$DA9_{b6}$	$DA9_{b5}$	$DA9_{b4}$	$DA9_{b3}$	$DA9_{b2}$	$DA9_{b1}$	$DA9_{b0}$
DA10	2Ah (r/w)	$DA10_{b7}$	$DA10_{b6}$	$DA10_{b5}$	$DA10_{b4}$	$DA10_{b3}$	$DA10_{b2}$	$DA10_{b1}$	$DA10_{b0}$
DA11	2Bh (r/w)	$DA11_{b7}$	$DA11_{b6}$	$DA11_{b5}$	$DA11_{b4}$	$DA11_{b3}$	$DA11_{b2}$	$DA11_{b1}$	$DA11_{b0}$
DA12	2Ch (r/w)	$DA12_{b7}$	$DA12_{b6}$	$DA12_{b5}$	$DA12_{b4}$	$DA12_{b3}$	$DA12_{b2}$	$DA12_{b1}$	$DA12_{b0}$
DA13	2Dh (r/w)	$DA13_{b7}$	$DA13_{b6}$	$DA13_{b5}$	$DA13_{b4}$	$DA13_{b3}$	$DA13_{b2}$	$DA13_{b1}$	$DA13_{b0}$
WDT	80h	WEN	WCLR	CLRDDC	DIV253	X	WDT2	WDT1	WDT0

DA0 (r/w) : The output pulse width control for DA0.
DA1 (r/w) : The output pulse width control for DA1.
DA2 (r/w) : The output pulse width control for DA2.
DA3 (r/w) : The output pulse width control for DA3.
DA4 (r/w) : The output pulse width control for DA4.
DA5 (r/w) : The output pulse width control for DA5.
DA6 (r/w) : The output pulse width control for DA6.
DA7 (r/w) : The output pulse width control for DA7.
DA8 (r/w) : The output pulse width control for DA8.
DA9 (r/w) : The output pulse width control for DA9.
DA10 (r/w) : The output pulse width control for DA10.

DA11 (r/w) : The output pulse width control for DA11.
DA12 (r/w) : The output pulse width control for DA12.
DA13 (r/w) : The output pulse width control for DA13.
WDT (w) : Watchdog timer & special control bit.
DIV253 = 1 → The PWM DAC output frequency is Xtal frequency/253.
= 0 → The PWM DAC output frequency is Xtal frequency/256.

*1. All D/A converters are centered with value 80h after power-on.

4. H/V SYNC Processing

The H/V SYNC processing block performs the functions of composite signal separation, SYNC input presence check, frequency counting, and polarity detection and control, as well as the protection of VBLANK output while VSYNC speeds up to a high DDC communication clock rate. The present and frequency function block treat any pulse less than one OSC period as noise.

4.1 Composite SYNC Separation

MTV112E continuously monitors the input HSYNC. If the vertical SYNC pulse can be extracted from the input, a CVpre flag is set and the user can select the extracted "CVSYNC" for the source of polarity check, frequency count and VBLANK. The CVSYNC will have a 10-16 us delay compared to the original signal. The delay depends on the OSC frequency and composite mix method.

4.2 H/V Frequency Counter

MTV112E can discriminate HSYNC/VSYNC frequency and saves the information in XFRs. The 15-bit Hcounter counts the time of the 64xHSYNC period, but only 11 upper bits are loaded into the HCNTH/HCNTL latch. The 11-bit output value is {2/H-Freq} / {1/OSC-Freq}, updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is not present. The 14-bit Vcounter counts the time between 2 VSYNC pulses, but only 9 upper bits are loaded into the VCNTH/VCNTL latch. The 9-bit output value is {1/V-Freq} / {512/OSC-Freq}, updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of the H/V counter overflow. The VFchg/HFchg interrupt is active when VCNT/HCNT value changes or overflows. Tables 4.2.1 and 4.2.2 show the HCNT/VCNT value under the operations of 8MHz and 12MHz.

4.2.1 H-Freq Table

H-Freq(KHZ)		Output Value (11 bits)	
		8MHz OSC (hex / dec)	12MHz OSC (hex / dec)
1	30	215h / 533	320h / 800
2	31.5	1FBh / 507	2F9h / 761
3	33.5	1DDh /477	2CCh / 716
4	35.5	1C2h / 450	2A4h / 676
5	36.8	1B2h / 434	28Ch / 652
6	38	1A5h / 421	277h / 631
7	40	190h / 400	258h / 600
8	48	14Dh / 333	1F4h / 500
9	50	140h / 320	1E0h / 480
10	57	118h / 280	1A5h / 421
11	60	10Ah / 266	190h / 400
12	64	0FAh / 250	177h / 375
13	100	0A0h / 160	0F0h / 240

*1. The H-Freq output (HF10 - HF0) is valid.
*2. The tolerance deviation is ± 1 LSB.

4.2.2 V-Freq Table

V-Freq(Hz)		Output Value (9 bits)	
		8MHz OSC (hex / dec)	12MHz OSC (hex / dec)
1	56.25	115h / 277	1A0h / 416
2	59.94	104h / 260	187h / 391
3	60	104h / 260	186h / 390
4	60.32	103h / 259	184h / 388
5	60.53	102h / 258	183h / 387
6	66.67	0EAh / 234	15Fh / 351
7	70.069	0DEh / 222	14Eh / 334
8	70.08	0DEh / 222	14Eh / 334
9	72	0D9h /217	145h / 325
10	72.378	0D7h / 215	143h / 323
11	72.7	0D6h / 214	142h / 322
12	87	0B3h / 179	10Dh / 269

*1. The V-Freq output (VF8 - VF0) is valid.
*2. The tolerance deviation is ± 1 LSB.

4.3 H/V Presence Check

The Hpresent function checks the input HSYNC pulse. The Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz. The Vpresent function checks the input VSYNC pulse. The Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz. A control bit "PREFS" selects the time base for these functions. The HPRchg interrupt is set when the Hpre value changes. The VPRchg interrupt is set when the Vpre/CVpre value changes. However, the CVpre flag interrupt may be disabled when S/W disables the composite function.

4.4 H/V Polarity Detection

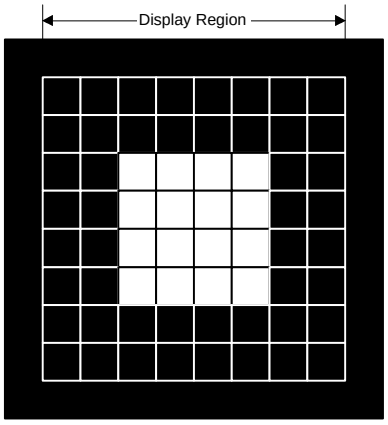
The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The HPLchg interrupt is set when the Hpol value changes. The VPLchg interrupt is set when the Vpol value changes.

4.5 Output HBLANK/VBLANK Control and Polarity Adjustment

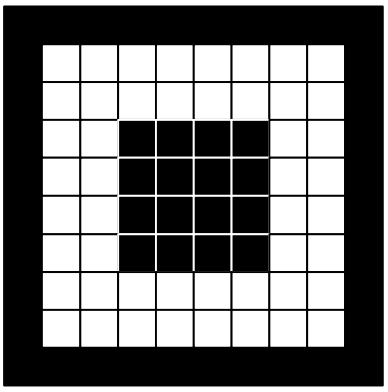
The HBLANK is the mux output of HSYNC and self-test horizontal pattern. The VBLANK is the mux output of VSYNC, CVSYNC and the self-test vertical pattern. The mux selection and output polarity are S/W controllable. The VBLANK output is cut off when VSYNC frequency is over 200Hz or 133Hz depends on 8MHz/12MHz OSC selection. The HBLANK/VBLANK shares the output pin with P4.1/ P4.0.

4.6 Self-Test Pattern Generator

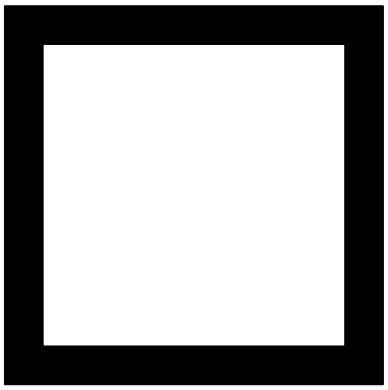
This generator can generate 4 display patterns for testing purposes: positive cross-hatch, negative cross-hatch, full white, and full black (shown in the following figure). It was originally designed to support the monitor manufacturer in performing a burn-in test, or to offer the end-user a reference to check the monitor. The generator's output STOUT shares the output pin with P4.2.



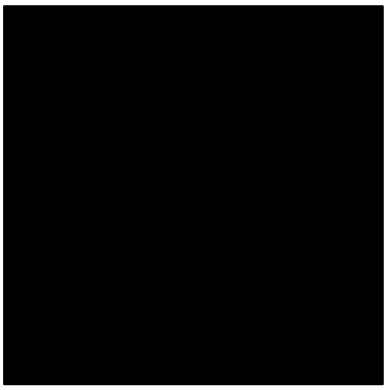
Positive Cross-Hatch



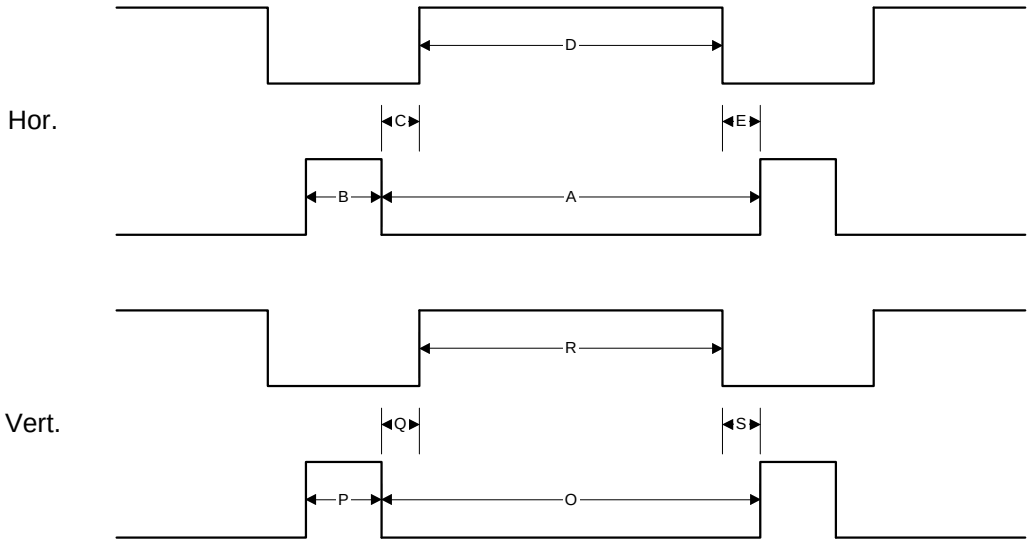
Negative Cross-Hatch



Full White



Full Black



MTV112E Self-Test Pattern Timing (8MHz)

	63.5KHz, 60Hz		31.7KHz, 60Hz	
	Absolute time	H dots	Absolute time	H dots
Hor. Total Time	Us(A)=15.75	1280	Us(A)=31.5	640
Hor. Acitve Time	Us(D)=12.05	979.3	Us(D)=24.05	488.6
Hor. F. P.	Us(E)=0.2	16.25	Us(E)=0.45	9
SYNC Pulse Width	Us(B)=1.5	122	Us(B)=3	61
Hor. B. P.	Us(C)=2	162.54	Us(C)=4	81.27
	V lines		V lines	
Hor. Total Time	Us(O)=16.6635	1024	Us(O)=16.6635	480
Hor. Active Time	Us(R)=15.6555	962	Us(R)=15.6555	451
Hor. F. P.	Us(S)=0.063	3.87	Us(S)=0.063	1.82
SYNC Pulse Width	Us(P)=0.063	3.87	Us(P)=0.063	1.82
Hor. B. P.	Us(Q)=0.882	54.2	Us(Q)=0.882	25.4

* 8 x 8 blocks of cross-hatch pattern in display region.

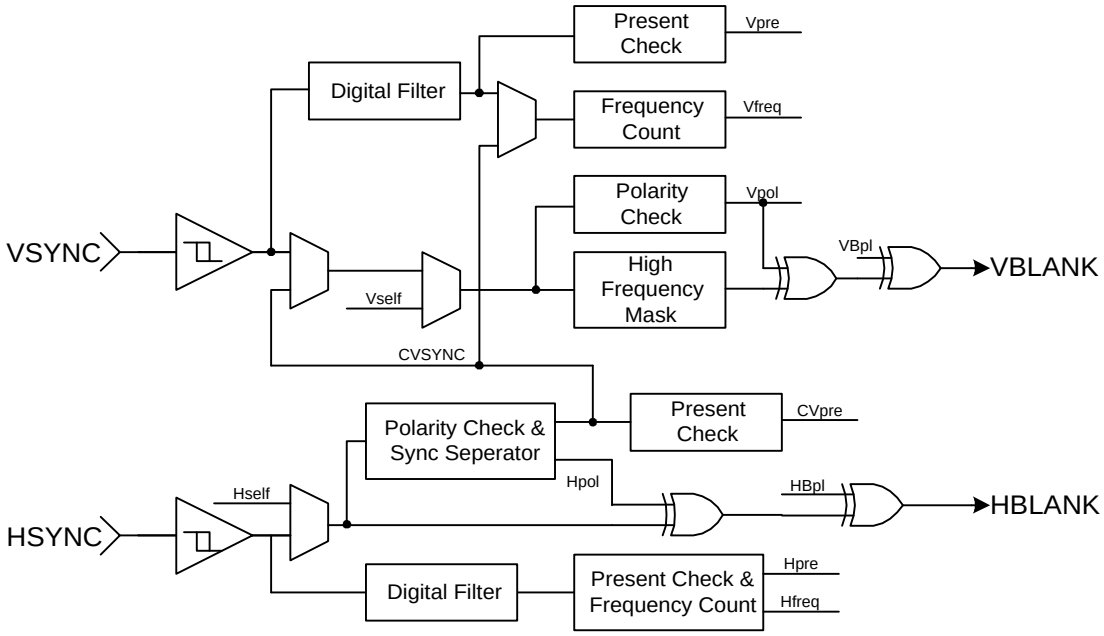
4.7 VSYNC Interrupt

MTV112E checks the VSYNC input pulse and generates an interrupt at its leading edge. The VSYNC1 flag is set each time MTV112E detects a VSYNC pulse.

4.8 H/V SYNC Processor Register

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PSTUS	40h (r)	CVpre	X	Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	41h (r)	Hovf	X	X	X	X	HF10	HF9	HF8
HCNTL	42h (r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	43h (r)	Vovf	X	X	X	X	X	X	VF8
VCNTL	44h (r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
PCTR0	40h (w)	C1	C0	HVsel	STOsel	PREFS	HALFV	HBpl	VBpl
PCTR2	42h (w)	X	X	X	Selft	STbsh	Rt1	Rt0	STF
P4OUT	44h (w)	X	X	X	X	X	P42	P41	P40
INTFLG	50h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg	FIFOI	MI

INTEN	60h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF	EFIFO	EMI
INTFLG	51h(r/w)	X	X	X	X	X	X	X	VSYNC
INTEN	61h(w)	X	X	X	X	X	X	X	EVSI



H/V SYNC Processor Block Diagram

PSTUS (r) : The status of polarity, presence and static level for HSYNC and VSYNC.

CVpre = 1 → The extracted CVSYNC is present.
= 0 → The extracted CVSYNC is not present.
H_{pol} = 1 → HSYNC input is positive polarity.
= 0 → HSYNC input is negative polarity.
V_{pol} = 1 → VSYNC (CVSYNC) is positive polarity.
= 0 → VSYNC (CVSYNC) is negative polarity.
H_{pre} = 1 → HSYNC input is present.
= 0 → HSYNC input is not present.
V_{pre} = 1 → VSYNC input is present.
= 0 → VSYNC input is not present.
H_{off}* = 1 → HSYNC input's off-level is high.
= 0 → HSYNC input's off-level is low.
V_{off}* = 1 → VSYNC input's off-level is high.
= 0 → VSYNC input's off-level is low.
*H_{off} and V_{off} are valid when H_{pre}=0 or V_{pre}=0.

HCNTH (r) : H-Freq counter's high bits.
Hovf = 1 → H-Freq counter overflows; this bit is cleared by H/W when condition removed.
HF10 - HF8 : 3 high bits of H-Freq counter.

HCNTL (r) : H-Freq counter's low bits.

VCNTH (r) : V-Freq counter's high bits.
Vovf = 1 → V-Freq counter overflows; this bit is cleared by H/W when condition removed.
VF8 : High bit of V-Freq counter.

VCNTL (r) : V-Freq counter's low bits.

PCTR0 (w) : SYNC processor control register 0.

C1, C0 = 1,1 → Selects CVSYNC as the polarity, Freq and VBLANK source.
= 1,0 → Selects VSYNC as the polarity, Freq and VBLANK source.
= 0,0 → Disables composite function (MTV012 compatible mode).
= 0,1 → H/W auto switches to CVSYNC when CVpre=1 and VSpre=0.

HVsel = 1 → Pin #16 is P4.1, pin #17 is P4.0.
= 0 → Pin #16 is HBLANK, pin #17 is VBLANK.

STOsel = 1 → Pin #29 is P4.2.
= 0 → Pin #29 is STOUT.

PREFS = 0 → Selects 8MHz OSC as H/V presence check and self-test pattern time base.
= 1 → Selects 12MHz OSC as H/V presence check and self-test pattern time base.

HALFV = 1 → VBLANK is half frequency output of VSYNC.

HB_{pl} = 1 → Negative polarity HBLANK output.
= 0 → Positive polarity HBLANK output.

VB_{pl} = 1 → Negative polarity VBLANK output.
= 0 → Positive polarity VBLANK output.

PCTR2 (w) : Self-test pattern generator control.

S_{elft} = 1 → Enables generator.
= 0 → Disables generator.

ST_{bsh} = 1 → 63.5KHz (horizontal) output selected.
= 0 → 31.75KHz (horizontal) output selected.

Rt1, Rt0= 0,0 → Positive cross-hatch pattern output.
= 0,1 → Negative cross-hatch pattern output.
= 1,0 → Full white pattern output.
= 1,1 → Full black pattern output.

STF = 1 → Enables STOUT output.
= 0 → Disables STOUT output.

P4OUT (w) : Port 4 data output value.

INTFLG (w) : Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enabler bit is set, the 8051 core's INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

HPRchg= 1 → No action.
= 0 → Clears HSYNC presence change flag.

VPRchg= 1 → No action.
= 0 → Clears VSYNC presence change flag.

HPLchg= 1 → No action.
= 0 → Clears HSYNC polarity change flag.

VPLchg= 1 → No action.
= 0 → Clears VSYNC polarity change flag.

HFchg = 1 → No action.
= 0 → Clears HSYNC frequency change flag.

VFchg = 1 → No action.
= 0 → Clears VSYNC frequency change flag.

VSYNCi= 1 → No action.
= 0 → Clears VSYNC interrupt flag.

INTFLG (r) : Interrupt flag.

HPRchg= 1 → Indicates an HSYNC presence change.

VPRchg= 1 → Indicates a VSYNC presence change.
HPLchg= 1 → Indicates a HSYNC polarity change.
VPLchg= 1 → Indicates a VSYNC polarity change.
HFchg = 1 → Indicates an HSYNC frequency change or counter overflow.
VFchg = 1 → Indicates a VSYNC frequency change or counter overflow.
VSYNCi= 1 → Indicates a VSYNC interrupt.

INTEN (w) : Interrupt enabler.
EHPR = 1 → Enables HSYNC presence change interrupt.
EVPR = 1 → Enables VSYNC presence change interrupt.
EHPL = 1 → Enables HSYNC polarity change interrupt.
EVPL = 1 → Enables VSYNC polarity change interrupt.
EHF = 1 → Enables HSYNC frequency change / counter overflow interrupt.
EVF = 1 → Enables VSYNC frequency change / counter overflow interrupt.
EVSI = 1 → Enables VSYNC interrupt.

5. DDC & IIC Interface

5.1 DDC1 Mode

MTV112E enters DDC1 mode after Reset. In this mode, VSYNC is used as a data clock. The HSCL pin should remain at high. The data output to the HSDA pin is taken from 8 bytes f FIFO in MTV112E. MTV112E fetches the data byte from FIFO, then sends it in a 9-bit packet format which includes a null bit (=1) as packet separator. The software program should load EDID data (original stored in EEPROM) into FIFO and take care of the FIFO depth. FIFO sets the FIFOI (FIFO low interrupt) flag when there are fewer than N (N=2,3,4 or 5 controlled by LS1, LS0) bytes to be output to the HSDA pin. To prevent FIFO from emptying, software needs to write EDID data to FIFO as soon as FIFOI is set. On the other hand, FIFO sets the FIFOH flag when its capacity is full. Software should not write additional data to FIFO in such instance. The FIFOI interrupt can be masked or enabled by an EFIFO control bit. A simple way to control FIFO is to set (LS1, LS0=1,0) and enable FIFOI interrupt, then software may load 4 bytes into FIFO each time a FIFOI interrupt arises. A special control bit "LDFIFO" can reduce the software effort when EDID data is stored in EEPROM. If LDFIFO=1, FIFO will be automatically loaded with MBUF data when software reads MBUF XFR.

5.2 DDC2B Mode

MTV112E switches to DDC2B mode when it detects a high to low transition on the HSCL pin. Once MTV112E enters DDC2B mode, the host can access the EEPROM using IIC bus protocol as if the HSDA and HSCL are directly bypassed to ISDA and ISCL pins. MTV112E will return to DDC1 mode if HSCL is kept high for a 128 VSYNC clock period. However, it will lock in DDC2B mode if a valid IIC access has been detected on HSCL/HSDA bus. The DDC2 flag reflects the current DDC status. S/W may clear it by setting CLRDDC. Control bits M128/M256 are used to block the EEPROM write operation from the host if the address is over 128/256.

5.3 Master Mode IIC Function Block

The master mode IIC block is connected to the ISDA and ISCL pins. Its speed can be set to 100kHz or 400kHz by s/w setting the IICF control bit. The software program can access the external EEPROM through this interface. Since the EDID/VDIF data and display information share the common EEPROM, precaution must be taken to avoid bus conflict. In DDC1 mode, the IIC interface is controlled by MTV112E only. In DDC2B mode, the host may access the EEPROM directly. Software can test the HSCL condition by reading the BUSY flag, which is set in case HSCL=0. A summary of master IIC access is illustrated as follows:

5.3.1. To Write EEPROM

1. Write the EEPROM slave address to MBUF (bit 0 = 0).
2. Set the S bit to Start.
3. After MTV112E transmits this byte, an MI interrupt will be triggered.
4. The program can write MBUF to transfer the next byte or set the P bit to Stop.

* Please see the attachments about "Master IIC Transmission Timing".

5.3.2. To Read EEPROM

1. Write the slave address to MBUF (bit 0 = 1).
2. Set the S bit to Start.
3. After MTV112E transmits this byte, a MI interrupt will be triggered.
4. Set or reset the ACK flag according to the IIC protocol.
5. Read out the useless byte to MBUF to continue the data transfer.
6. After MTV112E receives a new byte, the MI interrupt is triggered again.
7. Reading MBUF also triggers the next receiving operation, but setting the P bit before reading can terminate the operation.

* Please see the attachments about "Master IIC Timing Receiving".

5.4 Slave Mode IIC Function Block

The slave mode IIC block can be connected to HSDA/HSCL or ISDA/ISCL pins, and selected by the SLVsel control bit. This block can receive/transmit data using the IIC protocol. S/W may set the SLVADR register to determine which slave address the block should respond to.

In receiving mode, the block first detects an IIC slave address match condition then issues a SLVMI interrupt. The data received from SDA is shifted into a shift register and written to the RCBUF latch. The first byte loaded is the word address (slave address is dropped). This block also generates an RCBI (Receive Buffer full Interrupt) each time the RCBUF is loaded. If S/W can't read out the RCBUF in time, the next byte will not be written to RCBUF and the slave block will return NACK to the master. This feature guarantees the data integrity of communication. A WADR flag can tell S/W if the data in RCBUF is a word address.

In transmission mode, the block first detects an IIC slave address match condition then issues a SLVMI. In the meantime, the data pre-stored in the TXBUF is loaded into the shift register, results in TXBUF emptying and generates a TXBI (Transmission Buffer Interrupt). S/W should write the TXBUF a new byte for the next transfer before the shift register empties. Failure to do this will cause data corruption. The TXBI occurs each time the shift register receives new data from TXBUF. The SLVMI is cleared by writing the SLVSTUS register. The RCBI is cleared by reading the RCBUF. The TXBI is cleared by writing the TXBUF.

If the control bit ENSCL is set, the block will hold SCL low until the RCBI/TXBI is cleared.

*Please see the attachments about "Slave IIC Block Timing".

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MCTR	00h (w)	LS1	LS0	LDFIFO	M256	M128	ACK	P	S
MSTUS	00h (r)	X	SCLERR	DDC2	BERR	HFREQ	FIFOH	FIFOL	BUSY
MBUF	10h (r/w)	MBUF7	MBUF6	MBUF5	MBUF4	MBUF3	MBUF2	MBUF1	MBUF0
INTFLG	50h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg	FIFOI	MI
INTEN	60h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF	EFIFO	EMI
FIFO	70h (w)	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
SLVCTR	90h (w)	ENSLV	SLVsel	ERCBI	ESLVMI	ETXBI	ENSCL	X	X
SLVSTUS	91h (r)	WADR	SLVS	RCBI	SLVMI	TXBI	RWB	ACKIN	X
SLVSTUS	91h (w)	Write to clear SLVMI							
RCBUF	92h (r)	RCbuf7	RCbuf6	RCbuf5	RCbuf4	RCbuf3	RCbuf2	RCbuf1	RCbuf0
TXBUF	92h (w)	TXbuf7	TXbuf6	TXbuf5	TXbuf4	TXbuf3	TXbuf2	TXbuf1	TXbuf0
SLVADR	93h (w)	SLVadr7	SLVadr6	SLVadr5	SLVadr4	SLVadr3	SLVadr2	SLVadr1	X

MCTR (w) : Master IIC interface control register.

LS1, LS0	= 11	→ FIFOL is the status in which FIFO depth < 5.
	= 10	→ FIFOL is the status in which FIFO depth < 4.
	= 01	→ FIFOL is the status in which FIFO depth < 3.
	= 00	→ FIFOL is the status in which FIFO depth < 2.
LDFIFO	= 1	→ FIFO will be written while S/W reads MBUF.
M256	= 1	→ Disables host writing EEPROM when address is over 256.
M128	= 1	→ Disables host writing EEPROM when address is over 128.

ACK	= 1	→ In receiving mode, no acknowledgment is given by MTV112E.
	= 0	→ In receiving mode, ACK is returned by MTV112E.
S, P	= ↑, 0	→ Start condition when Master IIC is not transferring.
	= X, ↑	→ Stop condition when Master IIC is not transferring.
	= 1, X	→ Will resume transfer after a read/write MBUF operation.
	= X, 0	→ Forces HSCL low and occupies the IIC bus.

* MTV112E uses a 100KHz clock to sample the S/P bit; any pulse should sustain at least 20us.
* A write/read MBUF operation can be recognized only after 10us of the MI flag's rising edge.

MSTUS (r) : Master IIC interface status register.

SCLERR	= 1	→ The ISCL pin has been pulled low by other devices during the transfer, cleared when S=0.
DDC2	= 1	→ DDC2B is active.
	= 0	→ MTV112E remains in DDC1 mode.
BERR	= 1	→ IIC bus error, no ACK received from the slave, updated each time the slave sends ACK on the ISDA pin.
HFREQ	= 1	→ MTV112E has detected a higher than 200Hz clock on the VSYNC pin.
FIFOH	= 1	→ FIFO high indicated.
FIFOL	= 1	→ FIFO low indicated.
BUSY	= 1	→ Host drives the HSCL pin to low.

* While writing FIFO, the FIFOH/FIFOL flag will reflect the FIFO condition after 30us.

MBUF (w) : Master IIC data shift register, after START and before STOP condition, write this register will resume MTV112E's transmission to the IIC bus.

MBUF (r) : Master IIC data shift register, after START and before STOP condition, read this register will resume MTV112E's receiving from the IIC bus.

INTFLG (w) : Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enabler bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

FIFOI	= 1	→ No action.
	= 0	→ Clears FIFOI flag.
MI	= 1	→ No action.
	= 0	→ Clears Master IIC bus interrupt flag (MI).

INTFLG (r) : Interrupt flag.

FIFOI	= 1	→ Indicates the FIFO low condition; when EFIFO is set, MTV112E will be interrupted by INT1.
MI	= 1	→ Indicates when a byte is sent/received to/from the IIC bus; when EME is active, MTV112E will be interrupted by INT1.

INTEN (w) : Interrupt enabler.

EFIFO	= 1	→ Enables FIFO interrupt.
EMI	= 1	→ Enables Master IIC bus interrupt.

FIFO (w) : Writes FIFO contents.

SLVCTR (w) : Slave IIC block control.

ENSLV	= 1	→ Enables slave IIC block.
	= 0	→ Disables slave IIC block.
SLVsel	= 1	→ Slave IIC connects to ISDA/ISCL.
	= 0	→ Slave IIC connects to HSDA/HSCL.
ERCBI	= 1	→ Enables slave receiving buffer interrupt.
ESLVMI	= 1	→ Enables slave address match interrupt.

ETXBI = 1 → Enables slave transmission buffer interrupt.
ENSCL = 1 → Enables slave block to hold SCL pin low.

SLVSTUS (r) : Slave IIC block status.

WADR = 1 → The data in SLVBUF is a word address.
SLVS = 1 → The slave block has detected a START; cleared when STOP detected.
RCBI = 1 → RCBUF has loaded a new data byte; reset by S/W reading RCBUF.
SLVMI = 1 → The slave block has detected the slave address match condition; cleared by S/W writing SLVSTUS.
TXBI = 1 → TXBUF is empty; reset by S/W writing TXBUF.
RWB = 1 → Current transfer is slave transmitting.
= 0 → Current transfer is slave receiving.
ACKIN = 1 → Master responds to NACK.

SLVSTUS (w) : Clears SLVMI flag.

RCBUF (r) : Slave IIC receives data buffer.

TXBUF (w) : Slave IIC transmits data buffer.

SLVADR (w) : Slave IIC address to which the slave block should respond.

6. Low Power Reset (LVR) & Watchdog Timer

When the voltage level of the power supply is below 4.0V for a specific time, the LVR will generate a chip resetting signal. After the power supply is above 4.0V, LVR maintains the reset state for 144 Xtal cycles to guarantee the chip exit reset condition has a stable Xtal oscillation. The specific time of power supply in a low level is 3us and is adjustable by an external capacitor connected to the RST pin.

The watchdog timer automatically generates a device reset when it overflows. The interval of overflow is 0.25 sec x N, in which N is a number from 1 to 8, and can be programmed via register WDT (2:0). The timer function is disabled after power-on reset. The user can activate this function by setting WEN and clear the timer by setting WCLR.

7. A/D Converter

MTV112E is equipped with two 4-bit A/D converters. Each can be enabled/disabled by S/W control. The refresh rate for the ADC is OSC freq./6144. The ADC compares the input pin voltage with the internal VDD*N/16 voltage (in which N = 0 -16). The ADC output value is N when the pin voltage is greater than VDD*N/16 and smaller than VDD*(N+1)/16.

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADC	A0h (w)	ENADC	X	X	X	X	X	EADC1	EADC0
ADC	A0h (r)	AD1b3	AD1b2	AD1b1	AD1b0	AD0b3	AD0b2	AD0b1	AD0b0
WDT	80h (w)	WEN	WCLR	CLRDDC	DIV253		WDT2	WDT1	WDT0

WDT (w) : Watchdog timer control register.

WEN = 1 → Enables watchdog timer.
WCLR = 1 → Clears watchdog timer.
CLRDDC = 1 → Clears DDC2 flag.
WDT2: WDT0 = 0 → Overflow interval = 8 x 0.25 sec.
= 1 → Overflow interval = 1 x 0.25 sec.
= 2 → Overflow interval = 2 x 0.25 sec.
= 3 → Overflow interval = 3 x 0.25 sec.

= 4 → Overflow interval = 4 x 0.25 sec.
= 5 → Overflow interval = 5 x 0.25 sec.
= 6 → Overflow interval = 6 x 0.25 sec.
= 7 → Overflow interval = 7 x 0.25 sec.

ADC (w) : ADC control.
ENADC = 1 → Enables ADC.
EADC1 = 1 → Enables ADC1 pin input.
EADC0 = 1 → Enables ADC0 pin input.

ADC (r) : ADC conversion result.
ADC1b3: ADC1b0 ADC1 conversion result.
ADC0b3: ADC0b0 ADC0 conversion result.

4.0 Test Mode Condition

In normal applications, users should keep MTV112E from entering its test/program mode, outlined as follows:
Test Mode A: RESET=1 & DA9=1 & DA8=0 & STO=0
Test Mode B: RESET falling edge & DA9=1 & DA8=0 & STO=1
Program Mode: RESET=1 & DA9=0 & DA8=1

5.0 INTERNAL EPROM

To program the internal EPROM, MTV112E must be running at a 4 to 6 MHz cycle time. The address of the EPROM location to be programmed is applied to Port 1(A0 - A7) and pins P2.0 - P2.6 (A8 - A14) of Port 2, while the code byte to be programmed is applied to DA0 - DA7. All other pins should be held at the level indicated in the following table:

Mode	RST	DA9	STOUT	DA8	P2.7	P3.2	p3.1	p3.0
Normal Reset	1	1	0	1	X	X	X	X
Program Code Data	1	0	P*	VPP	1	0	1	1
Program Lock Bit	1	0	P*	VPP	1	1	1	1
Code Verification	1	0	1	1	0	0	1	1

Note 1: VPP = 12.7V
Note 2: P* is pulsed low for 100uS for programming.

6.0 ELECTRICAL PARAMETERS

6.1 Absolute Maximum Ratings

at: Ta= 0 to 70 ^{o}C, VSS=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to +6.0	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	^{o}C
Maximum Storage Temperature	Tstg	-25 to +125	^{o}C

6.2 Allowable Operating Conditions

at: Ta= 0 to 70 ^{o}C, VSS=0V

Name	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	4.0	6.0	V
Input "H" Voltage	Vih1	0.4 x VDD	VDD +0.3	V
Input "L" Voltage	Vil1	-0.3	0.15 x VDD	V
Operating Freq.	Fopg	-	15	MHz

6.3 DC Characteristics

at: Ta=0 to 70 ^{o}C, VDD=4.0V ~ 6.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Output "H" Voltage, except open-drain pins: pin #s 16, 17, 29	Voh1	Ioh=-50uA	4			V
Output "H" Voltage, pin #s 16, 17, 29	Voh2	Ioh=-1mA	4			V
Output "L" Voltage	Vol	Iol=8mA			0.45	V
Power Supply Current	Idd	Active		18	24	mA
		Idle		1.3	4.0	mA
		Power-Down		50	80	uA
RST Pull-Down Resistor	Rrst	VDD=5V	50		150	Kohm
Pin Capacitance	Cio				15	pF

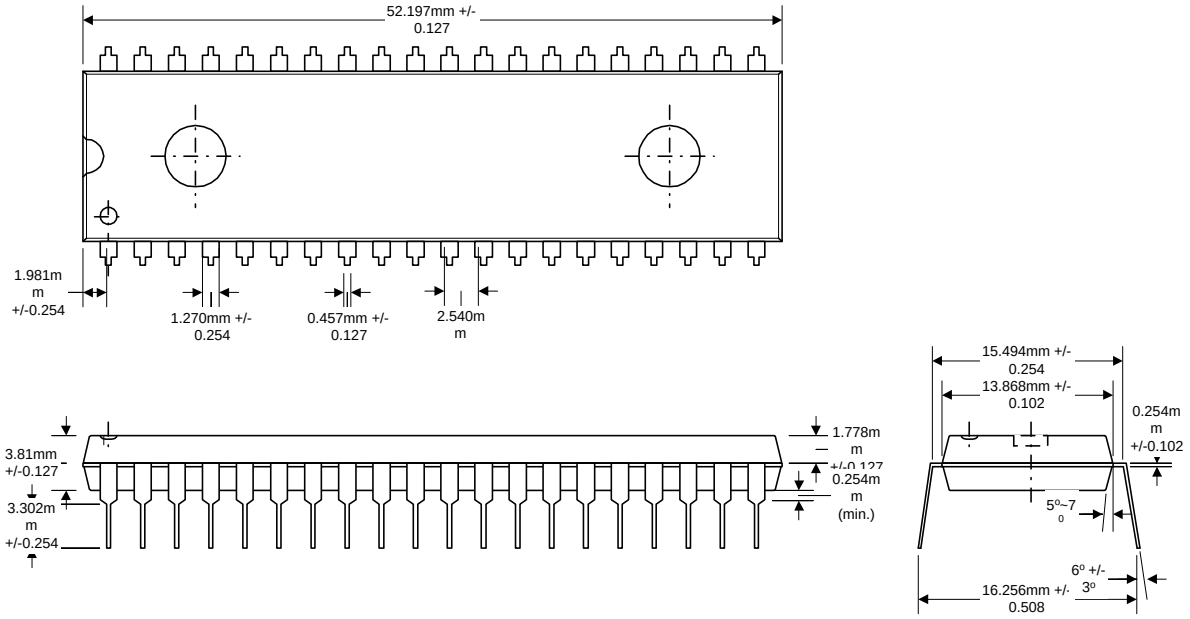
6.4 AC Characteristics

at: Ta=0 to 70 ^{o}C, VDD=4.0V ~ 6.0V, VSS=0V

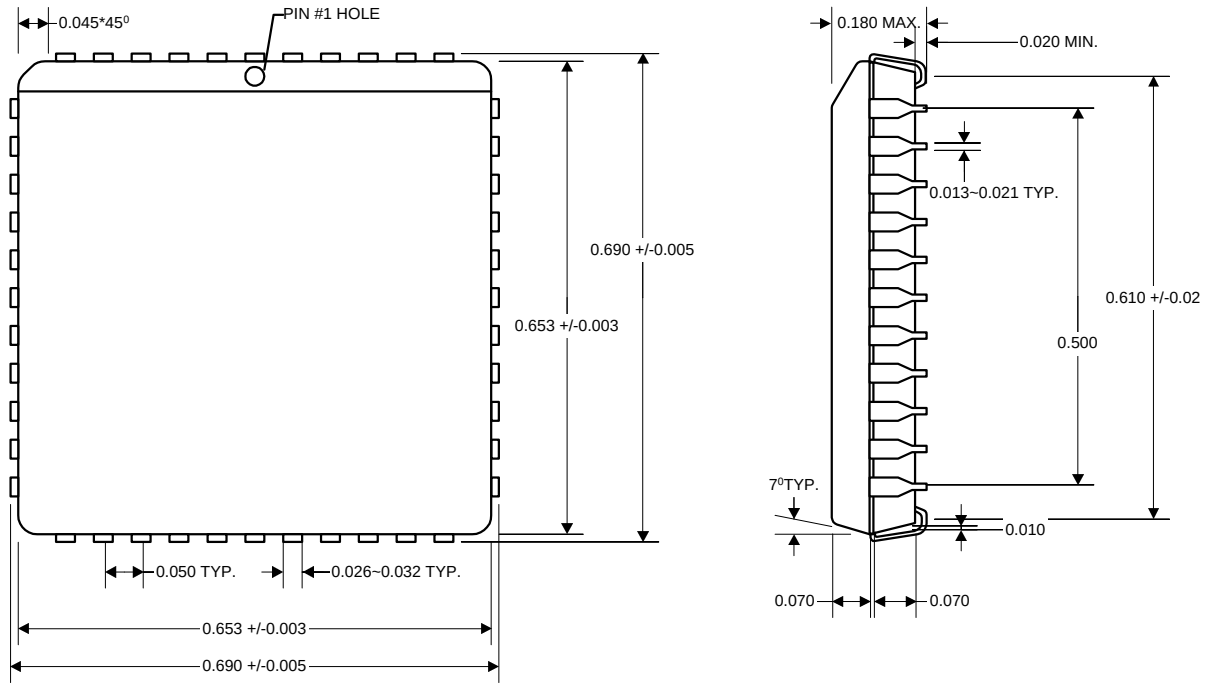
Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			8		MHz
PWM DAC Frequency	fDA	fXtal=8MHz	31.25		31.62	KHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		47.43	KHz
HS Input Pulse Width	tHIPW	fXtal=8MHz	0.3		12	uS
VS Input Pulse Width	tVIPW	fXtal=8MHz	3			US
HS Input Pulse Width	tHIPW	fXtal=12MHz	0.2		8	US
VS Input Pulse Width	tVIPW	fXtal=12MHz	2			US
HSYNC to HBLANK Output Jitter	tHHBJ				5	NS
H+V to VBLANK Output Delay	tVVBD	fXtal=8MHz		16		uS
H+V to VBLANK Output Delay	tVVBD	fXtal=12MHz		10		uS
VS Pulse Width in H+V Signal	tVCPW	fXtal=8MHz	32			uS
VS Pulse Width in H+V Signal	tVCPW	FXtal=12MHz	20			uS

7.0 PACKAGE DIMENSION

7.1 40-pin PDIP 600 mil



7.2 44-pin PLCC unit: inch



8.0 Ordering Information

Standard configurations:

Prefix	Part Type	Package Type	Other Information
MTV	112	N: PDIP V: PLCC	Mask or OTP

Part Numbers: