MYSON TECHNOLOGY

MTV24C16/
MTV24LC16

16384-Bit Serial EEPROM

FEATURES

- State- of- the- Art Architecture
  - Non-volatile data storage
  - Standard Voltage and Low Voltage Operation
    5.0(Vcc = 4.5V to 5.5V) for 24C16
    3.0(Vcc = 2.7V to 5.5V) for 24LC16

- 2 wire I^2C serial interface
  - Provides bi-directional data transfer protocol

- Software Write Protection
  - Programmable security bit
  - Vcc level verification before self-time programmable cycle

- 16 bytes page write mode
  - Minimizes total write time per word

- Self-timed write-cycle(including auto-erase)

- Durable and Reliable
  - 40 years data retention after 1KK write/erase cycles
  - Minimum of 1000,000 write/erase cycles per word
  - Unlimited read cycles
  - ESD protection

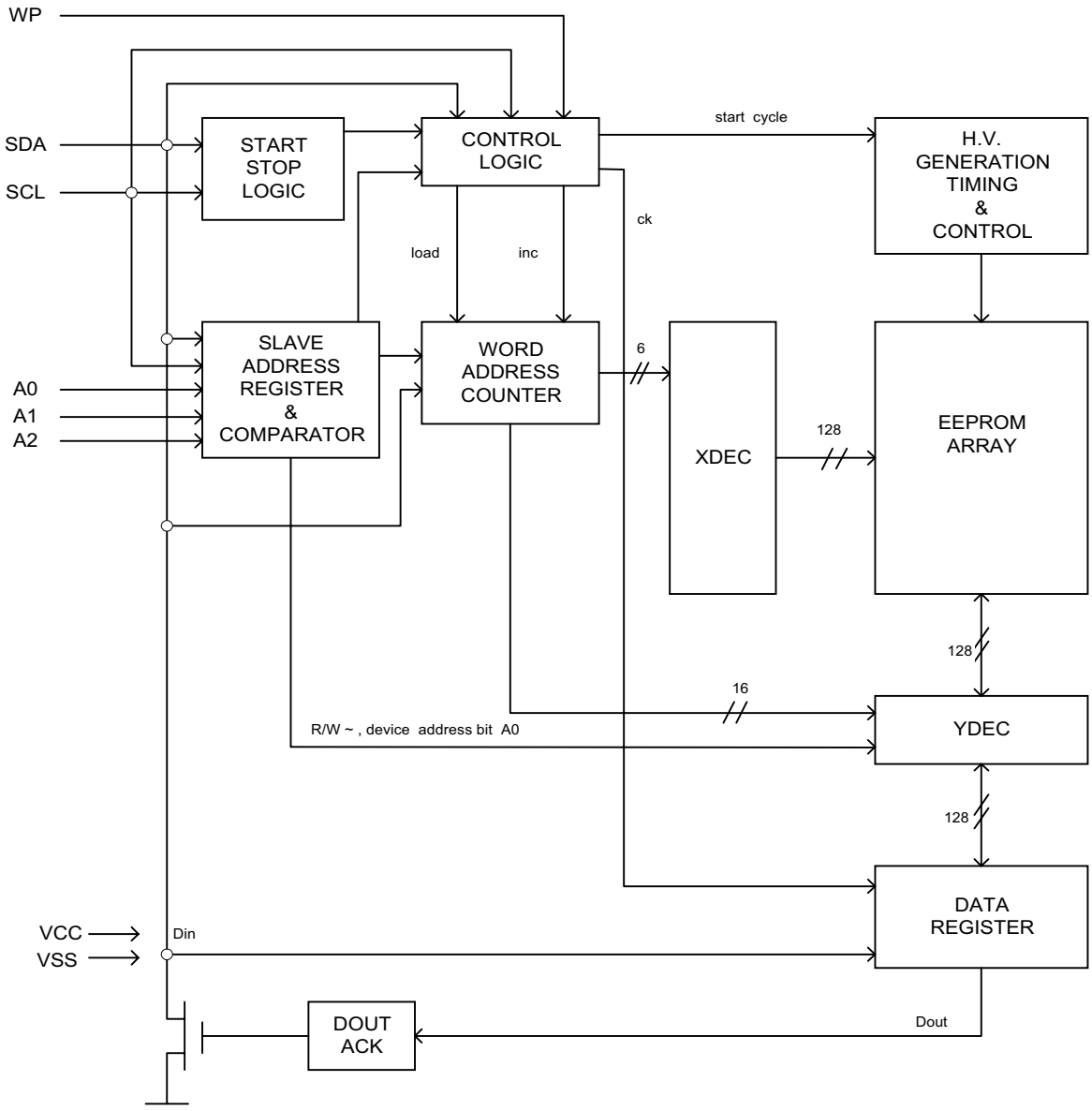
- Low standby current

GENERAL DESCRIPTION

The 24C16/24LC16 is a low cost, non-volatile, 16384-bit serial EEPROM with enhanced security device and conforms to all specifications in I^2C 2 wire protocol. The whole memory can be disabled (Write Protected) by connecting the WP pin to Vcc. This section of memory then becomes unalterable unless WP is switched to Vss. It is enhanced with security function. Every word of the memory has a programmable security bit to permit whether it can be altered or not. The 24C16/24LC16's communication protocol uses CLOCK(SCL) and DATA I/O(SDA) lines to synchronously clock data between the master (for example a microcomputer)and the slave EEPROM devices(s) .In addition, the bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the family in 2K, 4K, 8K, 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

MYSON EEPROMs are designed and tested for application requiring high endurance, high reliability, and low power consumption.

BLOCK DIAGRAM



PIN DESCRIPTIONS

SERIAL CLOCK (SCL)
The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)
SDA is a bidirection pin used to transfer data or security bit into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. Thus, the SDA bus requires a pull-up resistor to Vcc (typical 4.7KΩ for 100KHZ, 1KΩ for 400KHZ)

DEVICE ADDRESS INPUTS (A0, A1, A2)
The following table (Table A) shows the active pins across the 24C/LCXX device family.
TABLE A

Device	A0	A1	A2
24C02/24LC02	ADR	ADR	ADR
24C04/24LC04	XP	ADR	ADR
24C08/24LC08	XP	XP	ADR
24C016/24LC016	XP	XP	XP

ADR indicates the device address pin.

XP indicates that device address pin don't care but refers to an internal PAGE BLOCK memory segment.

WRITE PROTECTION (WP)
If WP is connected to Vcc, PROGRAM operation onto the whole memory will not be executed. READ operations are possible. If WP is connected to Vss, normal memory operation is enabled, READ/WRITE over the entire memory is possible.

1.0 FUNCTIONAL DESCRIPTION

1.1 APPLICATIONS

MYSON's electrically erasable programmable read only memories (EEPROMs) offer valuable security features including write protect function , two write modes ,three read modes, and a wide variety of memory size. Typical applications for the I^2C bus and 24XC0XX memories are included in SANs(small-area-networks), stereos, televisions, automobiles and other scaled-down systems that don't require tremendous speeds but instead cost efficiency and design simplicity.

1.2 ENDURANCE AND DATA RETENTION

The 24C16/24LC16 is designed for applications requiring up to 100,000 programming cycles (BYTE WRITE and PAGE WRITE). It provides 10 years of secure data retention, without power after the execution of 100,000 programming cycles.

1.3 DEVICE OPERATION

The 24C16/24LC16 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the 24C16/24LC16 is considered a slave in all applications.

Clock And Data Conventions
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. (Shown in Figures 1 and 2)

Start Condition
A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition. (Shown in Figure 2)

Stop Condition
A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition. (Shown in Figure 2)

Acknowledge
Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit. The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition. (Shown in Figure 3)

Devices Addressing
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C16/24LC16, 3-bit device address (A2 A1 A0) and 1-bit value indicating the read or write mode. All I^2C EEPROMs use and internal protocol that defines a PAGE BLOCK size of 8K bits. The 24C16/24LC16 contains two 2K-bits PAGE BLOCK, and the device address bit A0 is used for determinating which PAGE BLOCK of memory segment the read/write operation will be proceeded in. The eighth bit of slave address determines if the master device wants to read or write to the 24C16/24LC16. (Refer to table B).

The 24C16/24LC16 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

TABLE B

Operation	Control Code	Chip Select	R/W
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0

A0, A1, A2 is used to access page blocks , size of 8K bits, in the 24C16/24LC16

WRITE OPERATIONS

Byte Write
Following the start signal from the master, the slave address is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle.

Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C16/24LC16. After receiving another acknowledge signal from the 24C16/24LC16 the master device will transmit the data word to be written into the addressed memory location. The 24C16/24LC16 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this period the 24C16/24LC16 will not generate acknowledge signals. (Shown in Figure 4)

Page Write
The write control byte, word address and the first data byte are transmitted to the 24C16/24LC16 in the same way as in a byte write. But instead of generating a stop condition the master transmit up to four data bytes to the 24C16/24LC16 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the two lower order address pointer bits are internally incremented by one. The higher order six bits of the word address remains constant. If the master should transmit more than four words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (Shown in Figure 5).

Acknowledge Polling
Since the device will not acknowledge during a write cycle , this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughout). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle , then no ACK will returned. If the cycle is complete then the device will return the ACK and the master can then proceed with the next read or write commands.

Write Protection
Programming will not take place if the WP pin of the 24C16/24LC16 is connected to Vcc. The 24C16/24LC16 will accept slave and byte addresses; but if the memory accessed is write protected by the WP pin, the 24C16/24LC16 will not generate an acknowledge after the first byte of data has been received, and thus the programming cycle will not be started when the stop condition is asserted.

READ OPERATIONS
Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read
The 24C16/24LC16 contains an address counter that maintains the address of the last accessed word, internally incremented by one. Therefore if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to one, the 24C16/24LC16 issues an acknowledge and transmits the eight bit data word . The master will not acknowledge the transfer but does generate a stop condition and the 24C16/24LC16 discontinues transmission. (Shown in Figure 6)

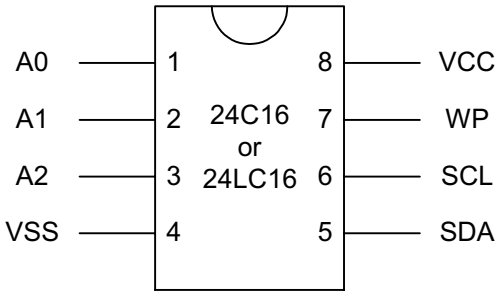
Random Read
Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C16/24LC16 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with R/W bit set to a one. The 24C16/24LC16 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C16/24LC16 discontinues transmission. (Shown in Figure 7)

Sequential Read
Sequential read is initiated in the same way as a random read except that after the 24C16/24LC16 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C16/24LC16 to transmit the next sequentially addressed 8 bit word (Shown in Figure 8). To provide sequential read the 24C16/24LC16 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire Page Block (8K bits) memory contents to be serially read during one operation. For example, if the current address is “011111111”, then the next address will be “000000000”, if the current address is “111111111” then the next address will be “100000000”.

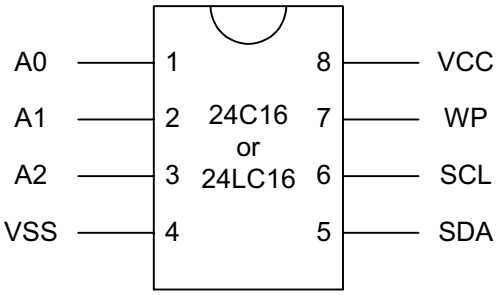
Security Consideration
The 24C16/24LC16 has the ability of protecting accidental modication to data of the entire part. Each programming operation(BYTE WRITE and PAGE WRITE for data and security) must satisfy three conditions before users initiate self-timed programming cycle. The first is that Vcc value must exceed a lock-out value which can be adjusted by Analog Technology, Inc.

Noise Protection
The 24C16/24LC16 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at normal conditions.
The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

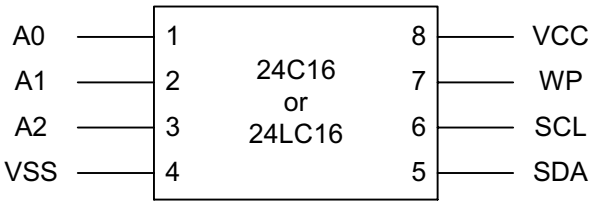
2.0 CONNECTION DIAGRAM



Dual-In-Line package



SO package (M8)



TSSOP

Pin Name

A0, A1, A2	N.C.
Vss	Ground
SDA	Data I/O
SCL	Clock input
WP	Write Protect
Vcc	+ 5 V or + 3 V

3.0 ABSOLUTE MAXIMUM RATINGS

Storage Temperature.....-65°C to + 125°C
Voltage with Respect to Ground.....-0.3 to + 6.5 V

NOTE: These are STRESS rating only. Appropriate conditions for operating these devices given elsewhere may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

4.0 OPERATING CONDITIONS

Temperature under bias: 24C16/24LC16.....0°C to + 70°C
24C16/24LC16-I.....-40°C to + 85°C

5.0 ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS
(Vcc =5V +/- 10% ,24C16/24LC16；Vcc =3V +/- 10% ,24LC16)

Symbol	Parameter	Conditions	24C16/ 24LC16		24LC16		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current (Program)	SCL = 100KHZ CMOS Input Levels	—	10	—	8	mA
I_{CC2}	Operating Current (Read)	SCL = 100KHZ CMOS Input Levels	—	1	—	1	mA
I_{SB}	Standby Current	SCL = SDA = 0 V	—	1	—	1	μA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}	-1	+1	-1	+1	μA
I_{OL}	Output Leakage	V_{OUT} = 0 V to Vcc	-1	+1	-1	+1	μA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.15 V_{CC}	V
V_{IH}	Input High Voltage		2	V_{CC} +0.2	0.8V_{CC}	V_{CC}+0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL	—	0.4	—	0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400uA TTL	2.4	—	2.4	—	V
V_{OL2}	Output Low Voltage	I_{OL} = 10uA CMOS	—	0.2	—	0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10uA CMOS	V_{CC}-0.2	—	V_{CC}-0.2	—	V
V_{LK}	V_{CC} Lockout Voltage	Programming Command Can Be Executed	Default	—	Default	—	V

6.0 SWITCHING CHACTERISTICS (Under Operating Conditions)

AC ELECTRICAL CHARACTERISTICS
(Vcc =5V +/- 10% , 24C16；Vcc =3V +/- 10% ,24LC16)
(Vcc =5V +/- 10% , 24C16 Fast Mode)

Parameter	Symbol	24C16/ 24LC16		24C16 (Fast Mode)		Units
		Min	Max	Min	Max	
Clock frequency	Fscl	0	100	—	400	kHz
Clock high time	Thigh	4000	—	600	—	ns
Clock low time	Tlow	4700	—	1200	—	ns
SDA and SCL rise time	Tr	—	1000	—	300	ns
SDA and SCL fall time	Tf	—	300	—	300	ns
START condition hold time	Thd:Sta	4000	—	600	—	ns
START condition setup time	Tsu:Sta	4700	—	600	—	ns
Data input hold time	Thd:Dat	0	—	0	—	ns
Data input setup time	Tsu:Dat	250	—	100	—	ns
STOP condition setup time	Tsu:Sto	4000	—	600	—	ns
Output valid from clock	Taa	300	3500	100	900	ns
Bus free time	Tbuf	4700	—	1200	—	ns
Data out hold time	Tdh	300	—	50	—	ns
Input filter spike suppression (SDA and SCL pins)	Tsp	—	100	—	50	ns
Write cycle time	Twr	—	10	—	10	ms

CAPACITANCE TA= 25°C , f=250KHZ

Symbol	Parameter	Max	Units
C_{OUT}	Output capacitance	5	pF
C_{IN}	Input capacitance	5	pF

A.C. Conditions of Test

Input Pulse Levels	Vcc x 0.1 to Vcc x 0.9
Input Rise and Fall times	10 ns
Input and Output Timming level	Vcc x 0.5
Output Load	1 TTL Gate and CL = 100pf

7.0TIMING DIAGRAM

BUS TIMING

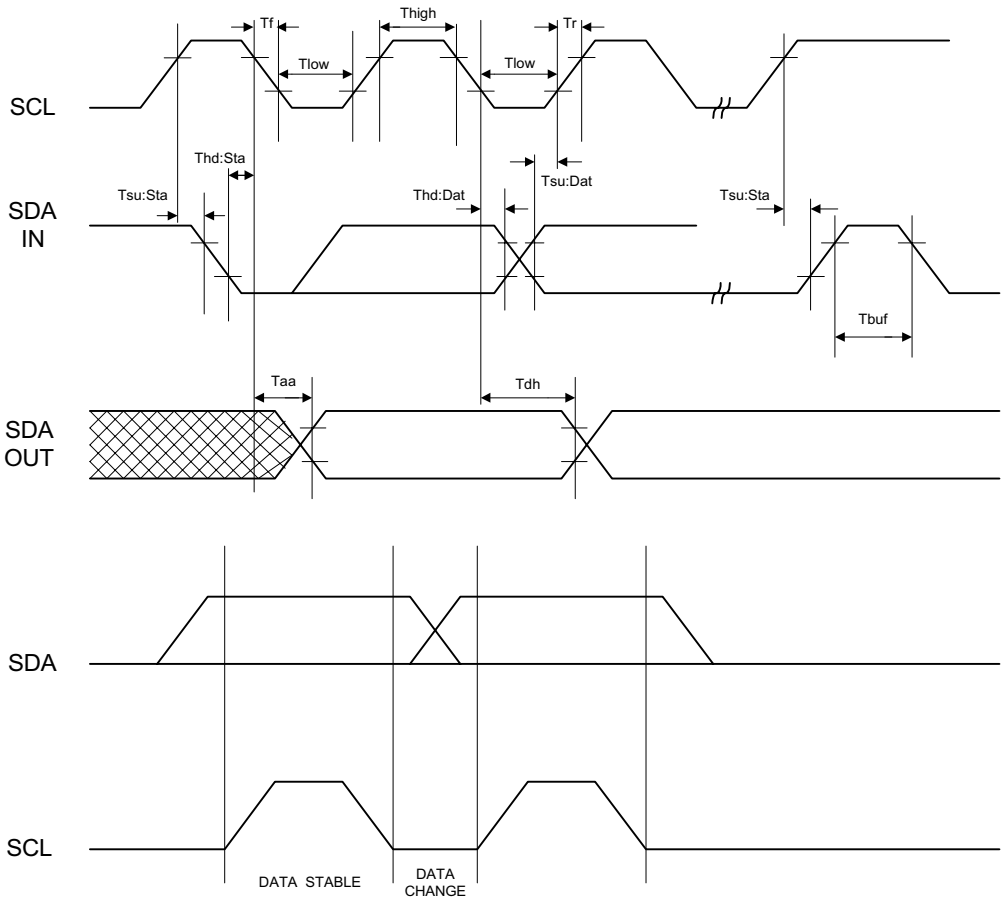


Figure 1. Data Validity

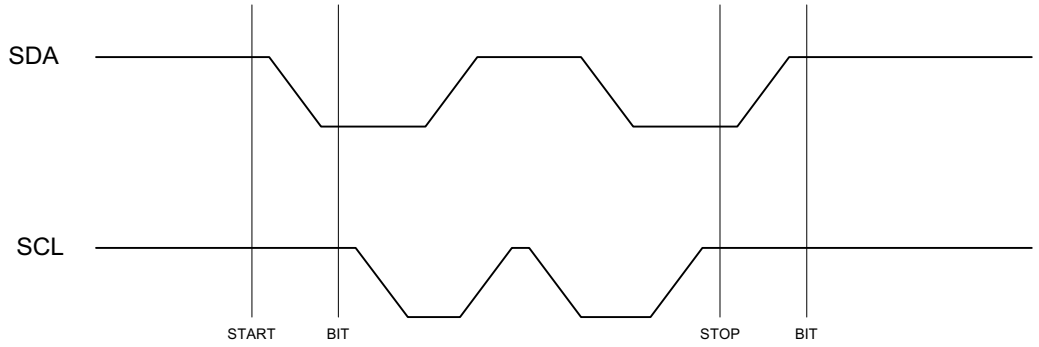


Figure 2. Definition of Start and Stop

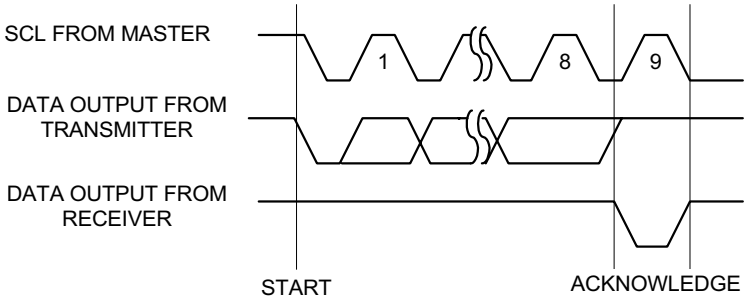


Figure 3. Acknowledge Response from Receiver

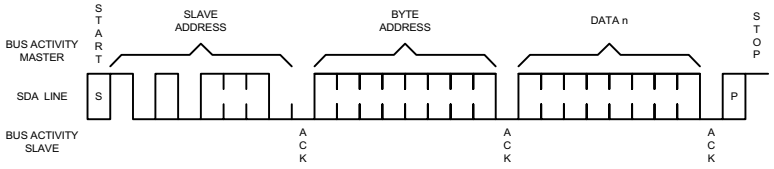


Figure 4. Byte Write for Data

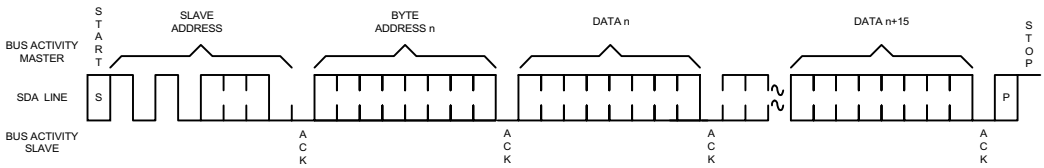


Figure 5. Page Write for Data

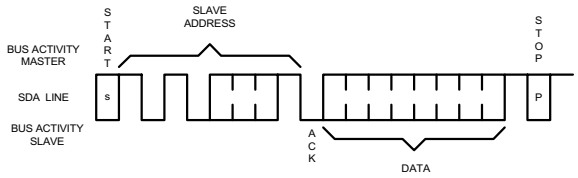


Figure 6. Current Address Read for Data

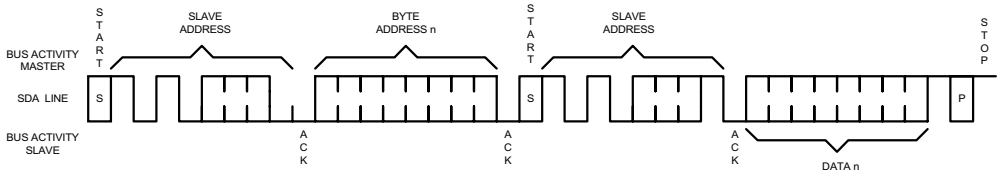


Figure 7. Random Read for Data

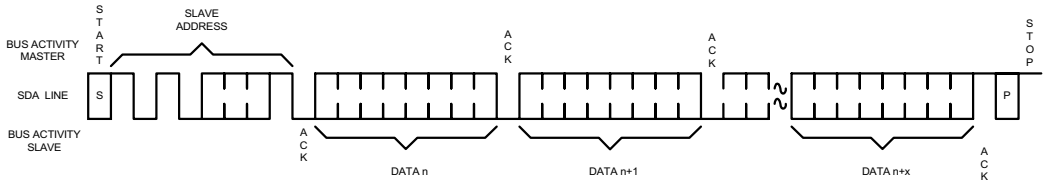
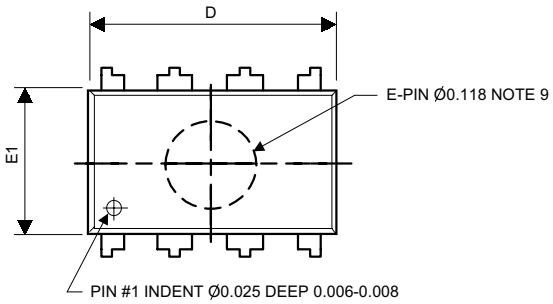
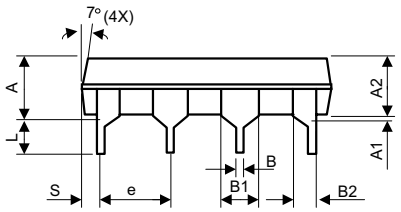


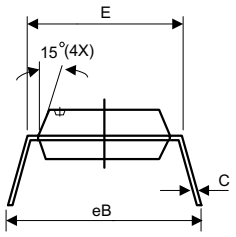
Figure 8. Sequential Read for Data

9.0 PACKAGE DIAGRAMS

Plastic Dual-in-line Package(PDIP)

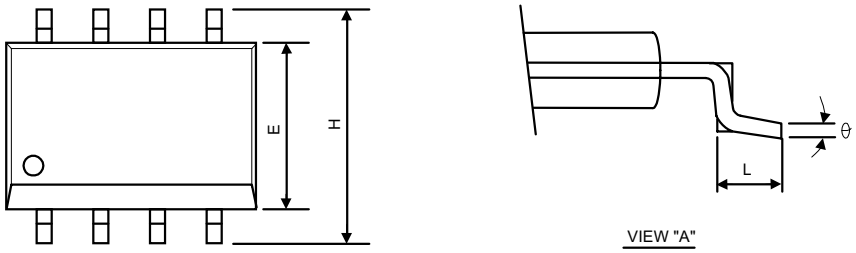


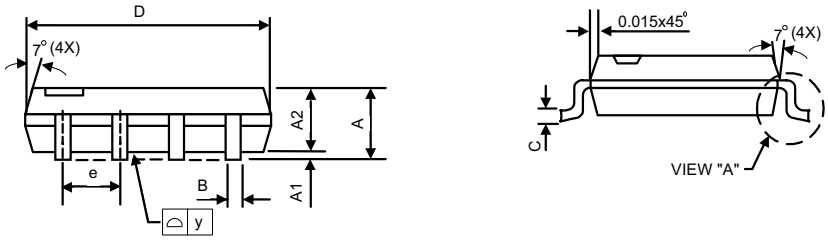




SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	5.33	—	—	0.210
A1	0.38	—	—	0.015	—	—
A2	3.25	3.30	3.45	0.128	0.130	0.136
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.14	1.27	1.52	0.045	0.050	0.060
B2	0.18	0.99	1.17	0.032	0.039	0.046
C	0.20	0.25	0.33	0.008	0.010	0.013
D	9.12	9.30	9.53	0.359	0.366	0.375
E	7.62	—	8.26	0.300	—	0.325
E1	6.20	6.35	6.60	0.244	0.250	0.260
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.38	—	9.40	0.330	—	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

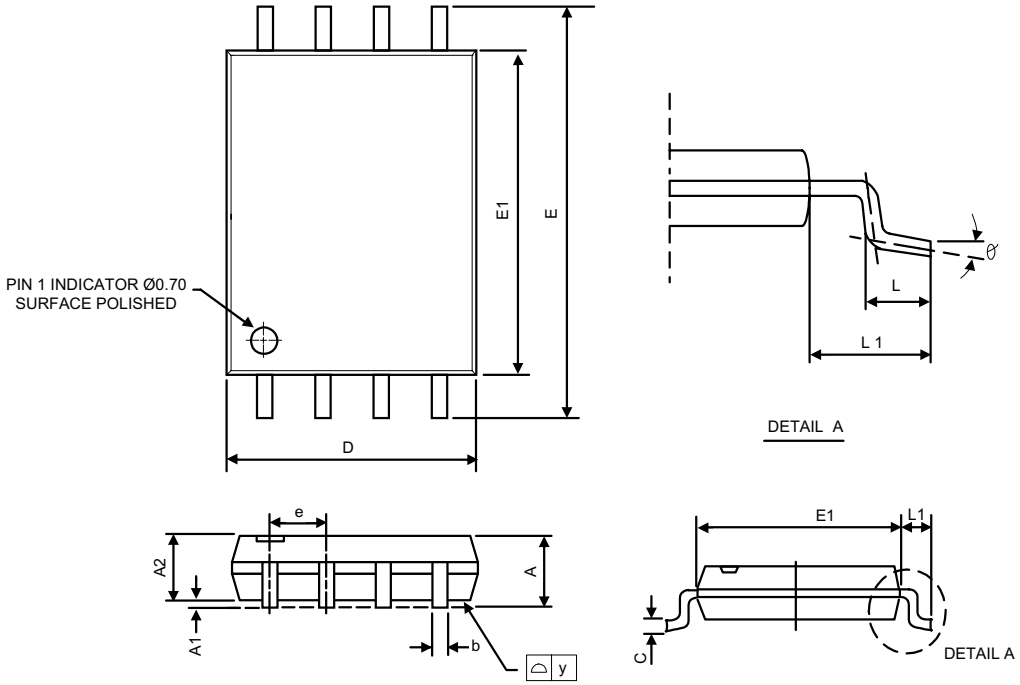
JEDEC Small Outline Package(SO-8)





SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	3.81	3.91	3.99	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

8L TSSOP PACKAGE OUTLING DRAWING



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.05	1.10	1.20
A1	0.05	0.10	0.15
A2	—	1.00	1.05
b	0.20	0.25	0.28
C	—	0.127	—
D	2.90	3.05	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	—	—	0.10
θ	0^O	4^O	8^O