DATA SHEET

P-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR 2SJ329

# SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

### DESCRIPTION

The 2SJ329 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

### **FEATURES**

- Low On-state Resistance
  - $R_{DS(on)} = 47 \text{ m}\Omega \text{ TYP.}$  (Vgs = -10 V, ID = -8 A)
  - $R_{DS(on)} = 80 \text{ m}\Omega \text{ TYP.} (V_{GS} = -4 \text{ V}, \text{ ID} = -6 \text{ A})$
- Low Ciss Ciss = 2 150 pF TYP.
- Built-in G-S Gate Protection Diodes

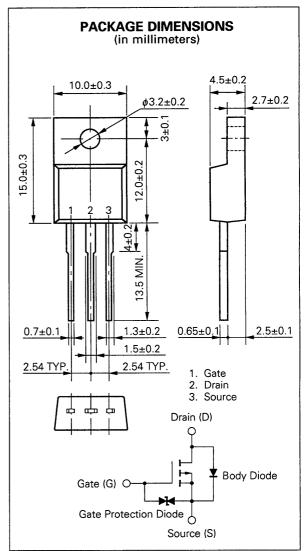
### **QUALITY GRADE**

#### Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

### ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub> = 25 °C)

Drain to Source Voltage	Vdss	-60	V
Gate to Source Voltage	VGSS(AC)	<b>∓20</b>	V
Gate to Source Voltage		-20, +10	V
Drain Current (DC)	ID(DC)	<b>∓15</b>	А
Drain Current (pulse)	D(pulse)*	<b>∓60</b>	А
Total Power Dissipation (Tc = 25 °C)	Рт1	35	W
Total Power Dissipation (Ta = 25 °C)	Ρτ2	2.0	W
Channel Temperature	Tch	150 °C	MAX.
Storage Temperature	Tstg	–55 to +150	°C
* PW ≦ 10 $\mu$ s, Duty Cycle ≦ 1 %			



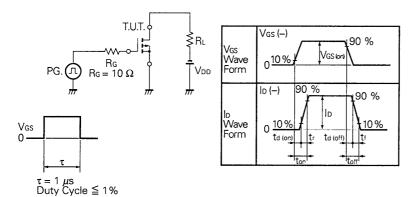
Document No. TC-2464 (O.D. No. TC-7969) Date Published November 1993 M Printed in Japan

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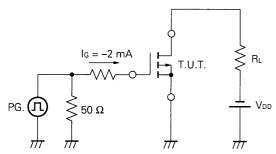
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-state Resistance	RDS(on)		47	60	mΩ	Vgs = -10 V, Id = -8 A	
Drain to Source On-state Resistance	RDS(on)		80	110	mΩ	$V_{GS} = -4 V$ , $I_D = -6 A$	
Gate to Source Cutoff Voltage	VGS(off)	-1.0	-1.5	-2.0	v	Vps = -10 V, lp = -1 mA	
Forward Transfer Admittance	yfs	8.0	12		S	$V_{DS} = -10 V$ , $I_D = -8 A$	
Drain Leakage Current	loss			-10	μΑ	$V_{DS} = -60 V, V_{GS} = 0$	
Gate to Source Leakage Current	lgss			<b>∓10</b>	μΑ	Vgs = ∓16 V, Vds = 0	
Input Capacitance	Ciss		2 150		pF	$V_{DS} = -10 V$ $V_{GS} = 0$ f = 1 MHz	
Output Capacitance	Coss		1 100		pF		
Reverse Transfer Capacitance	Crss		530		pF		
Turn-On Delay Time	td(on)		35		ns	VGS(on) = -10 V VDD = -30 V	
Rise Time	tr		150		ns		
Turn-Off Delay Time	td(off)		260		ns	lɒ =8 A, Rg = 10 Ω	
Fall Time	tr	·	230		ns	RL = 3.8 Ω	
Total Gate Charge	QG		80		nC	Vgs = -10 V	
Gate to Source Charge	Qgs		6		nC	$I_{D} = -15 \text{ A}$	
Gate to Drain Charge	Qgd		35		nC	Vdd =48 V	
Diode Forward Voltage	Vsd		1.0		V	IF = 15 A, VGS = 0	
Reverse Recovery Time	trr		120		ns	IF = 15 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs	
Reverse Recovery Charge	Qrr		260		nC		

### ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

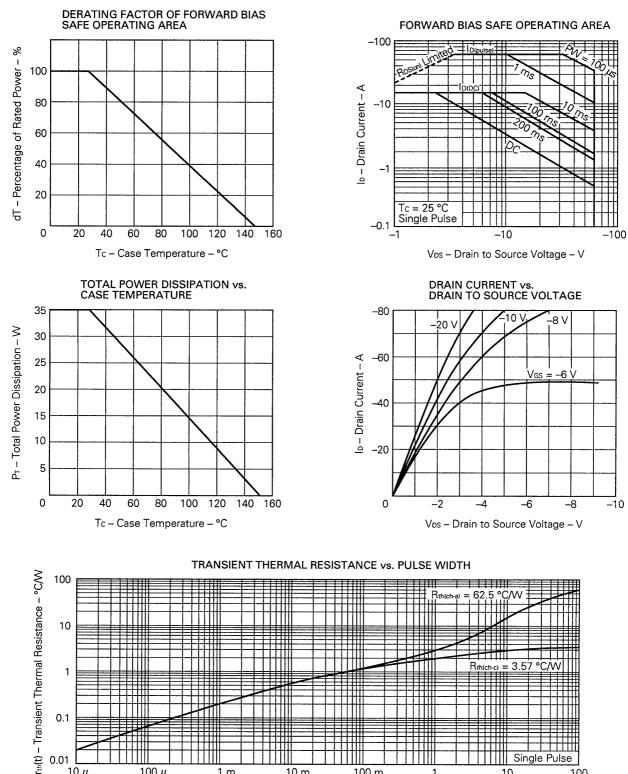
## **Test Circuit 1: Switching Time**

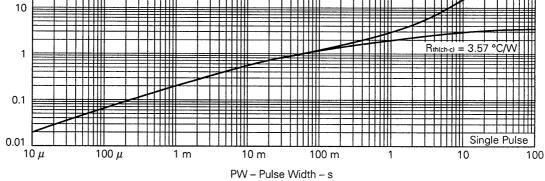


### **Test Circuit 2: Gate Charge**

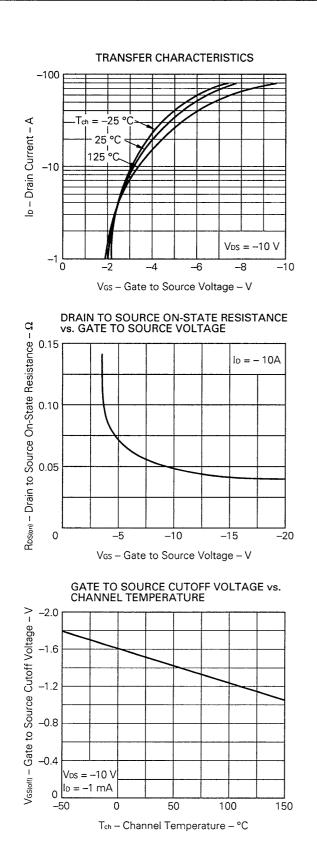


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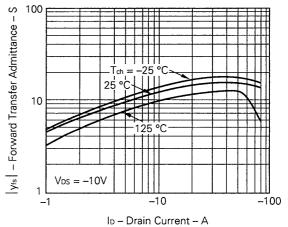




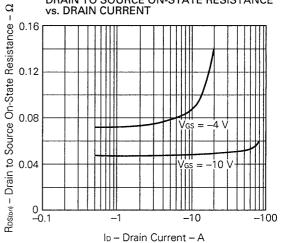
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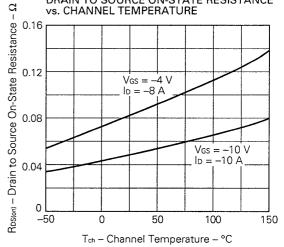
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



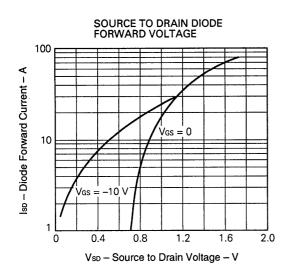
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



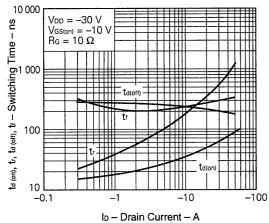
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

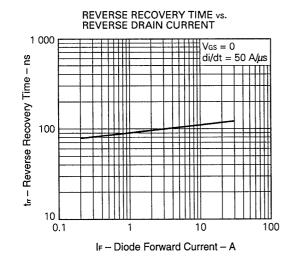


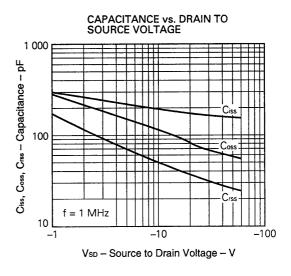
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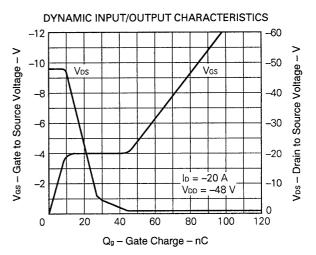












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#### Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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