

P-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR
2SJ330

SWITCHING
P-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SJ330 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 40 \text{ m}\Omega$ TYP. ($V_{GS} = -10 \text{ V}$, $I_D = -10 \text{ A}$)
 $R_{DS(on)} = 70 \text{ m}\Omega$ TYP. ($V_{GS} = -4 \text{ V}$, $I_D = -8 \text{ A}$)
- Low C_{iss} $C_{iss} = 2\ 570 \text{ pF}$ TYP.
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

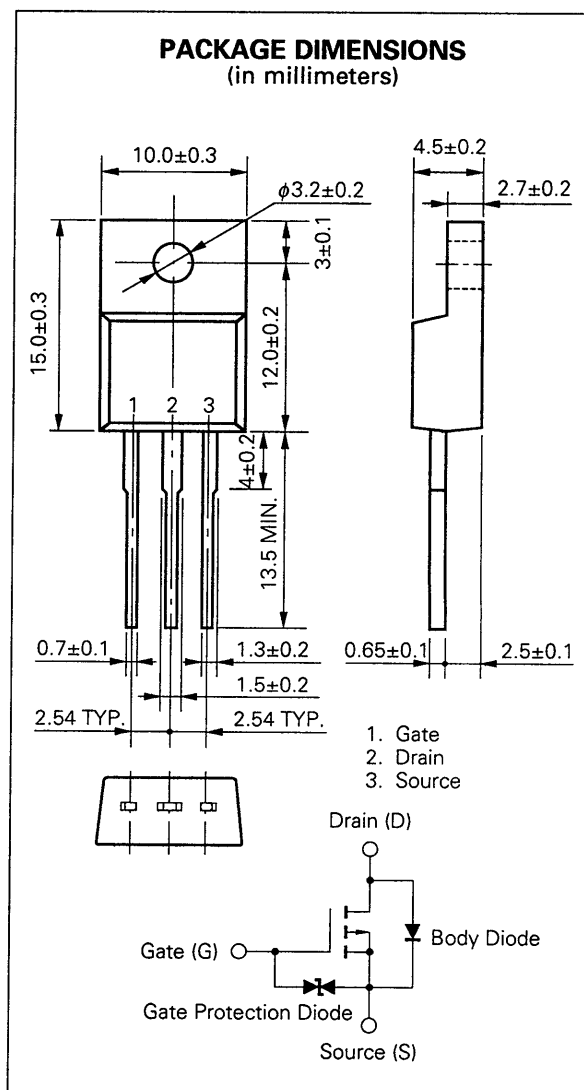
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25 \text{ }^\circ\text{C}$)

| | | | |
|---|------------------|-------------|-----------------------|
| Drain to Source Voltage | V_{DSS} | -60 | V |
| Gate to Source Voltage | $V_{GSS(AC)}$ | ∓ 20 | V |
| Gate to Source Voltage | $V_{GSS(DC)}$ | -20, +10 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ∓ 20 | A |
| Drain Current (pulse) | $I_{D(pulse)^*}$ | ∓ 80 | A |
| Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$) | PT_1 | 35 | W |
| Total Power Dissipation ($T_a = 25 \text{ }^\circ\text{C}$) | PT_2 | 2.0 | W |
| Channel Temperature | T_{ch} | 150 | $^\circ\text{C}$ MAX. |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |

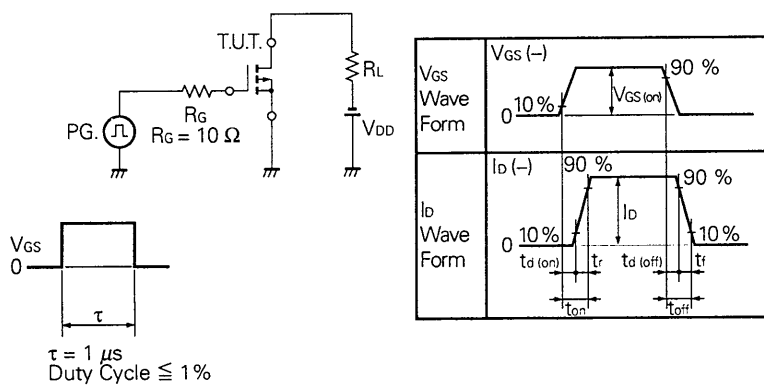
* $PW \leq 10 \text{ }\mu\text{s}$, Duty Cycle $\leq 1 \%$



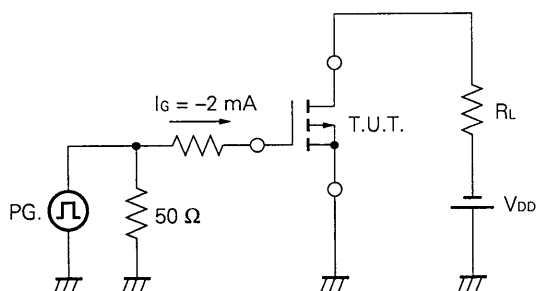
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|-------------------------------------|----------------------|------|-------|------|------|---|
| Drain to Source On-state Resistance | R _{DS(on)} | | 0.04 | 0.05 | Ω | V _{GS} = -10 V, I _D = -10 A |
| Drain to Source On-state Resistance | R _{DS(on)} | | 0.07 | 0.09 | Ω | V _{GS} = -4 V, I _D = -8 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | -1.0 | -1.6 | -2.0 | V | V _{DS} = -10 V, I _b = -1 mA |
| Forward Transfer Admittance | y _{fs} | 10 | | | S | V _{DS} = -10 V, I _b = -10 A |
| Drain Leakage Current | I _{DSS} | | | -10 | μA | V _{DS} = -60 V, V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±10 | μA | V _{GS} = ±16 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 2 570 | | pF | V _{DS} = -10 V V _{GS} = 0 f = 1 MHz |
| Output Capacitance | C _{oss} | | 1 460 | | pF | |
| Reverse Transfer Capacitance | C _{rss} | | 640 | | pF | |
| Turn-On Delay Time | t _{d(on)} | | 50 | | ns | V _{GS(on)} = -10 V V _{DD} = -30 V I _D = -10 A, R _G = 10 Ω R _L = 3.0 Ω |
| Rise Time | t _r | | 200 | | ns | |
| Turn-Off Delay Time | t _{d(off)} | | 340 | | ns | |
| Fall Time | t _f | | 230 | | ns | |
| Total Gate Charge | Q _G | | 90 | | nC | V _{GS} = -10 V I _b = -20 A V _{DD} = -48 V |
| Gate to Source Charge | Q _{GS} | | 7 | | nC | |
| Gate to Drain Charge | Q _{GD} | | 36 | | nC | |
| Diode Forward Voltage | V _{SD} | | 0.9 | | V | I _F = 20 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 100 | | ns | I _F = 20 A, V _{GS} = 0 |
| Reverse Recovery Charge | Q _{rr} | | 490 | | nC | di/dt = 50 A/μs |

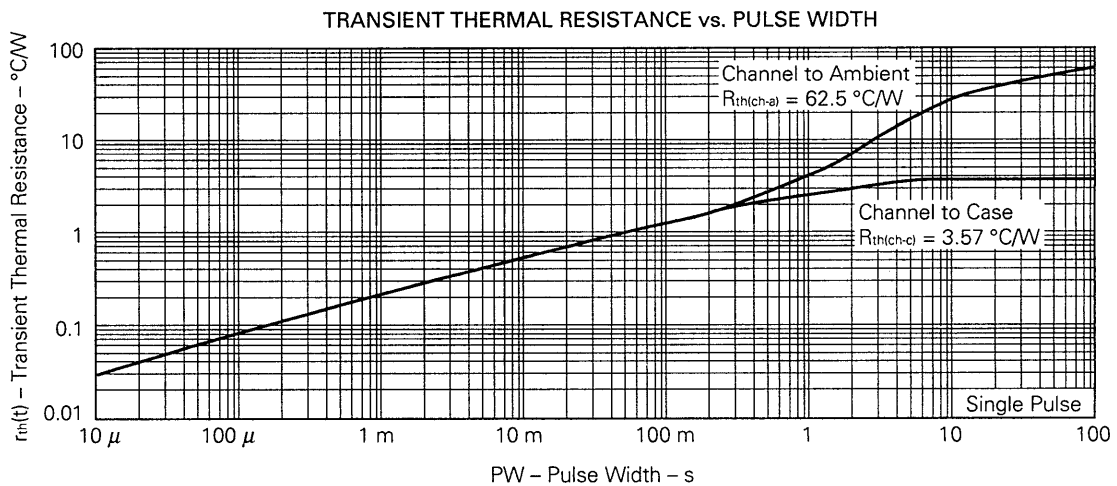
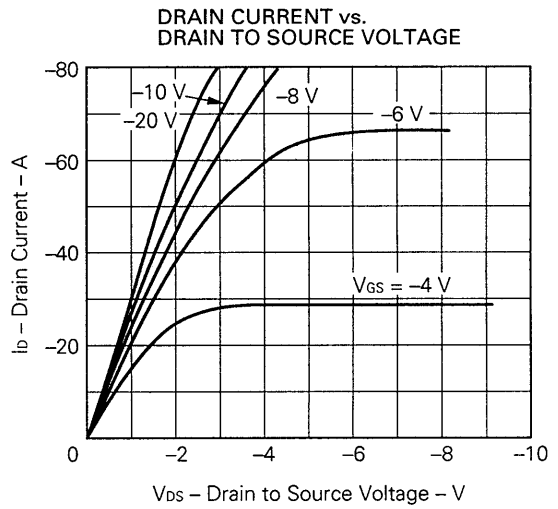
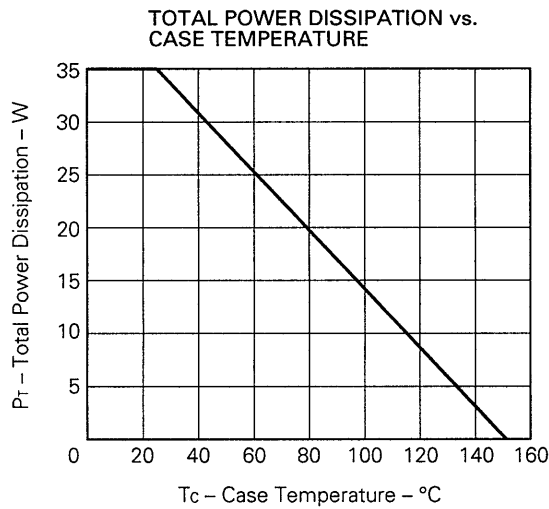
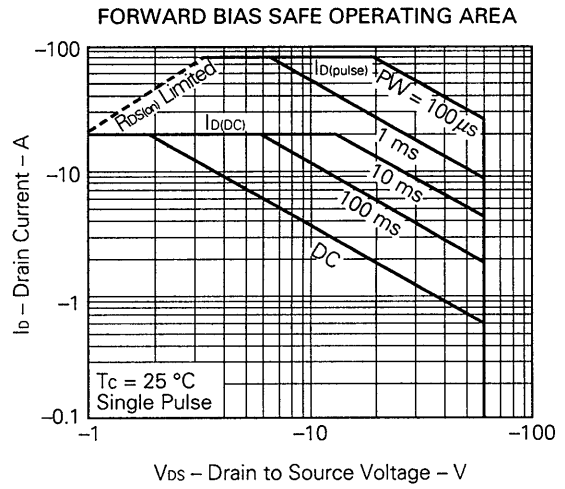
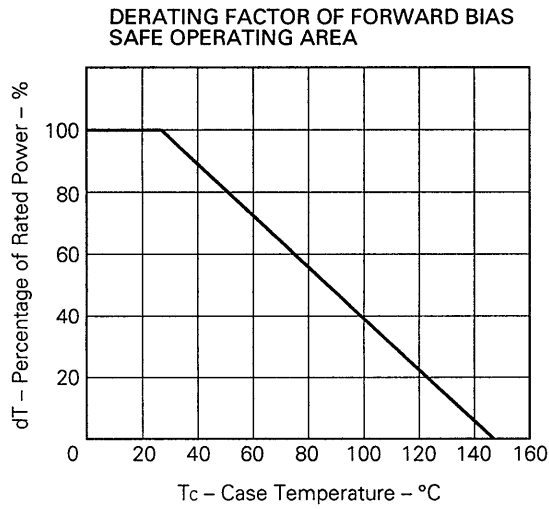
Test Circuit 1: Switching Time



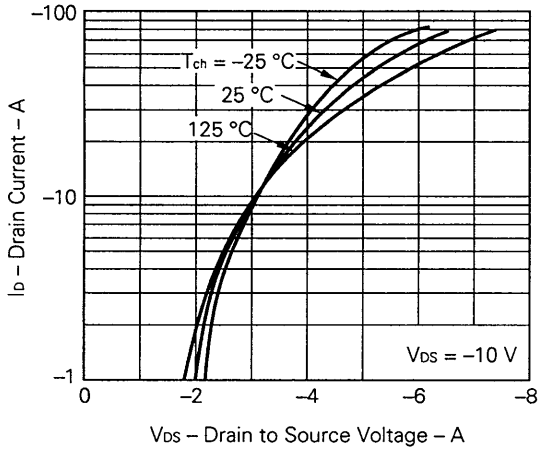
Test Circuit 2: Gate Charge



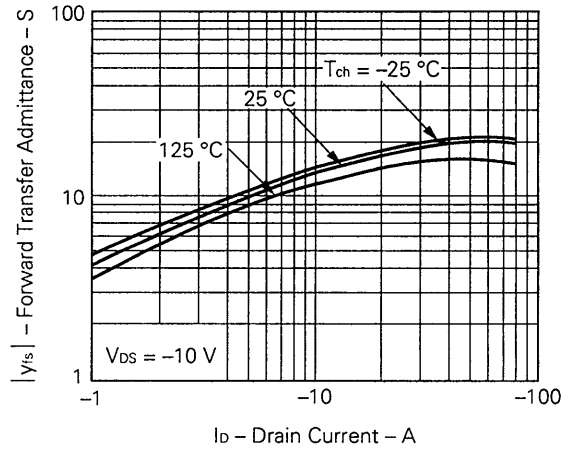
TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$)



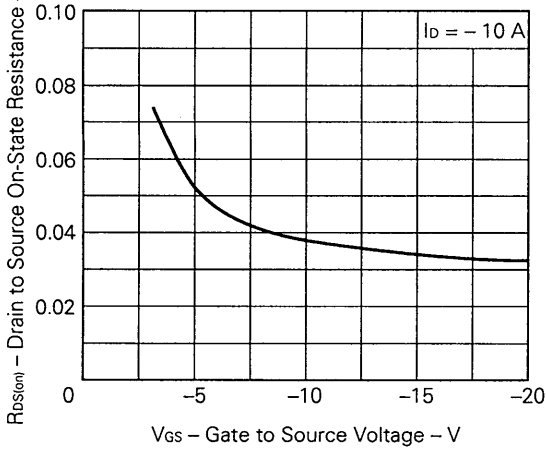
TRANSFER CHARACTERISTICS



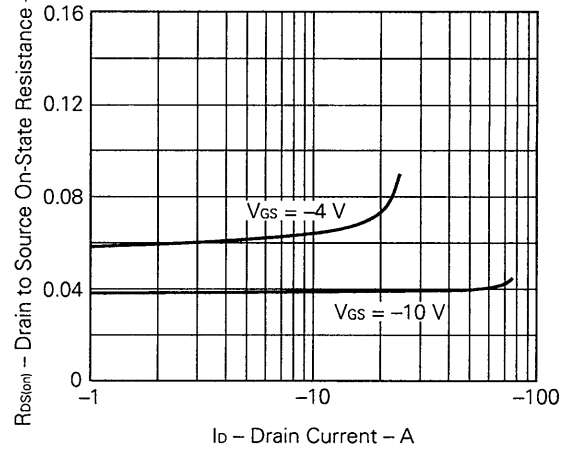
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



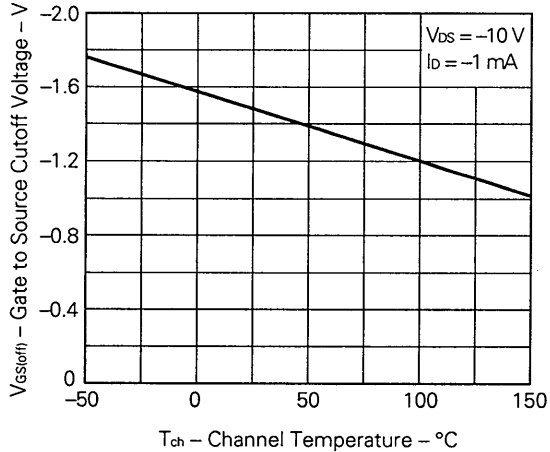
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



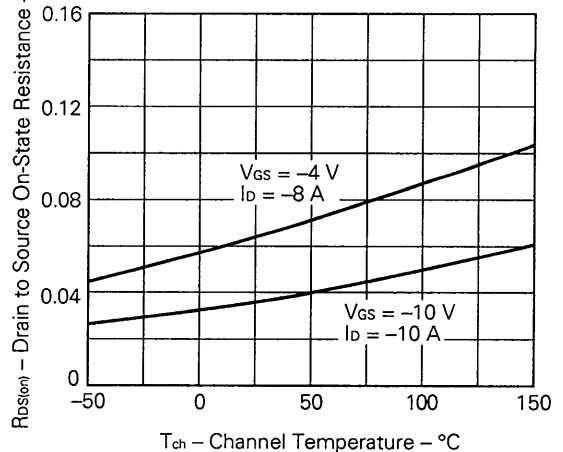
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



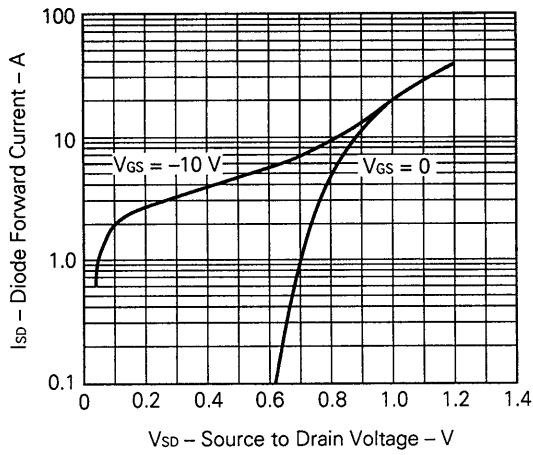
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



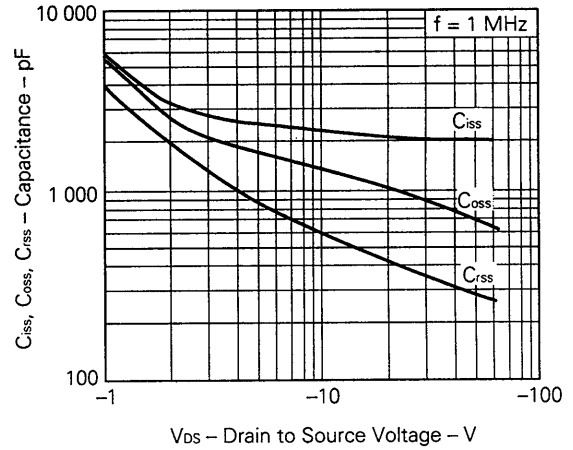
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



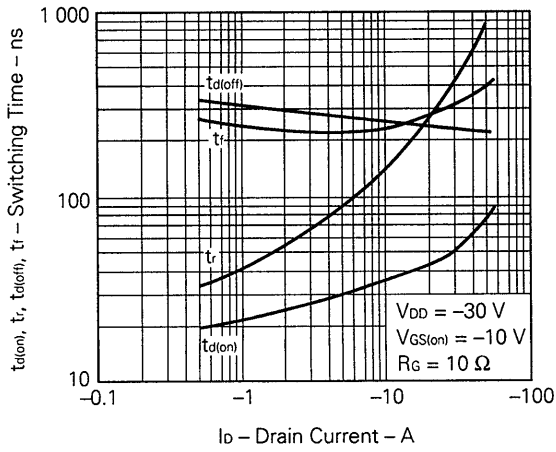
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



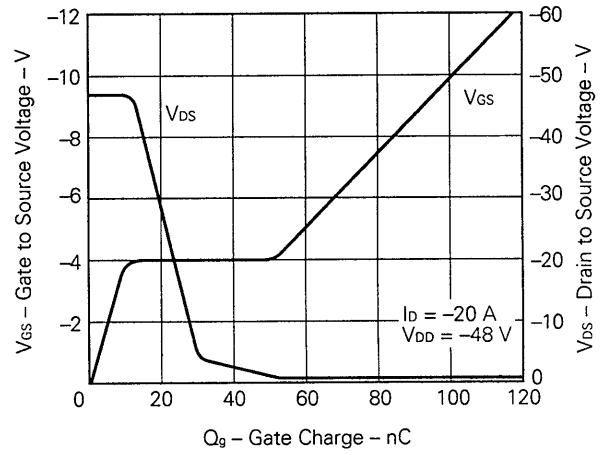
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



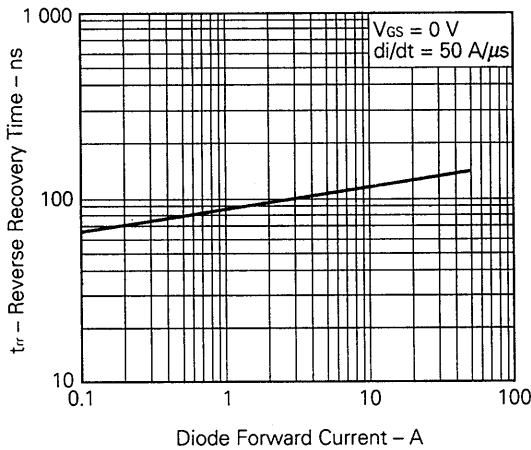
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



Reference

| Application note name | No. |
|--|----------|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

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