DATA SHEET



MOS FIELD EFFECT TRANSISTOR **2SK2480**

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2480 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

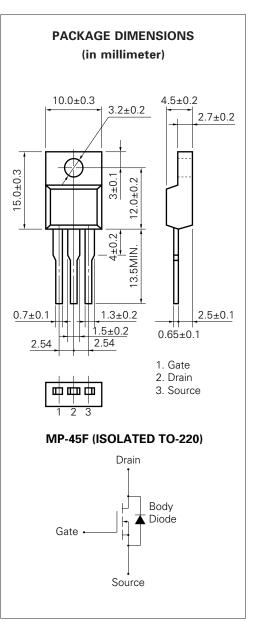
FEATURES

- Low On-Resistance
- RDS (on) = 4.0 Ω (VGS = 10 V, ID = 2.0 A)
- Low C_{iss} C_{iss} = 900 pF TYP.
- High Avalanche Capability Ratings
- Isolated TO-220 Package

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	VDSS	900	V
Gate to Source Voltage	Vgss	±30	V
Drain Current (DC)	D(DC)	±3.0	А
Drain Current (pulse)*	D(pulse	e) ±12	А
Total Power Dissipation (T _c = 25 $^{\circ}$ C)	P T1	35	W
Total Power Dissipation (T _A = 25 $^{\circ}$ C)	Рт2	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	Tstg	–55 to +150	°C
Single Avalanche Current**	las	3.0	А
Single Avalanche Energy**	Eas	37.1	mJ
* PW \leq 10 μ s, Duty Cycle \leq 1 %			

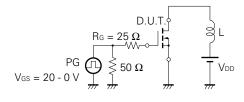
** Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0

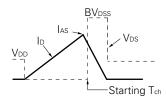


ELECTRICAL	CHARACTERISTICS	(Ta = 25	° C)
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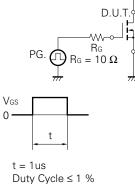
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	RDS (on)		3.2	4.0	Ω	$V_{GS} = 10 \text{ V}, \text{ Id} = 2.0 \text{ A}$
Gate to Source Cutoff Voltage	VGS (off)	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	1.0			S	$V_{DS} = 20 V, I_{D} = 2.0 A$
Drain Leakage Current	Ibss			100	μΑ	Vds = Vdss, Vgs = 0
Gate to Source Leakage Current	lgss			±100	nA	$V_{GS} = \pm 30 \text{ V}, \text{ V}_{DS} = 0$
Input Capacitance	Ciss		900		pF	V _{DS} = 10 V
Output Capacitance	Coss		130		pF	V _{GS} = 0
Reverse Transfer Capacitance	Crss		25		pF	f = 1 MHz
Turn-On Delay Time	td (on)		17		ns	ID = 2.0 A
Rise Time	tr		7		ns	Vgs = 10 V
Turn-Off Delay Time	td (off)		63		ns	V _{DD} = 150 V
Fall Time	tr		8		ns	$R_G = 75 \Omega$
Total Gate Charge	Q _G		30		nC	ID = 3.0 A
Gate to Source Charge	Q _{GS}		5		nC	$V_{DD} = 450 V$
Gate to Drain Charge	Qgd		16		nC	Vgs = 10 V
Body Diode Forward Voltage	VF (S-D)		1.0		V	IF = 3.0 A, VGS = 0
Reverse Recovery Time	trr		650		ns	IF = 3.0 A, VGS = 0
Reverse Recovery Charge	Qrr		2.8		μC	di/dt = 50 A/ μ s

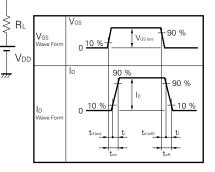
Test Circuit 1 Avalanche Capability



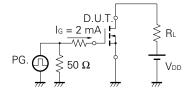


Test Circuit 2 Switching Time

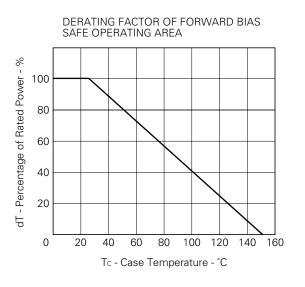




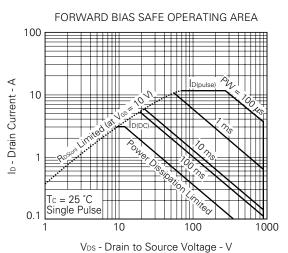
Test Circuit 3 Gate Charge



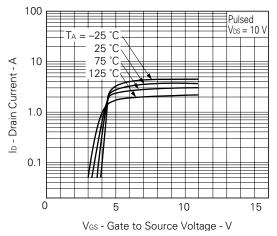
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

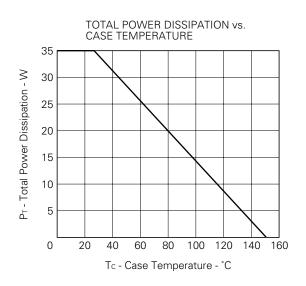




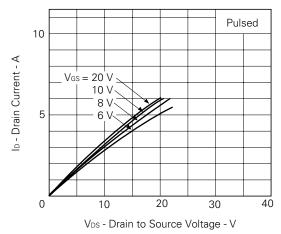


FORWARD TRANSFER CHARACTERISTICS

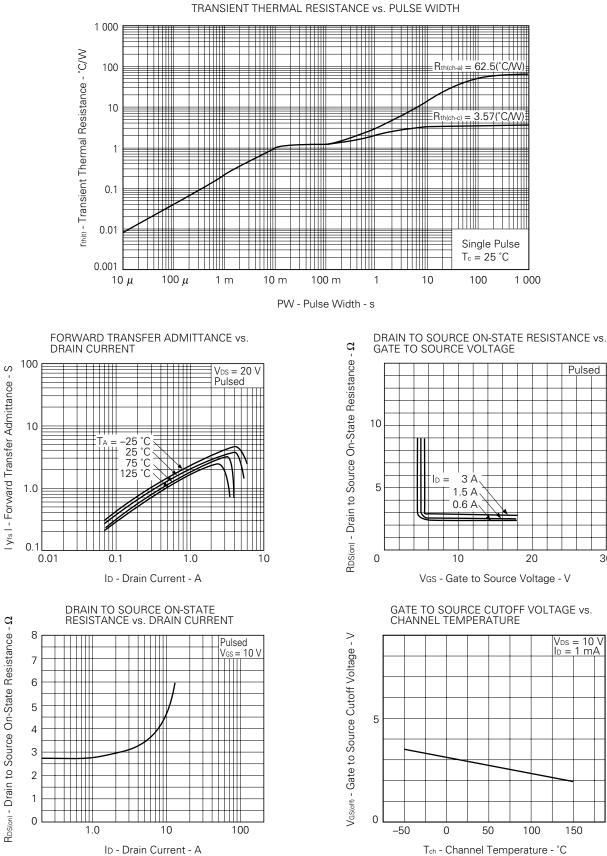




DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



30



Pulsed

1.5

 $V_{DD} = 150 V$ $V_{GS} = 10 V$ $R_{G} = 10 \Omega$

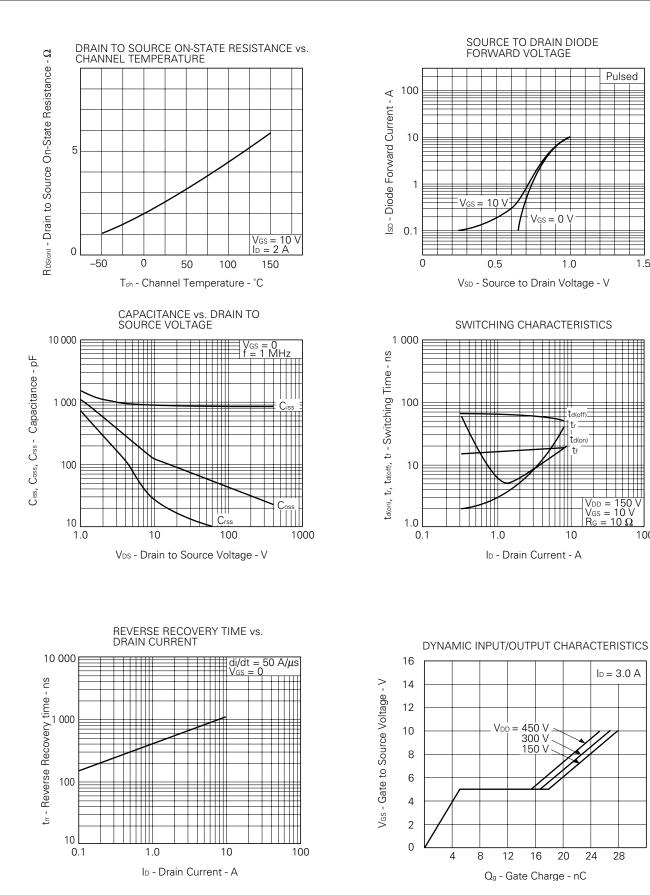
ID = 3.0 A

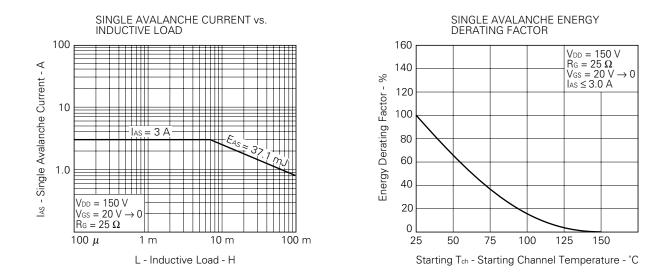
24

28

V

100





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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Anti-radioactive design is not implemented in this product.

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