NEC

MOS FIELD EFFECT TRANSISTOR

2SK3430

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3430 is N-channel MOS Field Effect Transistor designed for high current switching applications.

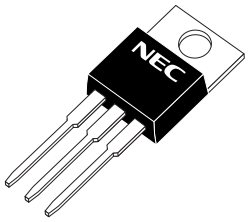
FEATURES

- Super low on-state resistance:
- ★ $R_{DS(on)1}$ = 7.3 mΩ MAX. (V_{GS} = 10 V, I_D = 40 A)
- ★ $R_{DS(on)2}$ = 15 mΩ MAX. (V_{GS} = 4 V, I_D = 40 A)
- ★ • Low C_{iss}: C_{iss} = 2800 pF TYP.
- Built-in gate protection diode

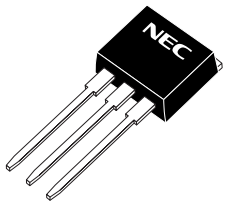
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3430	TO-220AB
2SK3430-S	TO-262
2SK3430-Z	TO-220SMD

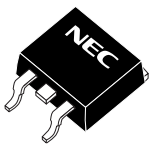
(TO-220AB)



(TO-262)



(TO-220SMD)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	40	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±80	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±200	A
Total Power Dissipation (T_C = 25°C)	P_T	84	W
Total Power Dissipation (T_A = 25°C)	P_T	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
★ Single Avalanche Current Note2	I_{AS}	37	A
★ Single Avalanche Energy Note2	E_{AS}	137	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

THERMAL RESISTANCE

Channel to Case	Rth(ch-C)	1.49	°C/W
Channel to Ambient	Rth(ch-A)	83.3	°C/W

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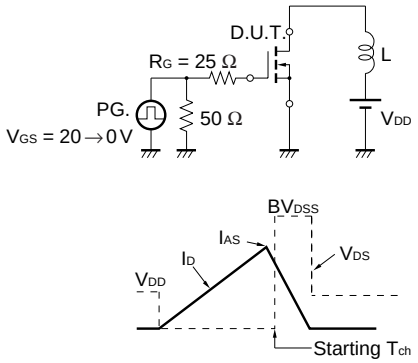
The mark ★ shows major revised points.

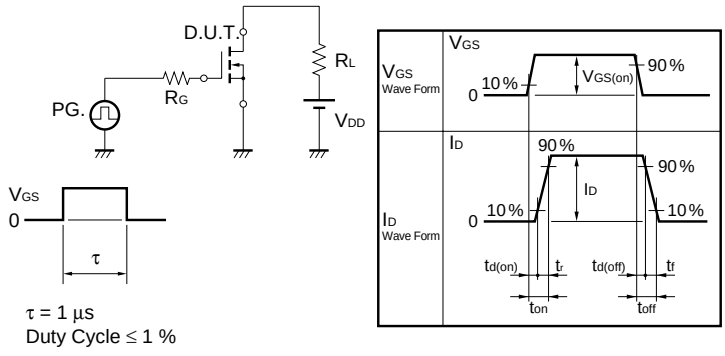
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
★	Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 40 A		5.9	7.3	mΩ
★		$R_{DS(on)2}$	V_{GS} = 4 V, I_D = 40 A		10.5	15	mΩ
	Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
	Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 40 A	20	40		S
	Drain Leakage Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			10	μA
	Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
★	Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		2800		pF
	Output Capacitance	C_{oss}			730		pF
★	Reverse Transfer Capacitance	C_{rss}			320		pF
★	Turn-on Delay Time	$t_{d(on)}$	I_D = 40 A, $V_{GS(on)}$ = 10 V, V_{DD} = 20 V,		110		ns
★	Rise Time	t_r	R_G = 10 Ω		1800		ns
★	Turn-off Delay Time	$t_{d(off)}$			170		ns
★	Fall Time	t_f			350		ns
	Total Gate Charge	Q_G	I_D = 80 A , V_{DD} = 32 V, V_{GS} = 10 V		50		nC
★	Gate to Source Charge	Q_{GS}			10		nC
★	Gate to Drain Charge	Q_{GD}			14		nC
	Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 80 A, V_{GS} = 0 V		1.0		V
★	Reverse Recovery Time	t_{rr}	I_F = 80 A, V_{GS} = 0 V,		50		ns
★	Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		77		nC

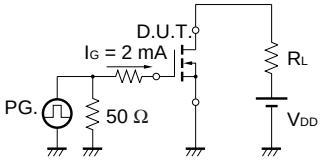
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

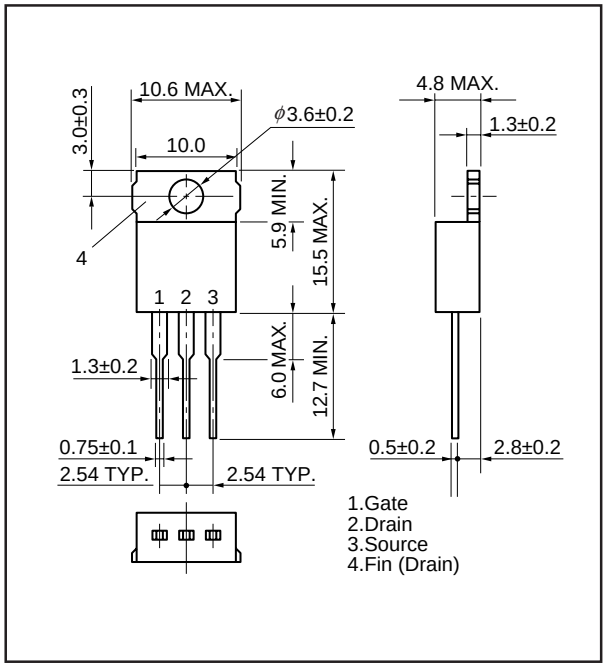


TEST CIRCUIT 3 GATE CHARGE

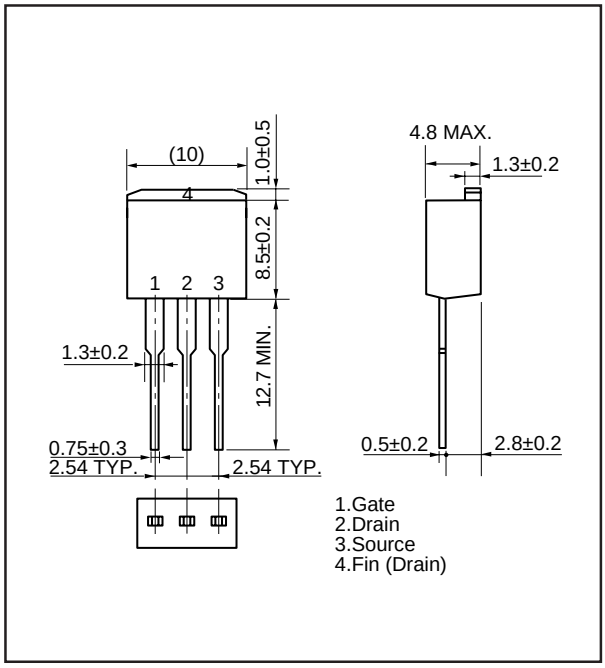


PACKAGE DRAWINGS (Unit: mm)

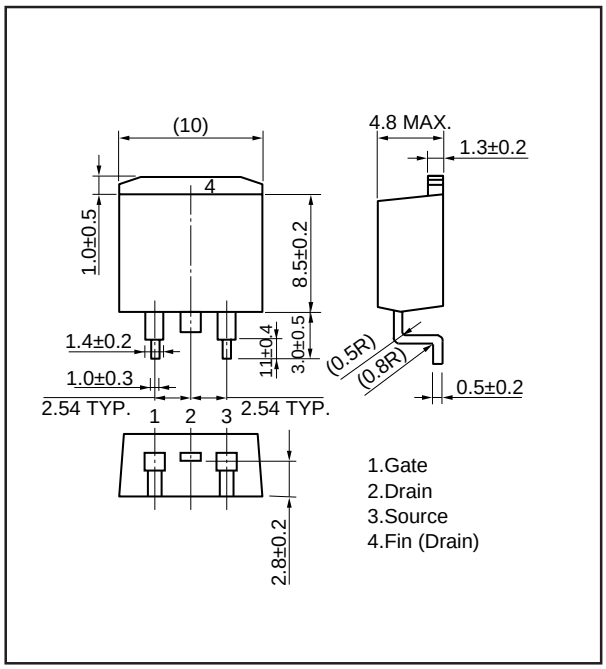
1) TO-220AB (MP-25)



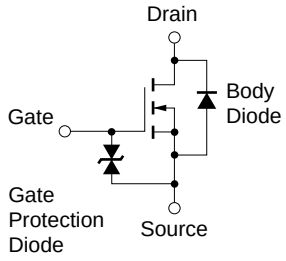
2) TO-262 (MP-25 Fin Cut)



3) TO-220SMD (MP-25Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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