

16M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE

UNBUFFERED TYPE

★ Description

The MC-4516CA727EF and MC-4516CA727PF are 16,777,216 words by 72 bits synchronous dynamic RAM module on which 9 pieces of 128M SDRAM: μ PD45128841 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 16,777,216 words by 72 bits organization (ECC Type)
- Clock frequency and access time from CLK

Part number	/CAS latency	Clock frequency (MAX.)	Access time from CLK (MAX.)
MC-4516CA727EF-A75	CL = 3	133 MHz	5.4 ns
	CL = 2	100 MHz	6.0 ns
MC-4516CA727PF-A75	CL = 3	133 MHz	5.4 ns
	CL = 2	100 MHz	6.0 ns

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and full page)
- Programmable wrap sequence (sequential / interleave)
- ★ Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- All DQs have $10\Omega \pm 10\%$ of series resistor
- Single 3.3 V \pm 0.3 V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Unbuffered type
- Serial PD

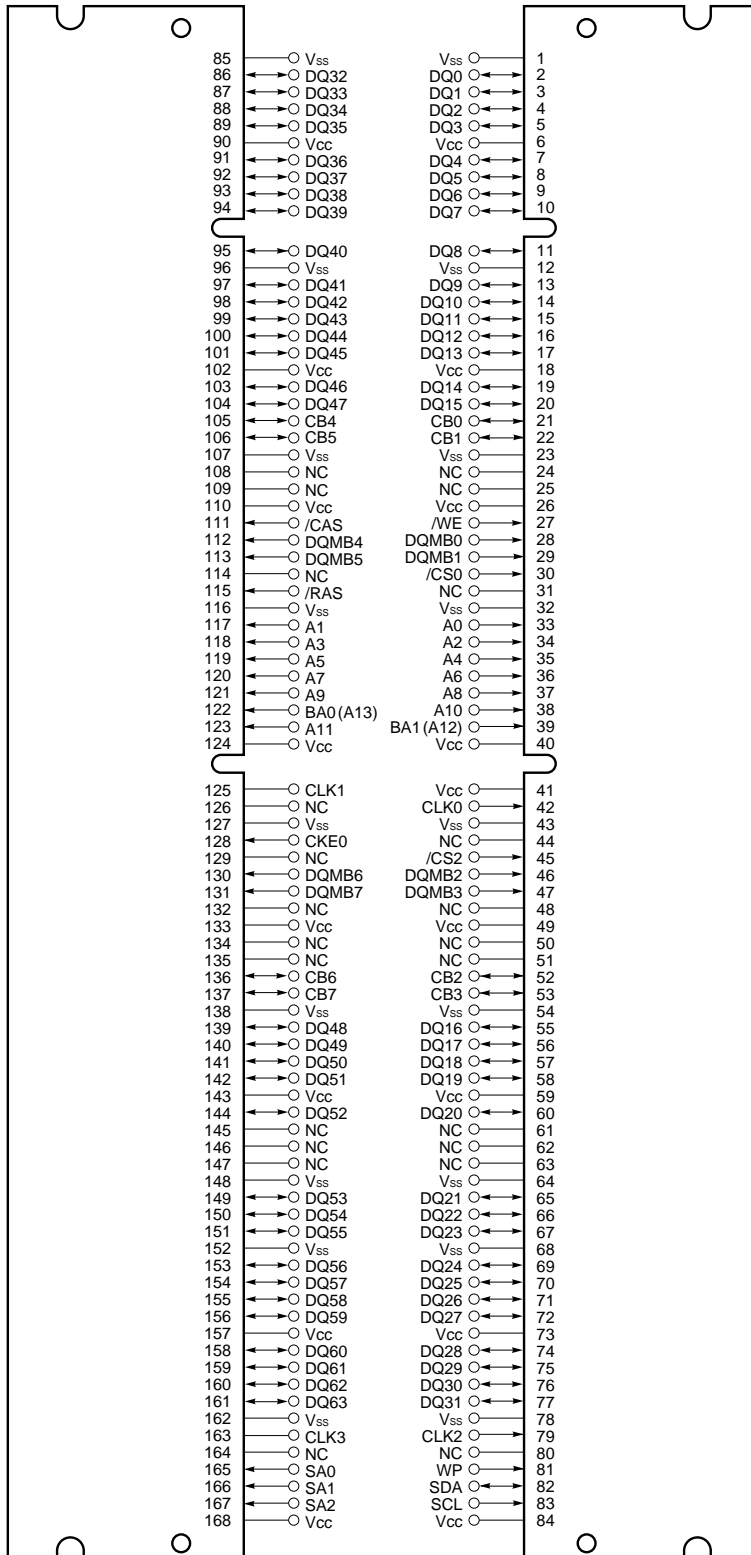
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Ordering Information

Part number	Clock frequency (MAX.)	Package	Mounted devices
MC-4516CA727EF-A75	133 MHz	168-pin Dual In-line Memory Module (Socket Type)	9 pieces of μ PD45128841G5 (Rev. E) (10.16 mm (400) TSOP (II))
★ MC-4516CA727PF-A75		Edge connector : Gold plated 34.93 mm height	9 pieces of μ PD45128841G5 (Rev. P) (10.16 mm (400) TSOP (II))

★ Pin Configuration

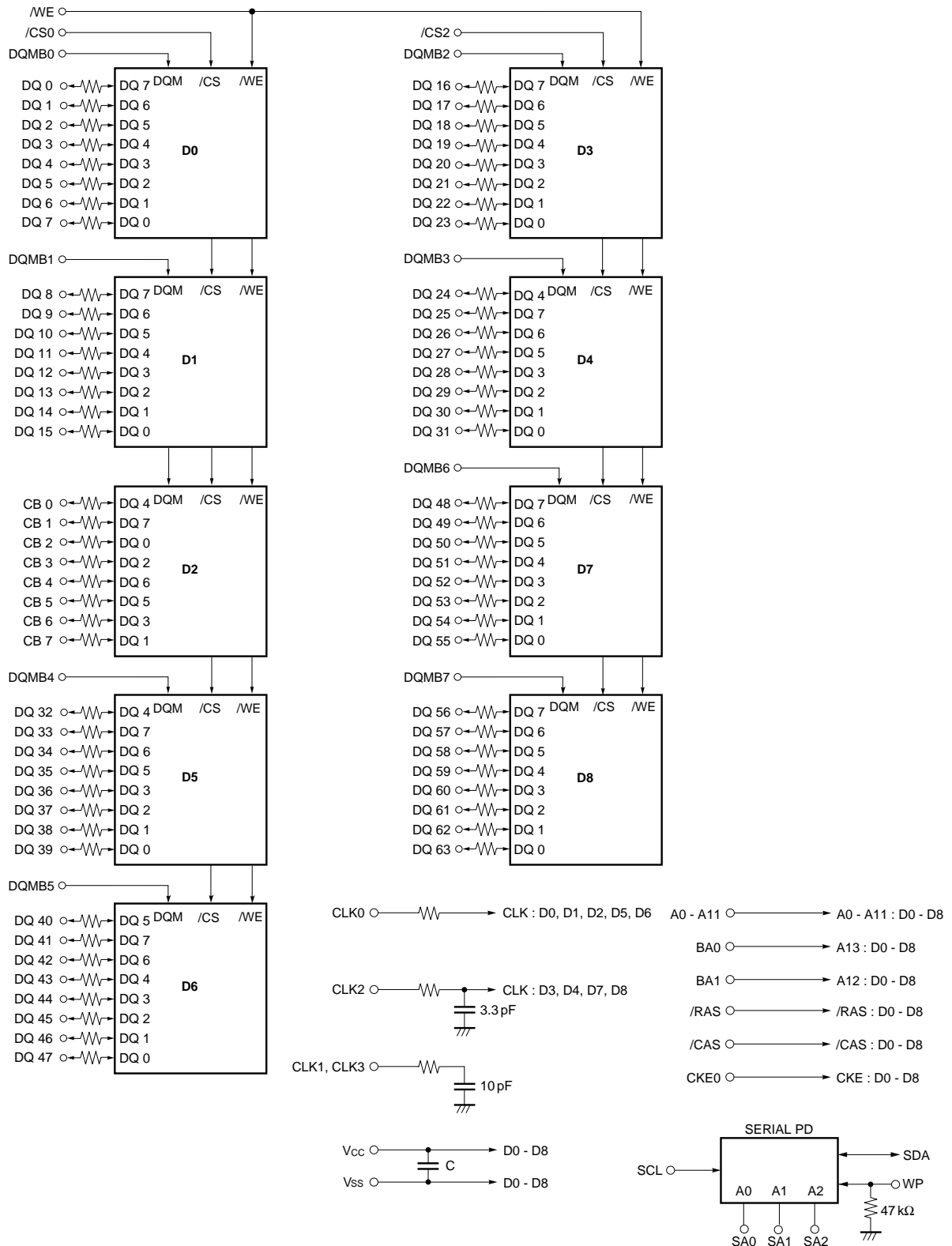
168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

- A0 - A11 : Address Inputs
- [Row: A0 - A11, Column: A0 – A9]
- BA0 (A13), BA1 (A12) : SDRAM Bank Select
- DQ0 - DQ63, CB0 - CB7 : Data Inputs/Outputs
- CLK0 - CLK3 : Clock Input
- CKE0 : Clock Enable Input
- /CS0, /CS2 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7: DQ Mask Enable
- SA0 - SA2 : Address Input for EEPROM
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- WP : Write Protect
- NC : No Connection

Block Diagram



- Remarks 1.** The value of all resistors is 10 Ω except WP.
2. D0 - D8: μPD45128841 (4M words × 8 bits × 4 banks)

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μ s and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _{CC}		-0.5 to +4.6	V
Voltage on input pin relative to GND	V _T		-0.5 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		9	W
Operating ambient temperature	T _A		0 to 70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		V _{CC} + 0.3	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A11, BA0(A13), BA1(A12), /RAS, /CAS, /WE	40		66	pF
	C _{I2}	CLK0, CLK2	24		40	
	C _{I3}	CKE0	34		56	
	C _{I4}	/CS0, /CS2	17		33	
	C _{I5}	DQMB0 - DQMB7	7		17	
Data input/output capacitance	C _{I/O}	DQ0 - DQ63, CB0 - CB7	7		13	pF

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

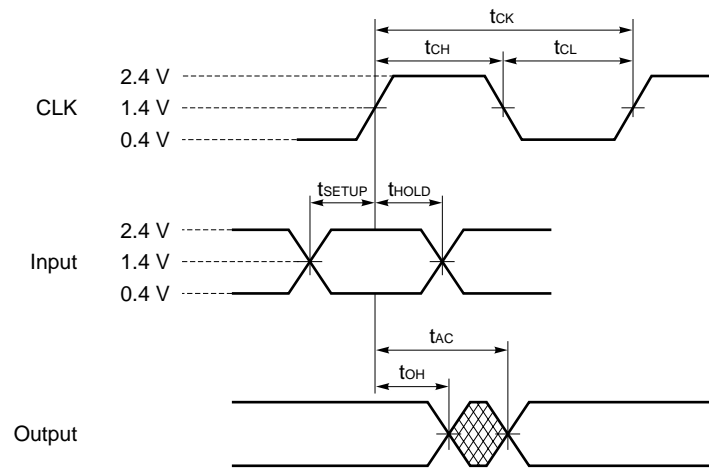
Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
★ Operating current	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC(MIN.)} , I _O = 0 mA	/CAS latency = 2	900	mA	1
			/CAS latency = 3	945		
★ Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns		9	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞		9		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.		180	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞ Input signals are stable.		72		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns		45	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞		36		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.		270	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.		180		
★ Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} , I _O = 0 mA	/CAS latency = 2	1,080	mA	2
			/CAS latency = 3	1,395		
★ CBR (Auto) refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}	/CAS latency = 2	2,070	mA	3
			/CAS latency = 3	2,160		
★ Self refresh current	I _{CC6}	CKE ≤ 0.2 V		18	mA	
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V	-9	+9	μA	
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V	-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +4 mA		0.4	V	

- Notes**
1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 3. I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

★ Test Conditions

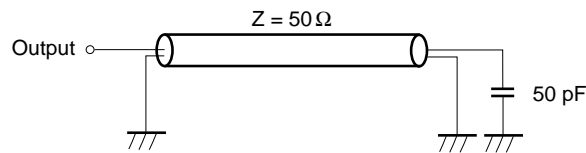
Parameter	Value	Unit
AC high level input voltage / low level input voltage	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Transition time (Input rise and fall time)	1	ns
Output timing measurement reference level	1.4	V



★ Synchronous Characteristics

Parameter		Symbol	-A75		Unit	Note
			MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t _{CK3}	7.5	(133 MHz)	ns	
	/CAS latency = 2	t _{CK2}	10	(100 MHz)	ns	
Access time from CLK	/CAS latency = 3	t _{AC3}		5.4	ns	1
	/CAS latency = 2	t _{AC2}		6.0	ns	1
CLK high level width		t _{CH}	2.5		ns	
CLK low level width		t _{CL}	2.5		ns	
Data-out hold time		t _{OH}	3.0		ns	1
Data-out low-impedance time		t _{LZ}	0		ns	
Data-out high-impedance time	/CAS latency = 3	t _{HZ3}	3.0	5.4	ns	
	/CAS latency = 2	t _{HZ2}	3.0	6.0	ns	
Data-in setup time		t _{DS}	1.5		ns	
Data-in hold time		t _{DH}	0.8		ns	
Address setup time		t _{AS}	1.5		ns	
Address hold time		t _{AH}	0.8		ns	
CKE setup time		t _{CKS}	1.5		ns	
CKE hold time		t _{CKH}	0.8		ns	
CKE setup time (Power down exit)		t _{CKSP}	1.5		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t _{CMS}	1.5		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t _{CMH}	0.8		ns	

Note 1. Output load



Remark These specifications are applied to the monolithic device.

★ Asynchronous Characteristics

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
ACT to REF/ACT command period (operation)	t _{RC}	67.5		ns	
REF to REF/ACT command period (refresh)	t _{RC1}	67.5		ns	
ACT to PRE command period	t _{RAS}	45	120,000	ns	
PRE to ACT command period	t _{RP}	20		ns	
Delay time ACT to READ/WRITE command	t _{RCD}	20		ns	
ACT(one) to ACT(another) command period	t _{RRD}	15		ns	
Data-in to PRE command period	t _{DPL}	8		ns	
Data-in to ACT(REF) command period (Auto precharge)	/CAS latency = 3	t _{DAL3}	1CLK+22.5	ns	1
	/CAS latency = 2	t _{DAL2}	1CLK+20	ns	1
Mode register set cycle time	t _{RSC}	2		CLK	
Transition time	t _T	0.5	30	ns	
Refresh time (4,096 refresh cycles)	t _{REF}		64	ms	

Note This device can satisfy the t_{DAL3} spec of 1CLK+20 ns for up to and including 125 MHz operation.

Serial PD

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM	
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows	
4	Number of columns	0AH	0	0	0	0	1	0	1	0	10 columns	
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank	
6	Data width	48H	0	1	0	0	1	0	0	0	72 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	CL = 3 Cycle time	75H	0	1	1	1	0	1	0	1	7.5 ns	
10	CL = 3 Access time	54H	0	1	0	1	0	1	0	0	5.4 ns	
11	DIMM configuration type	02H	0	0	0	0	0	0	1	0	ECC	
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	Normal	
13	SDRAM width	08H	0	0	0	0	1	0	0	0	×8	
14	Error checking SDRAM width	08H	0	0	0	0	1	0	0	0	×8	
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock	
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F	
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	4 banks	
★	18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	2, 3
	19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0
	20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0
	21	SDRAM module attributes	00H	0	0	0	0	0	0	0	0	
	22	SDRAM device attributes : General	0EH	0	0	0	0	1	1	1	0	
★	23	CL = 2 Cycle time	A0H	1	0	1	0	0	0	0	0	10 ns
★	24	CL = 2 Access time	60H	0	1	1	0	0	0	0	0	6 ns
	25-26		00H	0	0	0	0	0	0	0	0	
★	27	t _{RP(MIN.)}	14H	0	0	0	1	0	1	0	0	20 ns
	28	t _{RRD(MIN.)}	0FH	0	0	0	0	1	1	1	1	15 ns
★	29	t _{RCD(MIN.)}	14H	0	0	0	1	0	1	0	0	20 ns
	30	t _{RAS(MIN.)}	2DH	0	0	1	0	1	1	0	1	45 ns
	31	Module bank density	20H	0	0	1	0	0	0	0	0	128M bytes

(2/2)

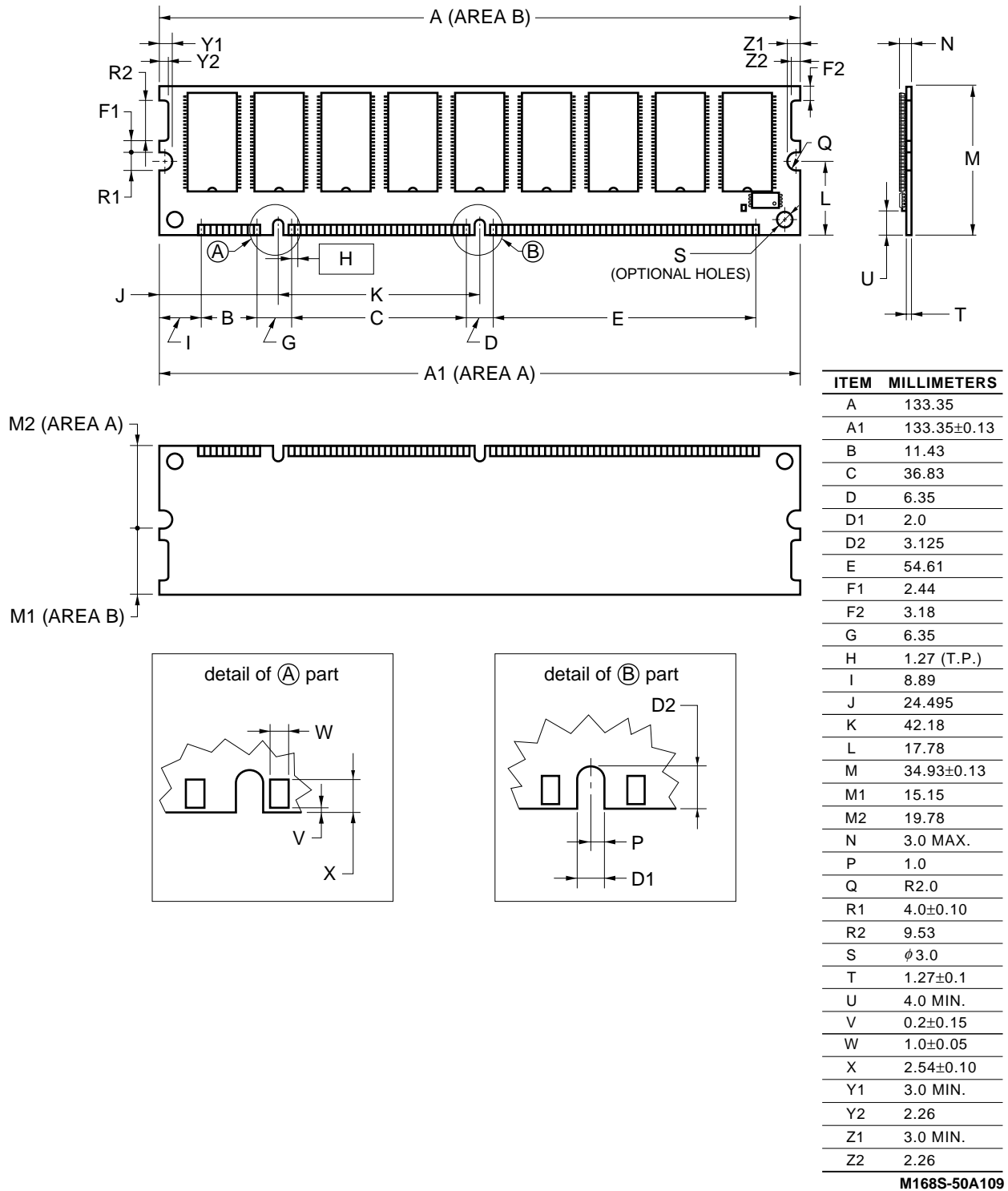
Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32	Command and address signal input setup time	15H	0	0	0	1	0	1	0	1	1.5 ns
33	Command and address signal input hold time	08H	0	0	0	0	1	0	0	0	0.8 ns
34	Data signal input setup time	15H	0	0	0	1	0	1	0	1	1.5 ns
35	Data signal input hold time	08H	0	0	0	0	1	0	0	0	0.8 ns
36-61		00H	0	0	0	0	0	0	0	0	
★ 62	SPD revision	12H	0	0	0	1	0	0	1	0	1.2
★ 63	Checksum for bytes 0 - 62	C1H	1	1	0	0	0	0	0	1	
64-71	Manufacture's JEDEC ID code										
72	Manufacturing location										
73-90	Manufacture's P/N										
91-92	Revision code										
93-94	Manufacturing date										
95-98	Assembly serial number										
99-125	Mfg specific										
126	Intel specification frequency	64H	0	1	1	0	0	1	0	0	
127	Intel specification /CAS latency support	A5H	1	0	1	0	0	1	0	1	

Timing Chart

Refer to the **SYNCHRONOUS DRAM MODULE TIMING CHART Information (M13348E)**.

★ Package Drawing

168-PIN DUAL IN-LINE MODULE (SOCKET TYPE)



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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