NEC

MOS INTEGRATED CIRCUIT
MC-4R128CPE6C

Direct Rambus™ DRAM RIMM™ Module
128M-BYTE (64M-WORD x 16-BIT)

Description

The Direct Rambus RIMM module is a general-purpose high-performance memory module subsystem suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

MC-4R128CPE6C modules consists of eight 128M Direct Rambus DRAM (Direct RDRAM™) devices (μPD488448). These are extremely high-speed CMOS DRAMs organized as 8M words by 16 bits. The use of Rambus Signaling Level (RSL) technology permits 600MHz, 711MHz or 800MHz transfer rates while using conventional system and board design technologies.

Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10 ns per sixteen bytes).

The architecture of the Direct RDRAM enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95 % bus efficiency. The Direct RDRAM's 32 banks support up to four simultaneous transactions per device.

Features

- 184 edge connector pads with 1mm pad spacing

- 128 MB Direct RDRAM storage

- Each RDRAM® has 32 banks, for 256 banks total on module

- Gold plated contacts

- RDRAMs use Chip Scale Package (CSP)

- Serial Presence Detect support

- Operates from a 2.5 V supply

- Low power and powerdown self refresh modes

- Separate Row and Column buses for higher efficiency

- Over Drive Factor (ODF) support

The mark ★ shows major revised points.

Order information

Part number	Organization	I/O Freq. MHz	RAS access time ns	Package	Mounted devices
MC-4R128CPE6C - 845	64M x 16	800	45	184 edge connector pads RIMM	8 pieces of
MC-4R128CPE6C - 745		711	45	with heat spreader	μPD488448FF
MC-4R128CPE6C - 653		600	53	Edge connector : Gold plated	FBGA (μBGA®) package

Module Pad Configuration

Side B		Side A
B1 — GND	GND — A1	
B2 — LDQA7	LDQA8 — A2	
B3 — GND	GND — A3	
B4 — LDQA5	LDQA6 — A4	
B5 — GND	GND — A5	
B6 — LDQA3	LDQA4 — A6	
B7 — GND	GND — A7	
B8 — LDQA1	LDQA2 — A8	
B9 — GND	GND — A9	
B10 — LCFM	LDQA0 — A10	
B11 — GND	GND — A11	
B12 — LCFMN	LCTMN — A12	
B13 — GND	GND — A13	
B14 — NC	LCTM — A14	
B15 — GND	GND — A15	
B16 — LROW2	NC — A16	
B17 — GND	GND — A17	
B18 — LROW0	LROW1 — A18	
B19 — GND	GND — A19	
B20 — LCOL3	LCOL4 — A20	
B21 — GND	GND — A21	
B22 — LCOL1	LCOL2 — A22	
B23 — GND	GND — A23	
B24 — LDQB0	LCOL0 — A24	
B25 — GND	GND — A25	
B26 — LDQB2	LDQB1 — A26	
B27 — GND	GND — A27	
B28 — LDQB4	LDQB3 — A28	
B29 — GND	GND — A29	
B30 — LDQB6	LDQB5 — A30	
B31 — GND	GND — A31	
B32 — LDQB8	LDQB7 — A32	
B33 — GND	GND — A33	
B34 — LCMD	LSCK — A34	
B35 — Vcmos	Vcmos — A35	
B36 — SIN	SOUT — A36	
B37 — Vcmos	Vcmos — A37	
B38 — NC	NC — A38	
B39 — GND	GND — A39	
B40 — NC	NC — A40	
B41 — Vdd	Vdd — A41	
B42 — Vdd	Vdd — A42	
B43 — NC	NC — A43	
B44 — NC	NC — A44	
B45 — NC	NC — A45	
B46 — NC	NC — A46	

Side B		Side A
B47 — NC	NC — A47	
B48 — NC	NC — A48	
B49 — NC	NC — A49	
B50 — NC	NC — A50	
B51 — Vref	Vref — A51	
B52 — GND	GND — A52	
B53 — SA0	SCL — A53	
B54 — Vdd	Vdd — A54	
B55 — SA1	SDA — A55	
B56 — SVdd	SVdd — A56	
B57 — SA2	SWP — A57	
B58 — Vdd	Vdd — A58	
B59 — RCMD	RSCK — A59	
B60 — GND	GND — A60	
B61 — RDQB8	RDQB7 — A61	
B62 — GND	GND — A62	
B63 — RDQB6	RDQB5 — A63	
B64 — GND	GND — A64	
B65 — RDQB4	RDQB3 — A65	
B66 — GND	GND — A66	
B67 — RDQB2	RDQB1 — A67	
B68 — GND	GND — A68	
B69 — RDQB0	RCOL0 — A69	
B70 — GND	GND — A70	
B71 — RCOL1	RCOL2 — A71	
B72 — GND	GND — A72	
B73 — RCOL3	RCOL4 — A73	
B74 — GND	GND — A74	
B75 — RROW0	RROW1 — A75	
B76 — GND	GND — A76	
B77 — RROW2	NC — A77	
B78 — GND	GND — A78	
B79 — NC	RCTM — A79	
B80 — GND	GND — A80	
B81 — RCFMN	RCTMN — A81	
B82 — GND	GND — A82	
B83 — RCFM	RDQA0 — A83	
B84 — GND	GND — A84	
B85 — RDQA1	RDQA2 — A85	
B86 — GND	GND — A86	
B87 — RDQA3	RDQA4 — A87	
B88 — GND	GND — A88	
B89 — RDQA5	RDQA6 — A89	
B90 — GND	GND — A90	
B91 — RDQA7	RDQA8 — A91	
B92 — GND	GND — A92	

LCFM, LCFMN,
RCFM, RCFMN : Clock from master
LCTM, LCTMN,
RCTM, RCTMN : Clock to master
LCMD, RCMD : Serial Command Pad
LROW2 - LROW0,
RROW2 - RROW0 : Row bus
LCOL4 - LCOL0,
RCOL4 - RCOL0 : Column bus
LDQA8 - LDQA0,
RDQA8 - RDQA0 : Data bus A
LDQB8 - LDQB0,
RDQB8 - RDQB0 : Data bus B
LSCK, RSCK : Clock input
SA0 - SA2 : Serial Presence Detect Address
SCL, SDA : Serial Presence Detect Clock
SIN, SOUT : Serial I/O
SVDD : SPD Voltage
SWP : Serial Presence Detect Write Protect
VCMOS : Supply voltage for serial pads
VDD : Supply voltage
VREF : Logic threshold
GND : Ground reference
NC : These pads are not connected

Module Pad Names

Pad	Signal Name	Pad	Signal Name	Pad	Signal Name	Pad	Signal Name
A1	GND	B1	GND	A47	NC	B47	NC
A2	LDQA8	B2	LDQA7	A48	NC	B48	NC
A3	GND	B3	GND	A49	NC	B49	NC
A4	LDQA6	B4	LDQA5	A50	NC	B50	NC
A5	GND	B5	GND	A51	V_{REF}	B51	V_{REF}
A6	LDQA4	B6	LDQA3	A52	GND	B52	GND
A7	GND	B7	GND	A53	SCL	B53	SA0
A8	LDQA2	B8	LDQA1	A54	V_{DD}	B54	V_{DD}
A9	GND	B9	GND	A55	SDA	B55	SA1
A10	LDQA0	B10	LCFM	A56	SV_{DD}	B56	SV_{DD}
A11	GND	B11	GND	A57	SWP	B57	SA2
A12	LCTMN	B12	LCFMN	A58	V_{DD}	B58	V_{DD}
A13	GND	B13	GND	A59	RSCK	B59	RCMD
A14	LCTM	B14	NC	A60	GND	B60	GND
A15	GND	B15	GND	A61	RDQB7	B61	RDQB8
A16	NC	B16	LROW2	A62	GND	B62	GND
A17	GND	B17	GND	A63	RDQB5	B63	RDQB6
A18	LROW1	B18	LROW0	A64	GND	B64	GND
A19	GND	B19	GND	A65	RDQB3	B65	RDQB4
A20	LCOL4	B20	LCOL3	A66	GND	B66	GND
A21	GND	B21	GND	A67	RDQB1	B67	RDQB2
A22	LCOL2	B22	LCOL1	A68	GND	B68	GND
A23	GND	B23	GND	A69	RCOL0	B69	RDQB0
A24	LCOL0	B24	LDQB0	A70	GND	B70	GND
A25	GND	B25	GND	A71	RCOL2	B71	RCOL1
A26	LDQB1	B26	LDQB2	A72	GND	B72	GND
A27	GND	B27	GND	A73	RCOL4	B73	RCOL3
A28	LDQB3	B28	LDQB4	A74	GND	B74	GND
A29	GND	B29	GND	A75	RROW1	B75	RROW0
A30	LDQB5	B30	LDQB6	A76	GND	B76	GND
A31	GND	B31	GND	A77	NC	B77	RROW2
A32	LDQB7	B32	LDQB8	A78	GND	B78	GND
A33	GND	B33	GND	A79	RCTM	B79	NC
A34	LSCK	B34	LCMD	A80	GND	B80	GND
A35	V_{CMOS}	B35	V_{CMOS}	A81	RCTMN	B81	RCFMN
A36	SOUT	B36	SIN	A82	GND	B82	GND
A37	V_{CMOS}	B37	V_{CMOS}	A83	RDQA0	B83	RCFM
A38	NC	B38	NC	A84	GND	B84	GND
A39	GND	B39	GND	A85	RDQA2	B85	RDQA1
A40	NC	B40	NC	A86	GND	B86	GND
A41	V_{DD}	B41	V_{DD}	A87	RDQA4	B87	RDQA3
A42	V_{DD}	B42	V_{DD}	A88	GND	B88	GND
A43	NC	B43	NC	A89	RDQA6	B89	RDQA5
A44	NC	B44	NC	A90	GND	B90	GND
A45	NC	B45	NC	A91	RDQA8	B91	RDQA7
A46	NC	B46	NC	A92	GND	B92	GND

Module Connector Pad Description (1/2)

Signal	I/O	Type	Description
GND	—	—	Ground reference for RDRAM core and interface. 72 PCB connector pads.
LCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	I	V$_{CMOS}$	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4..LCOL0	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8..LDQA0	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices.
LDQB8..LDQB0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices.
LROW2..LROW0	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	I	V$_{CMOS}$	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
NC	—	—	These pads are not connected. These 24 connector pads are reserved for future use.
RCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
RCMD	I	V$_{CMOS}$	Serial Command Input used to read from and write to the control registers. Also used for power management.
RCOL4..RCOL0	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8..RDQA0	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices.
RDQB8..RDQB0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices.
RROW2..RROW0	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.

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Signal	I/O	Type	Description
RSCK	I	V_{CMOS}	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	I	SV_{DD}	Serial Presence Detect Address 1.
SA2	I	SV_{DD}	Serial Presence Detect Address 2.
SCL	I	SV_{DD}	Serial Presence Detect Clock.
SDA	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O).
SIN	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{DD}	—	—	SPD Voltage. Used for signals SCL, SDA, SWP, SA0, SA1 and SA2.
SWP	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	—	—	CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
V_{DD}	—	—	Supply voltage for the RDRAM core and interface logic.
V_{REF}	—	—	Logic threshold reference voltage for RSL signals.

Block Diagram

Remarks 1. Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.

2. See Serial Presence Detection Specification for information on the SPD device and its contents.

Electrical Specification

Absolute Maximum Ratings

Symbol	Parameter	MIN.	MAX.	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to GND	−0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$	Voltage on V_{DD} with respect to GND	−0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	−50	+100	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Recommended Electrical Conditions

Symbol	Parameter and conditions		MIN.	MAX.	Unit
V_{DD}	Supply voltage		2.50 − 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O power supply at pad	2.5V controllers	2.5 − 0.13	2.5 + 0.25	V
		1.8V controllers	1.8 − 0.1	1.8 + 0.2	
V_{REF}	Reference voltage		1.4 − 0.2	1.4 + 0.2	V
V_{IL}	RSL input low voltage		V_{REF} − 0.5	V_{REF} − 0.2	V
V_{IH}	RSL input high voltage		V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL,CMOS}$	CMOS input low voltage		−0.3	$0.5V_{CMOS}$ − 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage		$0.5V_{CMOS}$+0.25	V_{CMOS} + 0.3	V
$V_{OL,CMOS}$	CMOS output low voltage, $I_{OL,CMOS}$ = 1 mA		—	0.3	V
$V_{OH,CMOS}$	CMOS output high voltage, $I_{OH,CMOS}$ = −0.25 mA		V_{CMOS} − 0.3	—	V
I_{REF}	V_{REF} current, $V_{REF,MAX}$		−80.0	+80.0	μA
$I_{SCK,CMD}$	CMOS input leakage current, $(0 \leq V_{CMOS} \leq V_{DD})$		−80.0	+80.0	μA
$I_{SIN,SOUT}$	CMOS input leakage current, $(0 \leq V_{CMOS} \leq V_{DD})$		−10.0	+10.0	μA

AC Electrical Specifications

	Symbol	Parameter and Conditions		MIN.	TYP.	MAX.	Unit
★	Z	Module Impedance		25.2	28	30.8	Ω
★	T_{PD}	Average clock delay from finger to finger of all RSL clock nets	-845			1.50	ns
★		(CTM, CTMN,CFM, and CFMN)	-745			1.50	
			-653			1.60	
	ΔT_{PD}	Propagation delay variation of RSL signals with respect to TPD [Note1,2]		−21		+21	ps
	$\Delta T_{PD-CMOS}$	Propagation delay variation of SCK and CMD signals with respect to an average clock delay [Note1]		−100		+100	ps
	V_α/V_{IN}	Attenuation Limit	-845			16	%
			-745			16	
			-653			10	
	V_{XF}/V_{IN}	Forward crosstalk coefficient	-845			4	%
		(300ps input rise time 20% - 80%)	-745			4	
			-653			4	
	V_{XB}/V_{IN}	Backward crosstalk coefficient	-845			2.0	%
		(300ps input rise time 20% - 80%)	-745			2.0	
			-653			2.0	
	R_{DC}	DC Resistance Limit	-845			0.8	Ω
			-745			0.8	
			-653			0.8	

Notes 1. TPD or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

    2. If the RIMM module meets the following specification, then it is compliant to the specification.

    If the RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔTPD Specification" table.

Adjusted ΔT$_{PD}$ Specification

Symbol	Parameter and conditions	Adjusted MIN./MAX.	Absolute		Unit
			MIN.	MAX.	
ΔT_{PD}	Propagation delay variation of RSL signals with respect to TPD	+/− [17+(18*N*ΔZ0)] [Note]	−30	+30	ps

Note N = Number of RDRAM devices installed on the RIMM module.

    ΔZ0 = delta Z0% = (MAX. Z0 − MIN. Z0) / (MIN. Z0)

    (MAX. Z0 and MIN. Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the module.)

RIMM Module Current Profile

I_{DD}	RIMM module power conditions [Note1]		MAX.	Unit
I_{DD1}	One RDRAM in Read [Note2], balance in NAP mode	-845	719.4	mA
		-745	654.4	
		-653	569.4	
I_{DD2}	One RDRAM in Read [Note2], balance in Standby mode	-845	1,460	mA
		-745	1,360	
		-653	1,205	
I_{DD3}	One RDRAM in Read [Note2], balance in Active mode	-845	1,950	mA
		-745	1,780	
		-653	1,555	
I_{DD4}	One RDRAM in Write, balance in NAP mode	-845	679.4	mA
		-745	624.4	
		-653	544.4	
I_{DD5}	One RDRAM in Write, balance in Standby mode	-845	1,420	mA
		-745	1,330	
		-653	1,180	
I_{DD6}	One RDRAM in Write, balance in Active mode	-845	1,910	mA
		-745	1,750	
		-653	1,530	

Notes 1. Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Power does not include Refresh Current.

    2. I/O current is a function of the % of 1's, to add I/O power for 50 % 1's for a x16 need to add 257 mA for the following : V_{DD} = 2.5 V, V_{TERM} = 1.8 V, V_{REF} = 1.4 V and V_{DIL} = V_{REF} − 0.5 V.

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Timing Parameters

The following timing parameters are from the RDRAMs pins, not the RIMM. Please refer to the RDRAM data sheet (μPD488448) for detailed timing diagrams.

Parameter	Description	MIN. -845	MIN. -745	MIN. -653	MAX.	Units
t_{RC}	Row Cycle time of RDRAM banks - the interval between ROWA packets with ACT commands to the same bank.	28	28	28	—	t_{CYCLE}
t_{RAS}	RAS-asserted time of RDRAM bank - the interval between ROWA packet with ACT command and next ROWR packet with PRER[Note 1] command to the same bank.	20	20	20	$64\mu s$ [Note 2]	t_{CYCLE}
t_{RP}	Row Precharge time of RDRAM banks - the interval between ROWR packet with PRER[Note 1] command and next ROWA packet with ACT command to the same bank.	8	8	8	—	t_{CYCLE}
t_{PP}	Precharge-to-precharge time of RDRAM device - the interval between successive ROWR packets with PRER[Note 1] commands to any banks of the same device.	8	8	8	—	t_{CYCLE}
t_{RR}	RAS-to-RAS time of RDRAM device - the interval between successive ROWA packets with ACT commands to any banks of the same device.	8	8	8	—	t_{CYCLE}
t_{RCD}	RAS-to-CAS Delay - the interval from ROWA packet with ACT command to COLC packet with RD or WR command. Note - the RAS-to-CAS delay seen by the RDRAM core (t_{RCD-C}) is equal to $t_{RCD-C} = 1 + t_{RCD}$ because of differences in the row and column paths through the RDRAM interface.	9	7	7	—	t_{CYCLE}
t_{CAC}	CAS Access delay - the interval from RD command to Q read data. The equation for t_{CAC} is given in the TPARM register.	8	8	8	12	t_{CYCLE}
t_{CWD}	CAS Write Delay - interval from WR command to D write data.	6	6	6	6	t_{CYCLE}
t_{CC}	CAS-to-CAS time of RDRAM bank - the interval between successive COLC commands.	4	4	4	—	t_{CYCLE}
t_{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet.	4	4	4	4	t_{CYCLE}
t_{RTR}	Interval from COLC packet with WR command to COLC packet which causes retire, and to COLM packet with bytemask.	8	8	8	—	t_{CYCLE}
t_{OFFP}	The interval (offset) from COLC packet with RDA command, or from COLC packet with retire command (after WRA automatic precharge), or from COLC packet with PREC command, or from COLX packet with PREX command to the equivalent ROWR packet with PRER. The equation for t_{OFFP} is given in the TPARM register.	4	4	4	4	t_{CYCLE}
t_{RDP}	Interval from last COLC packet with RD command to ROWR packet with PRER.	4	4	4	—	t_{CYCLE}
t_{RTP}	Interval from last COLC packet with automatic retire command to ROWR packet with PRER.	4	4	4	—	t_{CYCLE}

Notes 1. Or equivalent PREC or PREX command.

2. This is a constraint imposed by the core, and is therefore in units of ms rather than t_{CYCLE}.

★ **Standard RIMM Module Marking**

The RIMM modules available from NEC are marked per Figure 1 below. This marking assists users to specify and verify if the correct RIMM modules are installed in their systems. In the diagram, a label is shown attached to the RIMM module's heat spreader. Information contained on the label is specific to the RIMM module and provides RDRAM information without requiring removal of the RIMM module's heat spreader.

Figure 1. RIMM Module marking example
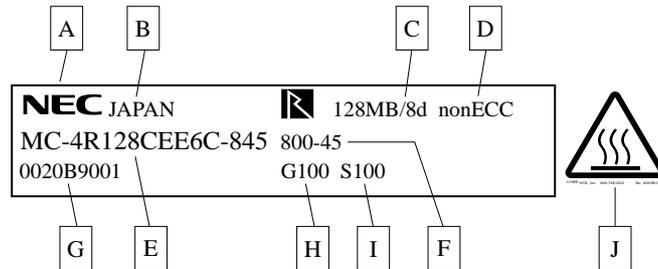
	Label Field	Description	Marked Text	Units
A	Vendor logo	Vendor logo area	NEC	–
B	Manufacturing Country	Country of origin	JAPAN, USA, FRANCE	–
C	Module Memory Capacity	Number of 8-bit or 9-bit MBytes of RDRAM storage in RIMM module	64MB, 96MB, 128MB, 192MB, 256MB	MBytes
	Number of RDRAMs	Number of RDRAM devices contained in the RIMM module	/4d, /6d, /8d, /12d, /16d	RDRAM devices
D	ECC Support	Indicates whether the RIMM module supports 8-bit (non ECC) or 9-bit (ECC) Bytes	non ECC, ECC	–
E	Part No.	NEC RIMM Part No.	See table **Order information**	–
F	Memory Speed	Data transfer speed for RIMM module	800, 711, 600	MHz
	t_{RAC}	Row Access Time	-45, -53	ns
G	Manufacturing Lot No.	Manufactured Year code, Week code, In-house code	YYWW*****	–
H	Gerber Version	PCB Gerber file revision used on RIMM Module	G100 as Rev 1.00	–
I	SPD Version	SPD code version	S100 as Rev 1.00	–
J	Caution Logo	–	–	–

Package Drawings

184 EDGE CONNECTOR PADS RIMM (SOCKET TYPE) (1/2)

detail of Ⓐ part

detail of Ⓑ part
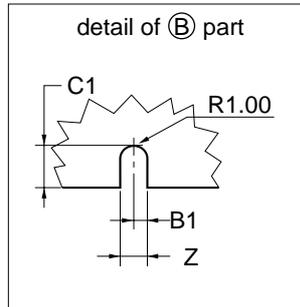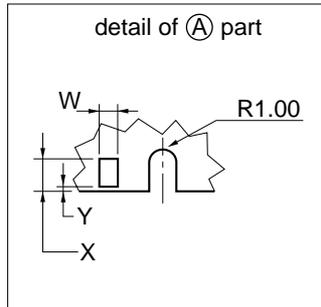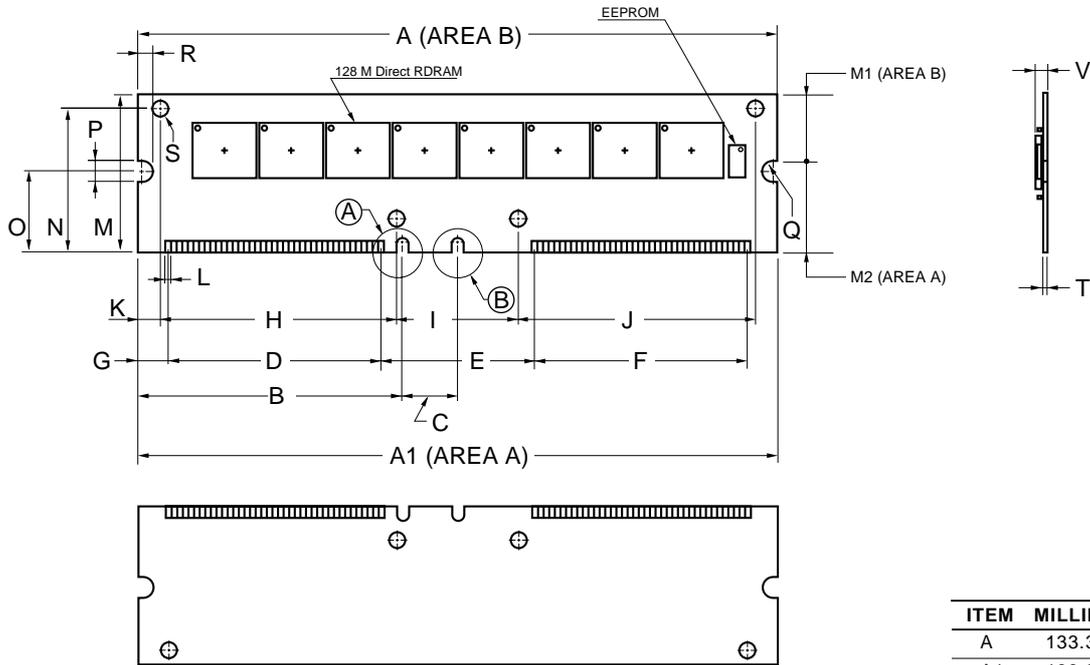
ITEM	MILLIMETERS
A	133.35 TYP.
A1	133.35±0.13
B	55.175
B1	1.00±0.10
C	11.50
C1	3.00±0.10
D	45.00
E	32.00
F	45.00
G	5.675
H	47.625
I	25.40
J	47.625
K	6.35
L	1.00 TYP.
M	31.75±0.13
M1	11.97
M2	19.78
N	29.21
O	17.78
P	4.00±0.10
Q	R 2.00
R	3.00±0.10
S	ϕ 2.44
T	1.27±0.10
V	2.43 MAX.
W	0.80±0.10
X	2.99
Y	0.15
Z	2.00±0.10

184 EDGE CONNECTOR PADS RIMM (SOCKET TYPE) (2/2)
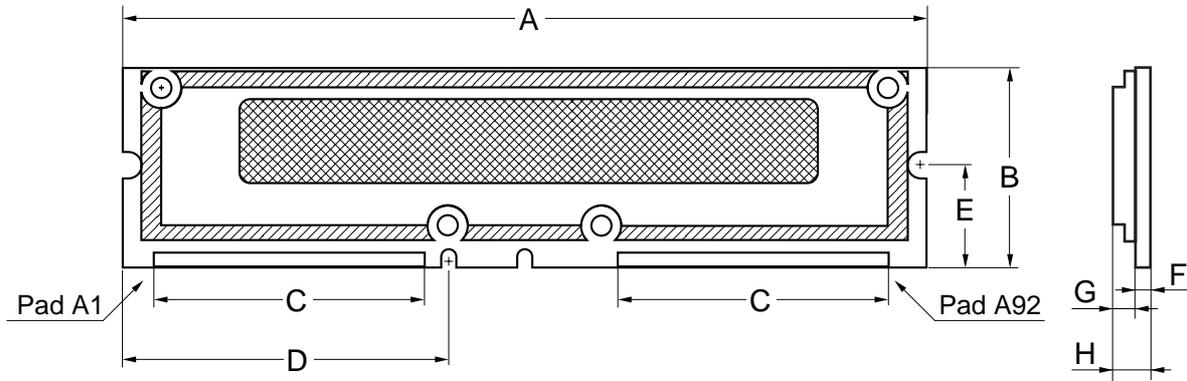
ITEM	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
A	PCB length	133.22	133.35	133.48	mm
B	PCB height for 1.25" RIMM Module	31.62	31.75	31.88	mm
C	Center-center pad width from pad A1 to A46, A47 to A92, B1 to B46 or B47 to B92	44.95	45.00	45.05	mm
D	Spacing from PCB left edge to connector key notch	-	55.175	-	mm
E	Spacing from contact pad PCB edge to side edge retainer notch	-	17.78	-	mm
F	PCB thickness	1.17	1.27	1.37	mm
G	Heat spreader thickness from PCB surface (one side) to heat spreader top surface	-	-	3.09	mm
H	RIMM thickness	-	-	4.46	mm

─── **NOTES FOR CMOS DEVICES** ───

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**
Note:
Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**
Note:
No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**
Note:
Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.