DATA SHEET

NEC

HYBRID INTEGRATED CIRCUIT

MC-9400A

320 (240)-BIT AC- PDP DRIVER MODULE

DESCRIPTION

The MC-9400A is a PDP driver module that incorporates five 64-bit high breakdown voltage output (150 V, 40 mA) CMOS driver ICs. It supports 320 outputs in the case of 4-bit parallel input, and 240 outputs in the case of 3-bit parallel input.

The integrated structure of the MC-9400A, which combines a COB with an aluminum heat sink and an output flexible printed circuit (FPC) board, enables the easy implementation of heat dissipation measures and high-density mounting.

FEATURES

- Incorporates five μPD16337s with four 16-bit bi-directional shift registers
- Low thermal resistance realized by chip-on-metal structure
- Provided with connector and capacitor for easy mounting on a panel
- Supports output electrode with a narrow pitch through use of a flexible printed circuit board
- Polarity of all driver outputs can be inverted through use of /PC pins
- Supports custom modules

Remark /XXX indicates active low.

ORDERING INFORMATION

Part Number	Package
MC-9400A	COB

The information in this document is subject to change without notice.

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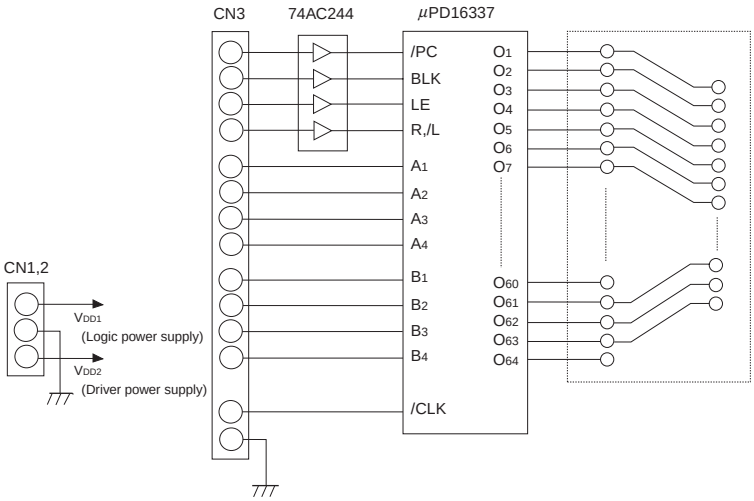
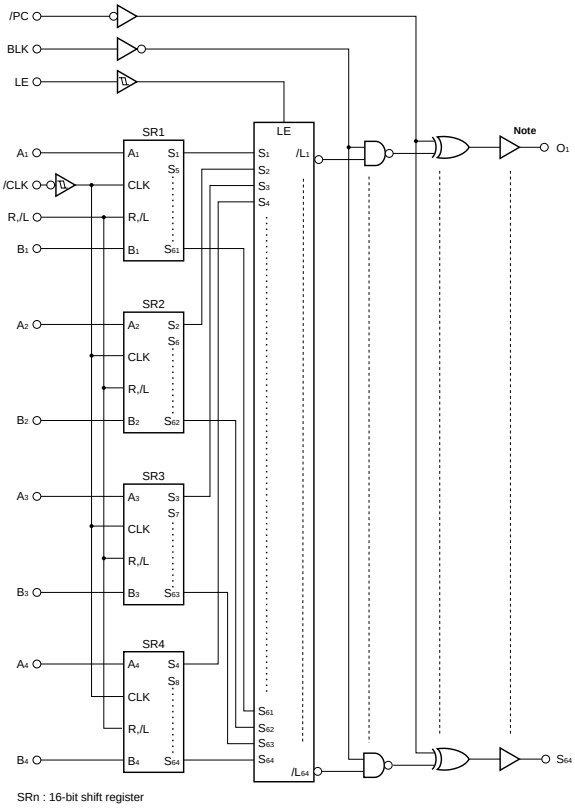
The mark ★ shows major revised points.

BLOCK DIAGRAM (1/5 CIRCUIT)



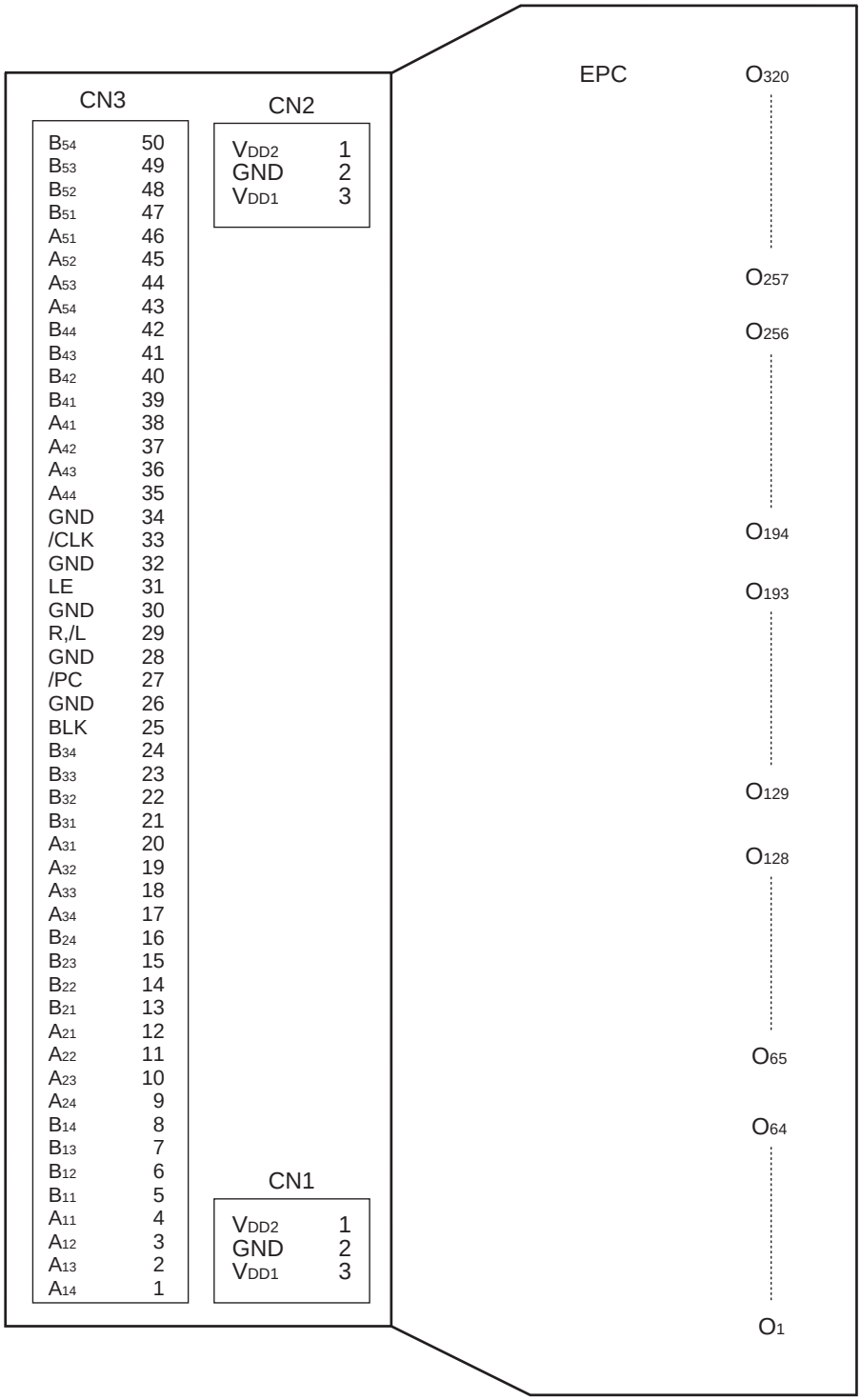
Remark Five μPD16337s incorporated : 240 outputs at 3 ch and 320 outputs at 4 ch.
See the following block diagram for the μPD16337.

μPD16337 BLOCK DIAGRAM



Note High breakdown voltage CMOS driver 150V, ±40 mA(MAX.).

★ PIN CONFIGURATION (Top View)



Caution To prevent latch-up breakage, be sure to turn the power on in the order of V_{DD1}, logic signal, and V_{DD2}, and turn the power off in the reverse order. Keep this order also during a transition period.

PIN FUNCTIONS

Pin Symbol	Pin Name	Pin No.	I/O	Description
/PC	Polarity inverted input	27	CN3	/PC = L : Polarity of all outputs inverted
BLK	Blanking input	25	CN3	BLK = H : All outputs = H or L
LE	Latch enable input	31	CN3	Automatically latches by a high level input at the rising edge of the clock
A_{11} to A_{14}, A_{21} to A_{24}, A_{31} to A_{34}, A_{41} to A_{44}, A_{51} to A_{54}	RIGHT data input	1 to 4 9 to 12 17 to 20 35 to 38 46	CN3	When R,/L = H A_{11} to A_{14}, A_{21} to A_{24}, A_{31} to A_{34}, A_{41} to A_{44}, A_{51} to A_{54} : Input B_{11} to B_{14}, B_{21} to B_{24}, B_{31} to B_{34}, B_{41} to B_{44}, B_{51} to B_{54} : Output When R,/L = L A_{11} to A_{14}, A_{21} to A_{24}, A_{31} to A_{34}, A_{41} to A_{44}, A_{51} to A_{54} : Output B_{11} to B_{14}, B_{21} to B_{24}, B_{31} to B_{34}, B_{41} to B_{44}, B_{51} to B_{54} : Input
B_{11} to B_{14}, B_{21} to B_{24}, B_{31} to B_{34}, B_{41} to B_{44}, B_{51} to B_{54}	LEFT data input	5 to 8 13 to 16 21 to 24 39 to 42 47 to 50	CN3	
/CLK	Clock input	33	CN3	Executes a shift at the rising edge
R,/L	Shift control input	29	CN3	Right shift mode by H SR_1 : $A_1 \rightarrow S_1$ ... $S_{61} \rightarrow B_1$ (SR_2, SR_3, and SR_4 also same direction) Left shift mode by L SR_1 : $B_1 \rightarrow S_{61}$ ... $S_1 \rightarrow A_1$ (SR_2, SR_3, and SR_4 also same direction)
O_1 to O_{320}	High breakdown voltage output	1 to 320	FPC	150 V, 40mA (MAX.)
V_{DD1}	Logic block power supply	1	CN1 CN2	5 V ± 10 %
V_{DD2}	Driver block power supply	3	CN1 CN2	30 V to 130 V
GND	Ground	2	CN1 CN2	Connected to system ground
		26,28, 30,32, 34	CN3	

TRUTH TABLE

1. Shift register block

Input		Output		Shift register
R,/L	/CLK	A	B	
H	↓	Input	Output[Note1]	Execution of right shift
H	X		Output	Retain
L	↓	Output[Note2]	Input	Execution of left shift
L	X	Output		Retain

Notes 1. On a clock rise, the data S_{57}, S_{58}, S_{59}, and S_{60} are shifted to S_{61}, S_{62}, S_{63}, and S_{64}, and output from B_1, B_2, B_3, and B_4, respectively.

2. On a clock fall, the data S_5, S_6, S_7, and S_8 are shifted to S_1, S_2, S_3, and S_4, and output from A_1, A_2, A_3, and A_4, respectively.

Remark X= H or L, H= High level, L= Low level

2. Latch block

LE	/CLK	Output state of latch block (/Ln)
H	↓	Latches the data of Sn and retains the output data
	↓	Retains the latch data
L	X	Retains the latch data

Remark X= H or L, H= High level, L= Low level

3. Driver block

/Ln	BLK	/PC	Driver output state
X	H	H	H (all driver outputs : H)
X	H	L	L (all driver outputs : L)
X	L	H	Outputs latch data (/Ln)
X	L	L	Outputs latch data (/Ln) with polarity inverted

Remark X= H or L, H= High level, L= Low level

ELECTRICAL CHARACTERISTICS

Absolute maximum ratings (T_A = +25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic block supply voltage	V_{DD1}	– 0.5 to + 7.0	V
Driver block supply voltage	V_{DD2}	– 0.5 to + 150	V
Logic block input voltage	V_I	– 0.5 to V_{DD1} + 0.5	V
Driver block output current	I_{O2}	40	mA
Module allowable power dissipation	$Pd_{MAX.}$	6[Note]	W
Junction temperature	$Tj_{MAX.}$	125	°C
Operating ambient temperature	T_A	– 10 to + 70	°C
Storage temperature	T_{stg}	– 40 to + 85	°C

Note The value when mounting this driver module on the aluminum frame by screw.

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore,specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended operating range (T_A = –10 to + 70°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic block supply voltage	V_{DD1}	4.5	5.0	5.5	V
Driver block supply voltage	V_{DD2}	30		130	V
Input voltage high	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Input voltage low	V_{IL}	0		0.2 V_{DD1}	V
Driver output current	I_{OH2}	–30			mA
	I_{OL2}			+30	mA

Electrical specifications (T_A = +25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage high	V_{OH21}	V_{DD2} = 130 V, I_{OH} = –10 mA		123			V
Output voltage high	V_{OH22}	V_{DD2} = 130 V, I_{OH} = –30 mA		110			V
Output voltage low	V_{OL21}	V_{DD2} = 130 V, I_{OH} = 10 mA				5.0	V
Output voltage low	V_{OL22}	V_{DD2} = 130 V, I_{OH} = 30 mA				15.0	V
Input leakage current (H1) PU	I_{LIH1}	V_{DD1} = 7.0 V, V_{DD2} = 30 V		–4.0		+4.0	μA
Input leakage current (H2) PC	I_{LIH2}	V_{DD1} = 7.0 V, V_{DD2} = 30 V		–4.0		+4.0	μA
Input leakage current (L2) PC	I_{LIL2}	V_{DD1} = 7.0 V, V_{DD2} = 30 V		–4.0		+4.0	μA
Input voltage high	V_{IH}	V_{DD1} = 5.0 V, V_{DD2} = 30 V		3.5			V
Input voltage low	V_{IL}	V_{DD1} = 5.0 V, V_{DD2} = 30 V				1.0	V
Power supply current 1(Logic)	I_{DD1} a1	V_{DD1} = 7.0 V				8	mA
Power supply current 1(Logic)	I_{DD1} –1		In : High Level			80	μA
Power supply current 2 (Driver)	I_{DD2}	V_{DD1} = 5.0 V, V_{DD2} =135 V	Out : ALL Low			500	μA
Power supply current 2 (Driver)	I_{DD2}		Out : ALL High			500	μA
Power supply current 2 (Driver)	I_{DD2}		Out :HLHLLHLH			500	μA
Power supply current 2 (Driver)	I_{DD2}		Out :LHLHHLHL			500	μA

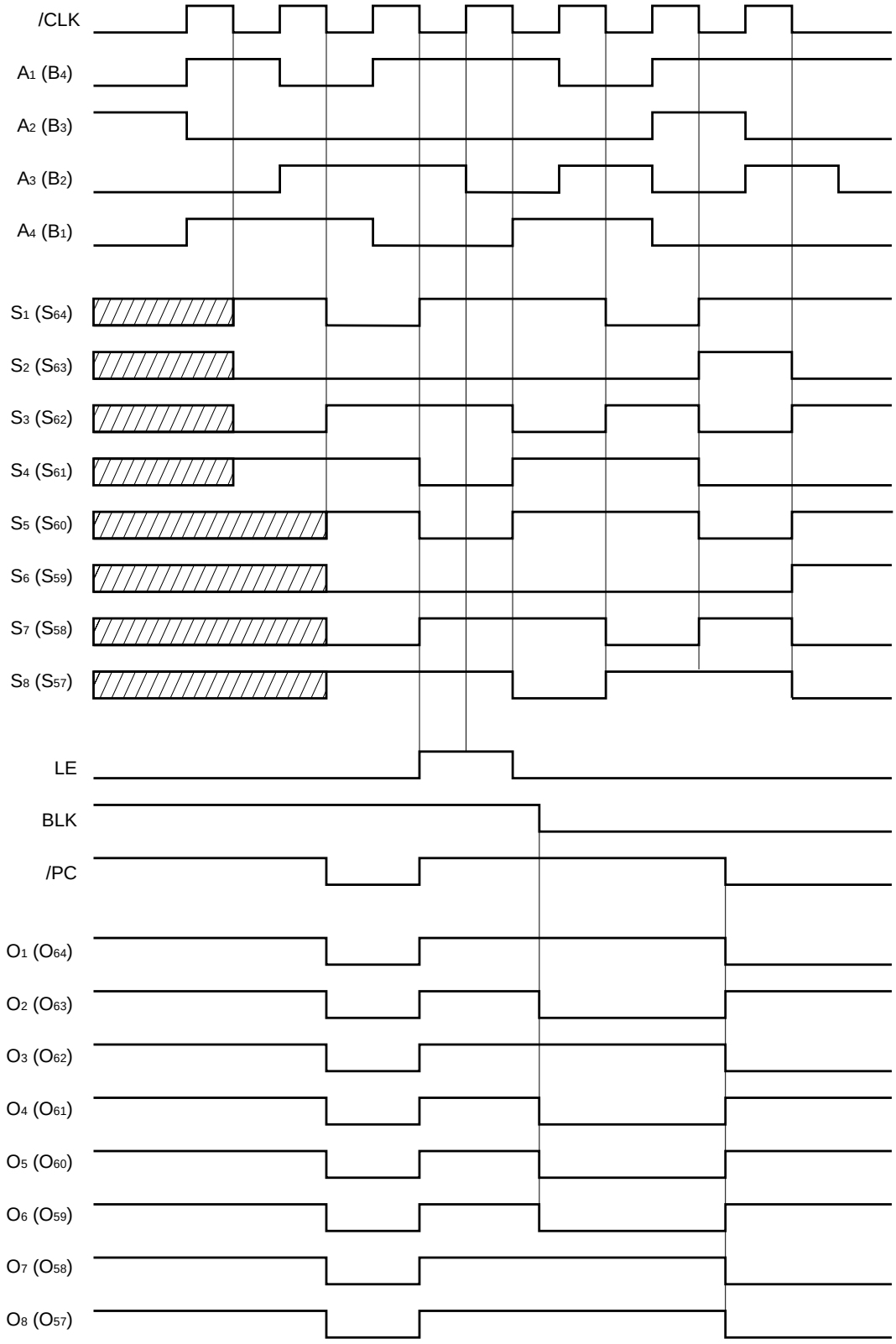
Switching characteristics (T_A = +25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation delay time	t_{PLH2}	V_{DD1} = 5.0 V, V_{DD2} = 130 V			187.5	ns
Propagation delay time	t_{PHL2}	V_{DD1} = 5.0 V, V_{DD2} = 130 V			187.5	ns
Propagation delay time	t_{PLH3}	V_{DD1} = 5.0 V, V_{DD2} = 130 V, BLK→OUT			172.5	ns
Propagation delay time	t_{PHL3}	V_{DD1} = 5.0 V, V_{DD2} = 130 V, BLK→OUT			172.5	ns
Propagation delay time	t_{PLH4}	V_{DD1} = 5.0 V, V_{DD2} = 130 V, PC→OUT			160.0	ns
Propagation delay time	t_{PHL4}	V_{DD1} = 5.0 V, V_{DD2} = 130 V, PC→OUT			160.0	ns
Rise time	t_{TLH}	V_{DD1} = 5.0 V, V_{DD2} = 130 V			200.0	ns
Fall time	t_{THL}	V_{DD1} = 5.0 V, V_{DD2} = 130 V			200.0	ns
Maximum clock frequency	$f_{MAX.}$	V_{DD1} = 4.0 V, V_{DD2} = 30 V	25.0			MHz

Timing requirements (T_A = +25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data setup time 1	t_{SETUP1}	V_{DD1} = 4.5 V, V_{DD2} = 30 V	31.2			ns
Data setup time 2	t_{SETUP2}	V_{DD1} = 4.5 V, V_{DD2} = 30 V	12.0			ns
Data hold time	t_{HOLD}	V_{DD1} = 4.5 V, V_{DD2} = 30 V	8.5			ns
Latch enable time 1	t_{LE1}	V_{DD1} = 4.5 V, V_{DD2} = 30 V	27.5			ns
Latch enable time 2	t_{LE2}	V_{DD1} = 4.5 V, V_{DD2} = 30 V	17.5			ns
Latch enable time 3	t_{LE3}	V_{DD1} = 4.5 V, V_{DD2} = 30 V	27.5			ns
Latch enable time 4	t_{LE4}	V_{DD1} = 4.5 V, V_{DD2} = 30 V	17.5			ns

Timing chart (Right shift)

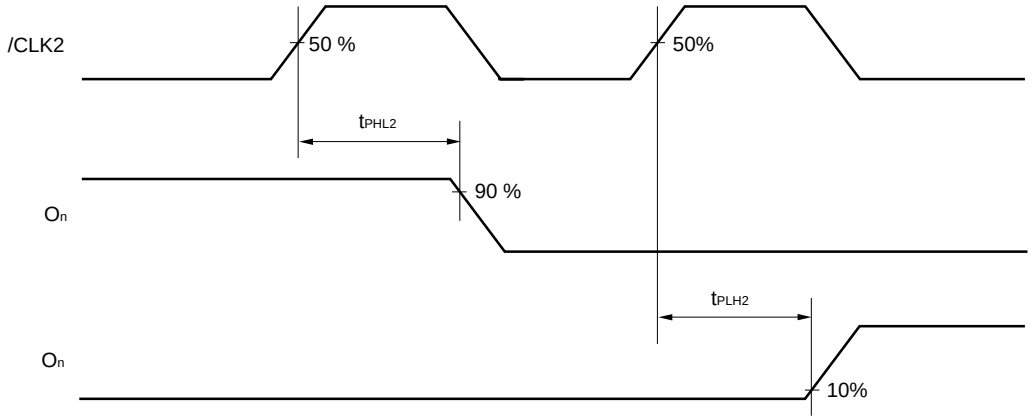


Remark () applies when R,/L = L

Switching characteristics waveform

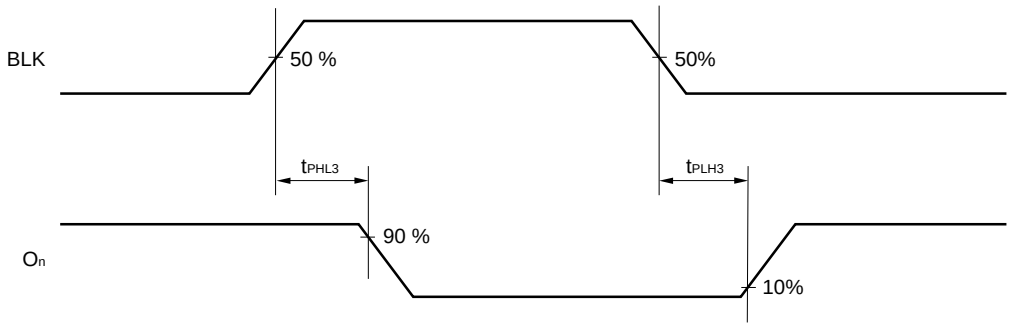
Propagation delay time

t_{PHL2}, t_{PLH2}



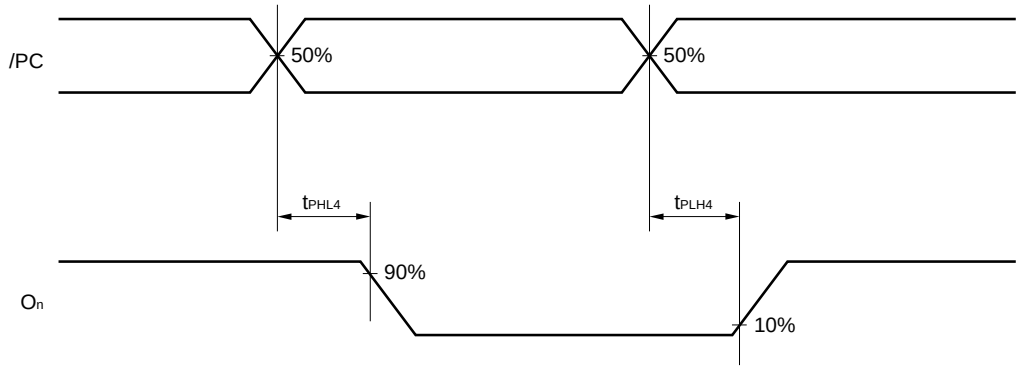
Propagation delay time (BLK → OUT)

t_{PHL3}, t_{PLH3}



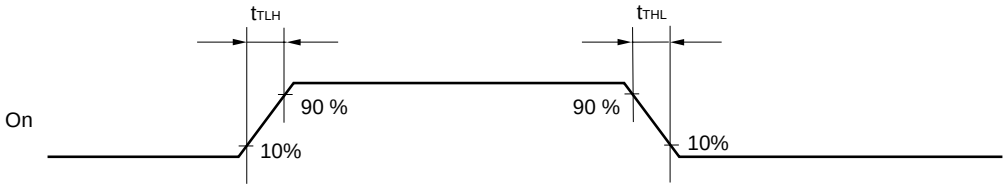
Propagation delay time (/PC → OUT)

t_{PHL4}, t_{PLH4}



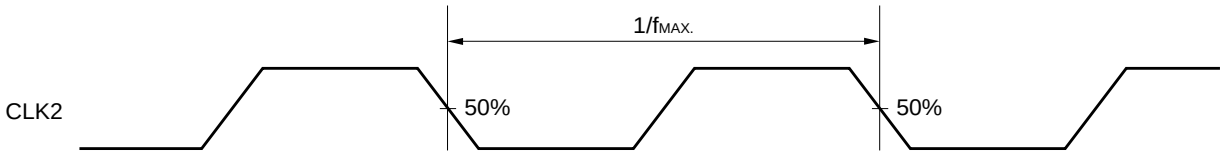
Rise time, Fall time

t_{TLH}, t_{THL}



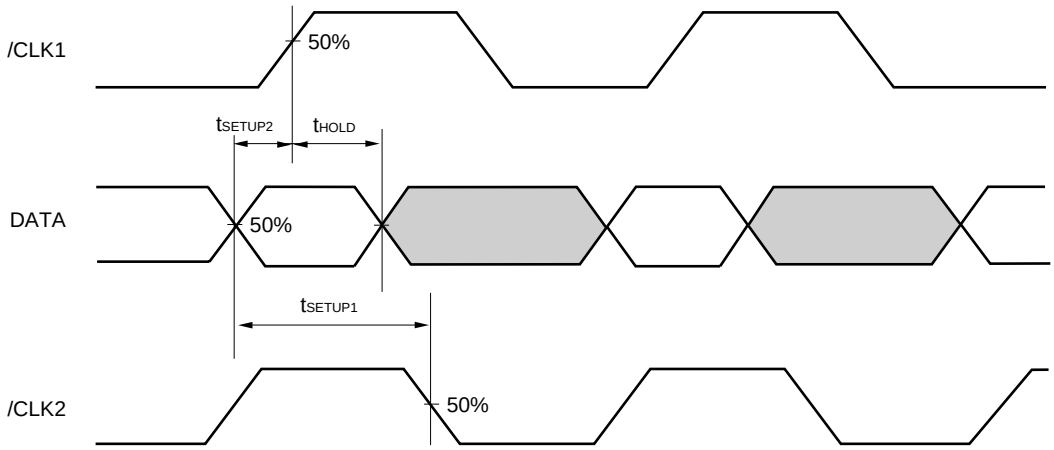
Maximum clock frequency

$F_{MAX.}$



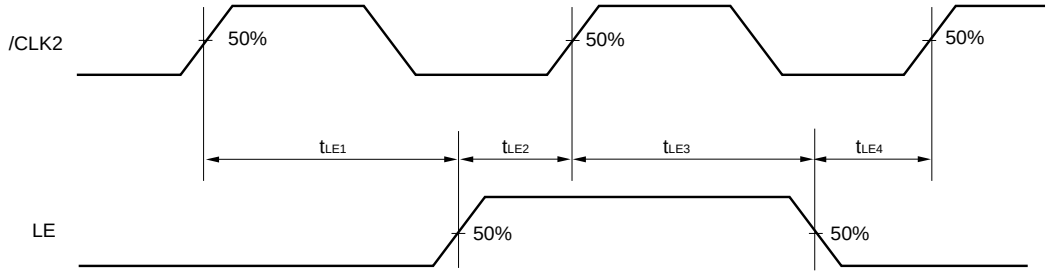
Data setup time1, 2, and Data hold time

t_{SETUP1}, t_{SETUP2}, t_{HOLD}



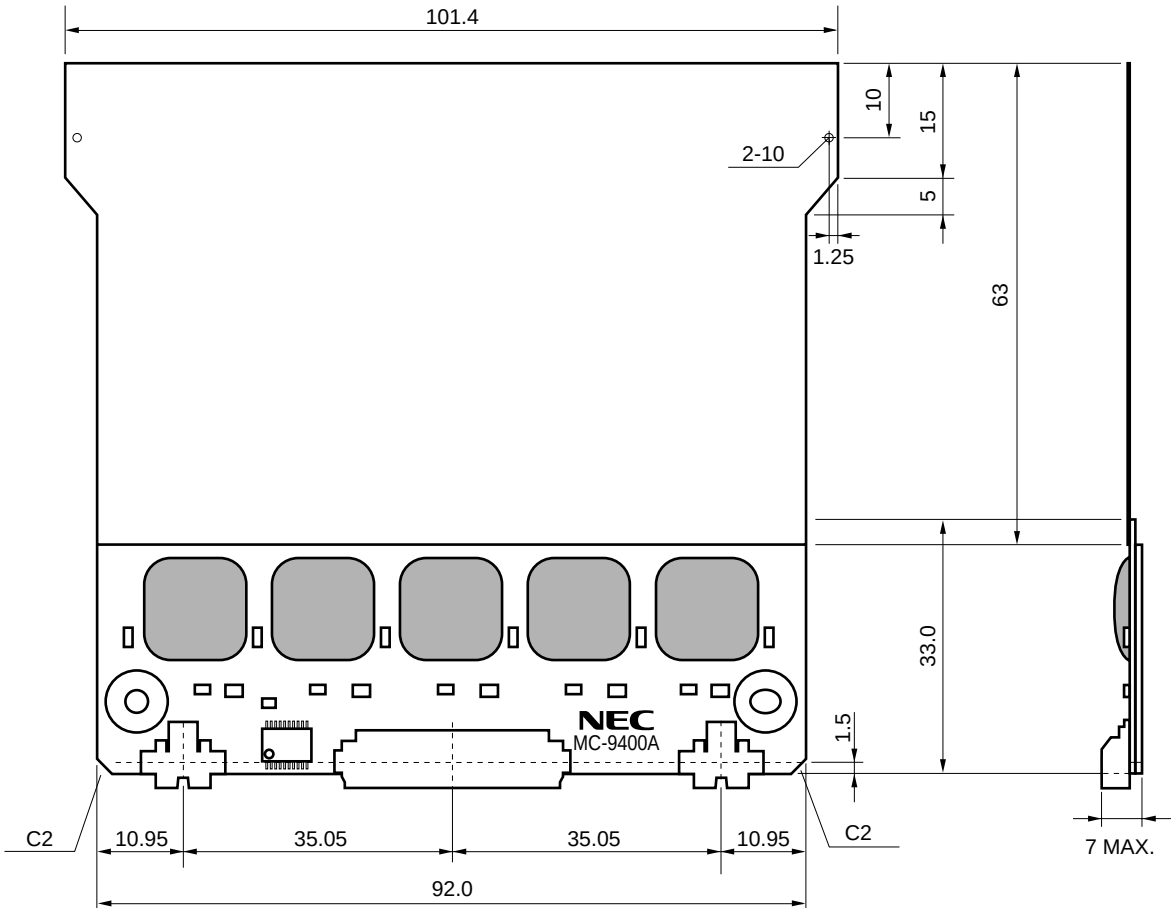
Latch enable time1, 2, 3, 4

t_{LE1}, t_{LE2}, t_{LE3}, t_{LE4}



PACKAGE DRAWING (unit : mm)

COB with radiation board attached + FPC module



[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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