

P-CHANNEL POWER MOS FET ARRAY
SWITCHING
INDUSTRIAL USE

DESCRIPTION

The μ PA1523B is P-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- Full Mold Package with 4 Circuits
- -4 V driving is possible
- Low On-state Resistance
 $R_{DS(on)1} = 0.8 \Omega$ MAX. (@ $V_{GS} = -10$ V, $I_D = -1$ A)
 $R_{DS(on)2} = 1.3 \Omega$ MAX. (@ $V_{GS} = -4$ V, $I_D = -1$ A)
- Low Input Capacitance $C_{iss} = 190$ pF TYP.

ORDERING INFORMATION

Type Number	Package
μ PA1523BH	10 Pin SIP

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

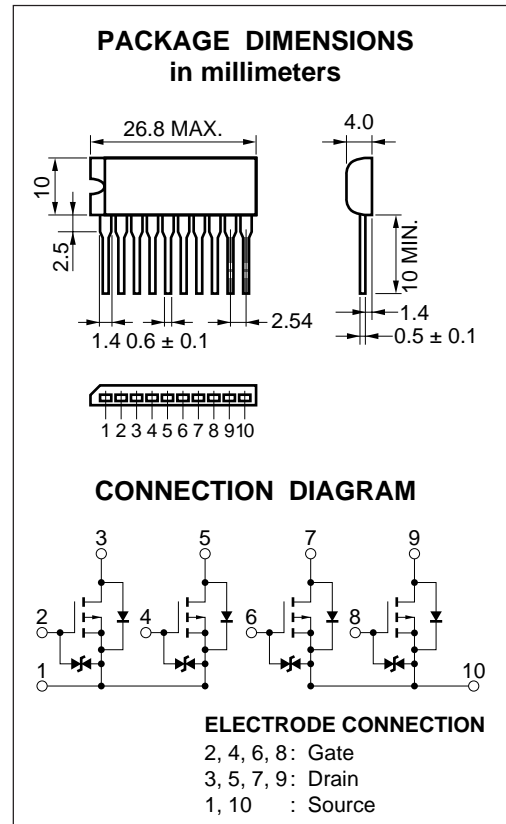
Drain to Source Voltage ($V_{GS} = 0$)	V_{DSS}	-60	V
Gate to Source Voltage ($V_{DS} = 0$)	$V_{GSS(AC)}$	∓ 20	V
Drain Current (DC)	$I_{D(DC)}$	∓ 2.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$ *1	∓ 8.0	A/unit
Total Power Dissipation	P_{T1} *2	28	W
Total Power Dissipation	P_{T2} *3	3.5	W
Channel Temperature	T_{CH}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current	I_{AS} *4	-2.0	A
Single Avalanche Energy	E_{AS} *4	0.4	mJ

*1 $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

*2 4 Circuits, $T_C = 25^\circ\text{C}$

*3 4 Circuits, $T_A = 25^\circ\text{C}$

*4 Starting $T_{CH} = 25^\circ\text{C}$, $V_{DD} = -30$ V, $V_{GS} = -20$ V \rightarrow 0, $R_G = 25 \Omega$,
 $L = 100 \mu H$



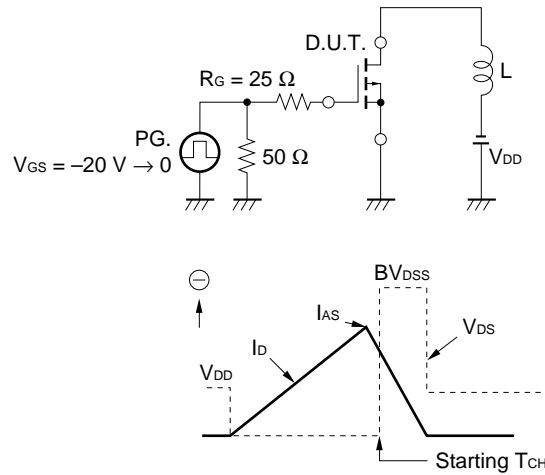
Build-in Gate Diodes are for protection from static electricity in handling.
 In case high voltage over V_{GSS} is applied, please append gate protection circuits.

The information in this document is subject to change without notice.

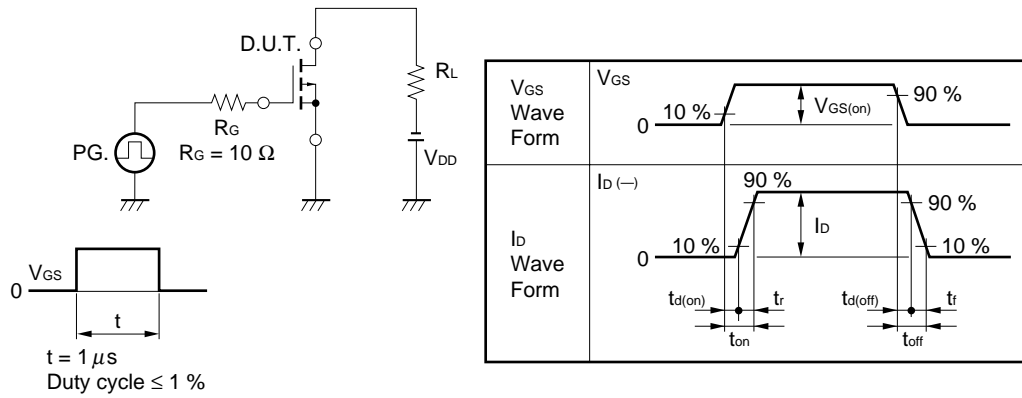
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0			-10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0			±10	μA
Gate Cutoff Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1.0 mA	-1.0		-2.0	V
Forward Transfer Admittance	Y _{fs}	V _{DS} = -10 V, I _D = -1.0 A	0.8			S
Drain to Source ON-Resistance	R _{DS(on)1}	V _{GS} = -10 V, I _D = -1.0 A		0.5	0.8	Ω
Drain to Source ON-Resistance	R _{DS(on)2}	V _{GS} = -4.0 V, I _D = -1.0 A		0.8	1.3	Ω
Input Capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0, f = 1.0 MHz		190		pF
Output Capacitance	C _{oss}			115		pF
Reverse Transfer Capacitance	C _{rss}			43		pF
Turn-on Delay Time	t _{d(on)}	I _D = -1.0 A, V _{GS(on)} = -10 V, V _{DD} ≐ -30 V, R _L = 30 Ω		8		ns
Rise Time	t _r			53		ns
Turn-off Delay Time	t _{d(off)}			400		ns
Fall Time	t _f			230		ns
Total Gate Charge	Q _G	V _{GS} = -10 V, I _D = -2.0 A, V _{DD} = -48 V		10		nC
Gate to Source Charge	Q _{GS}			1.1		nC
Gate to Drain Charge	Q _{GD}			3.5		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 2.0 A, V _{GS} = 0		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 2.0 A, V _{GS} = 0, di/dt = 50 A/μs		180		ns
Reverse Recovery Charge	Q _{rr}			250		nC

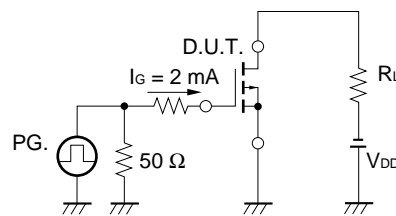
Test Circuit 1 Avalanche Capability



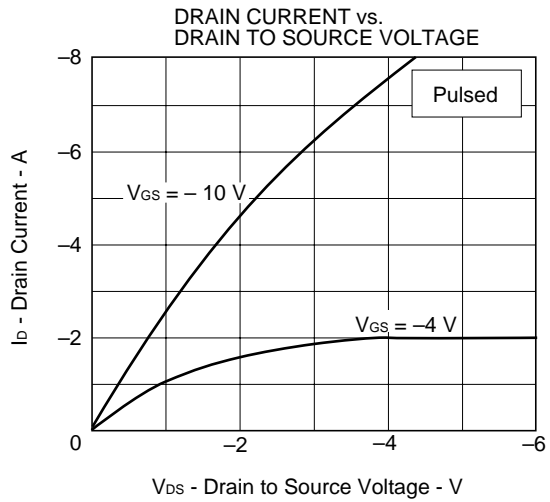
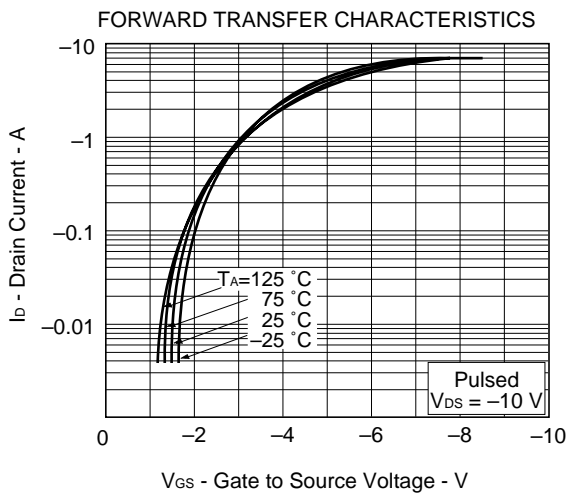
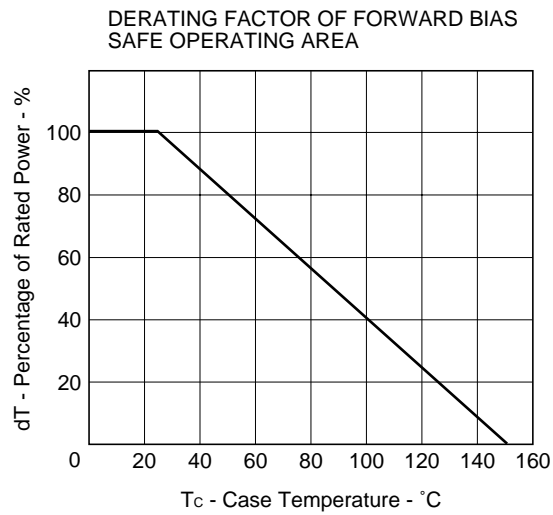
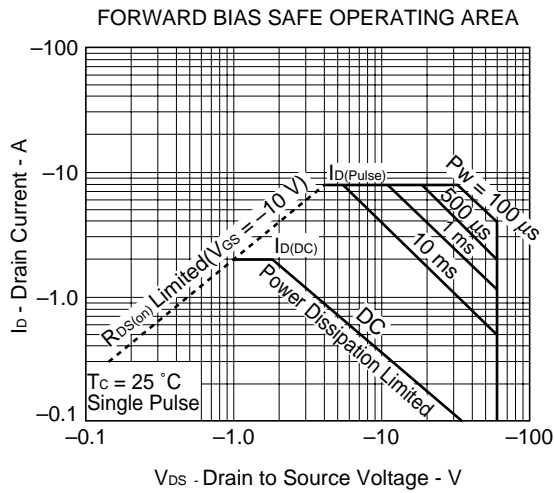
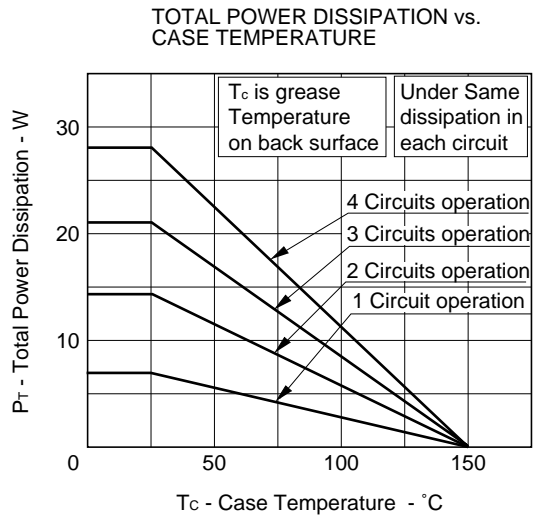
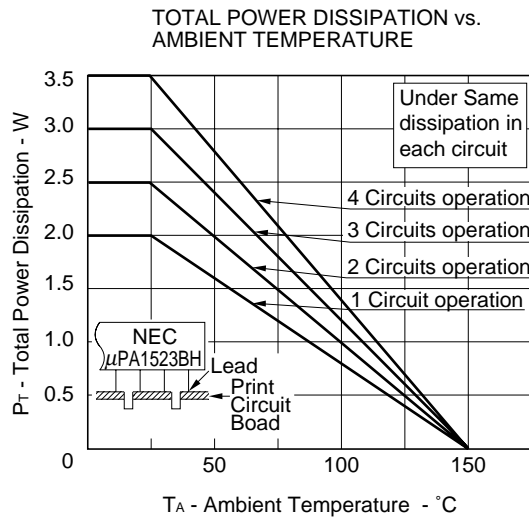
Test Circuit 2 Switching Time



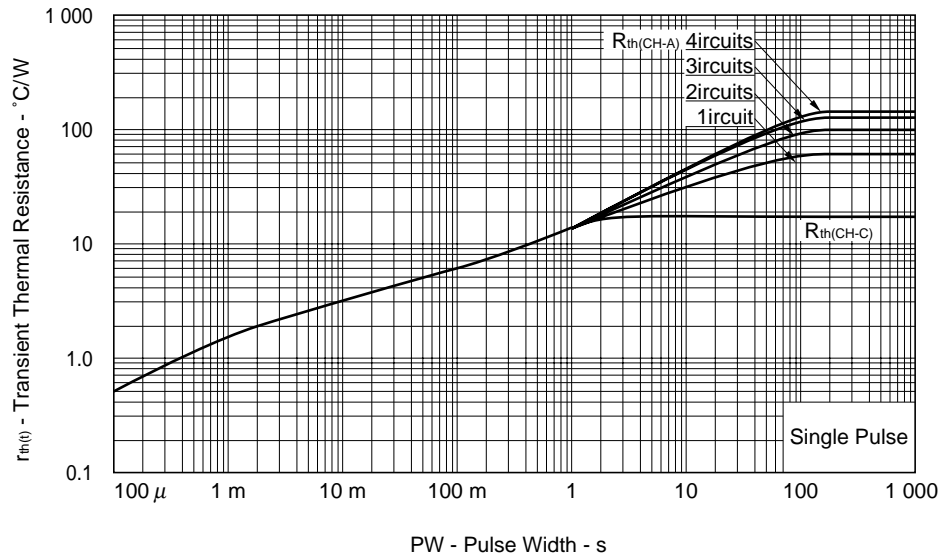
Test Circuit 3 Gate Charge



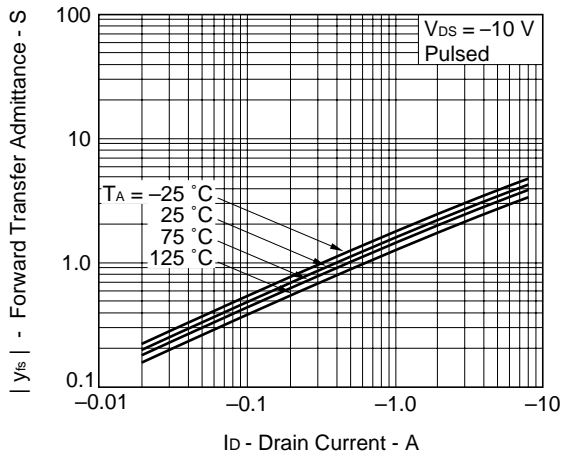
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



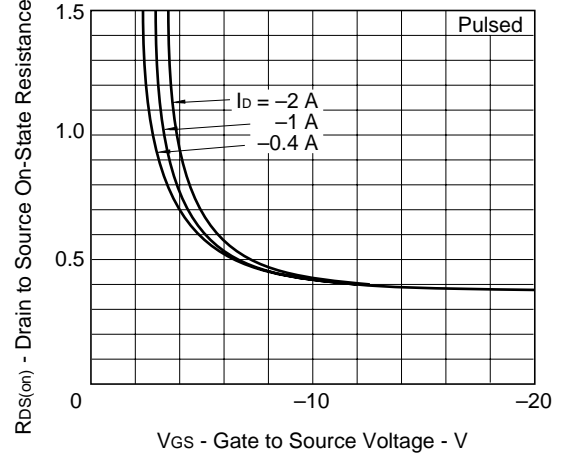
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



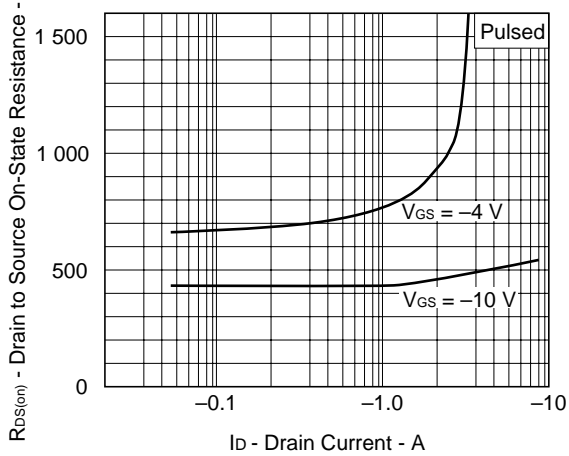
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



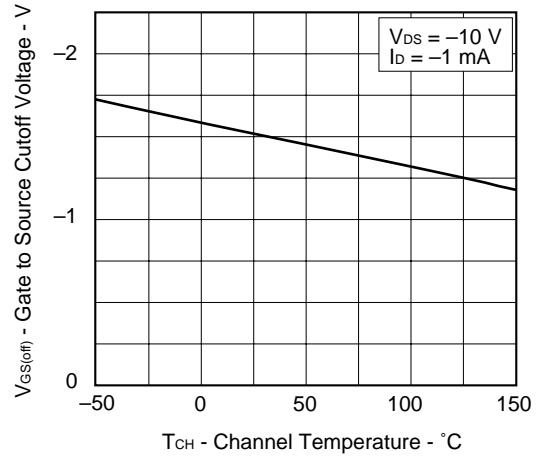
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

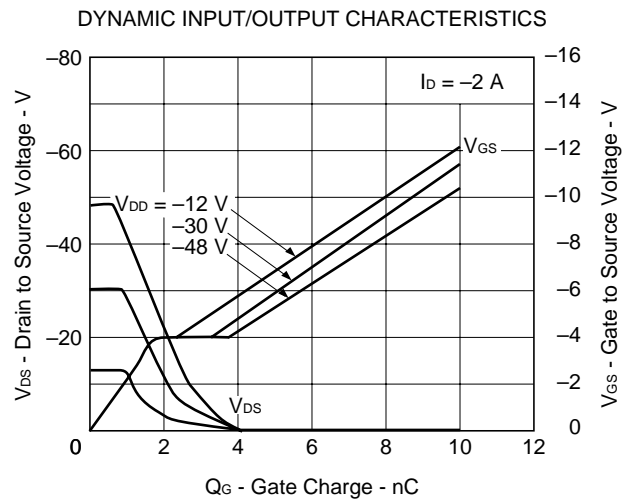
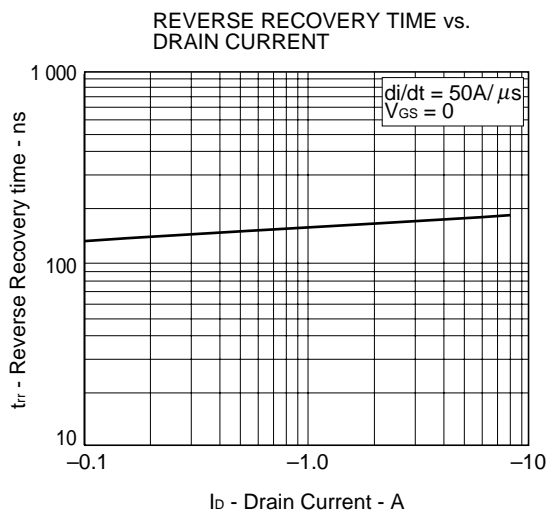
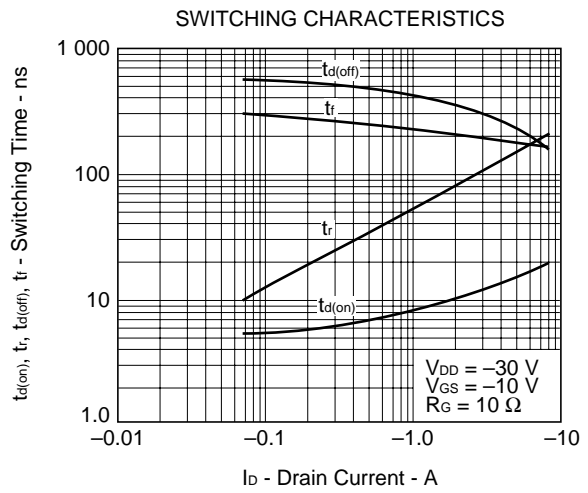
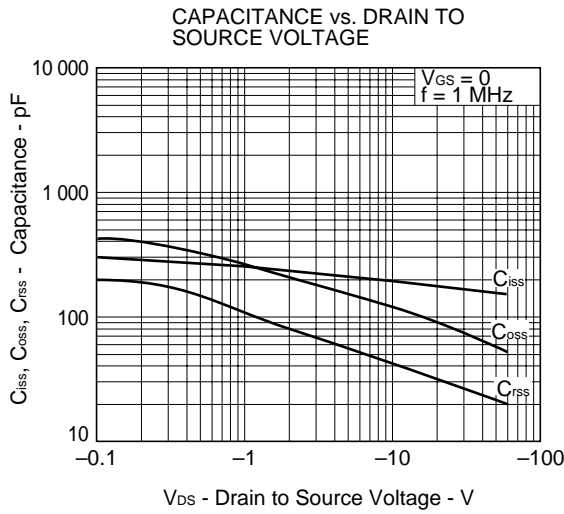
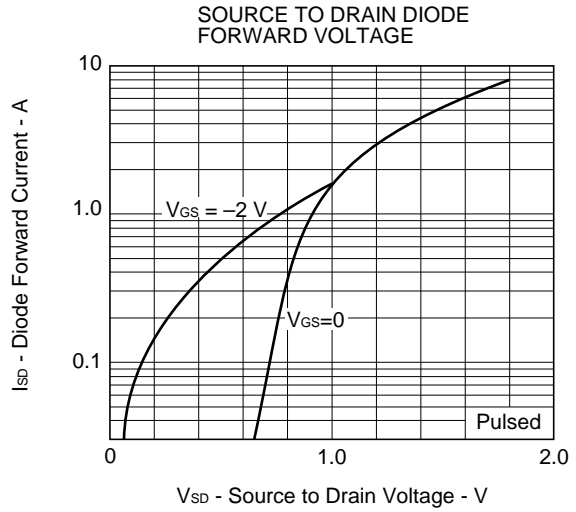
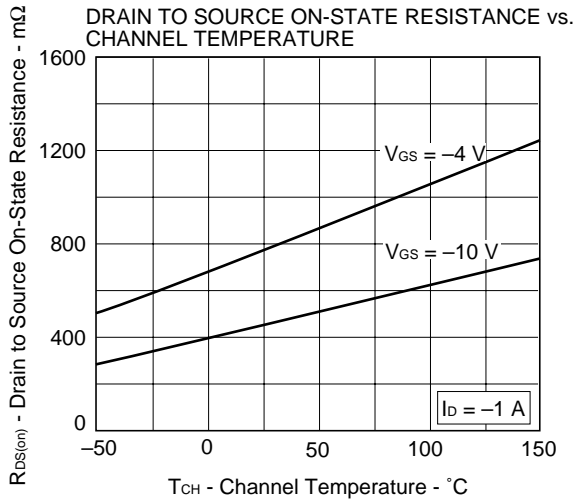


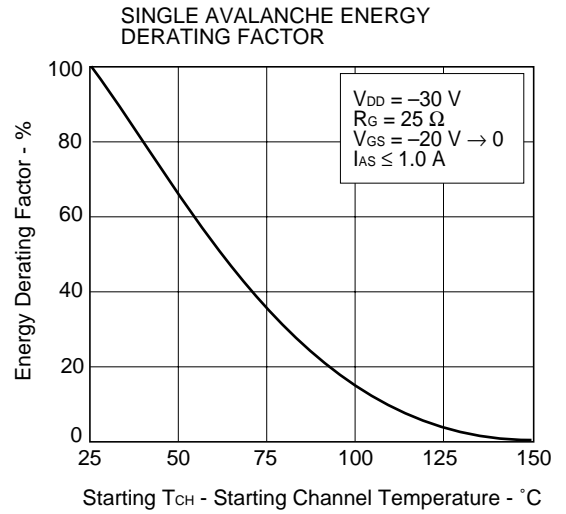
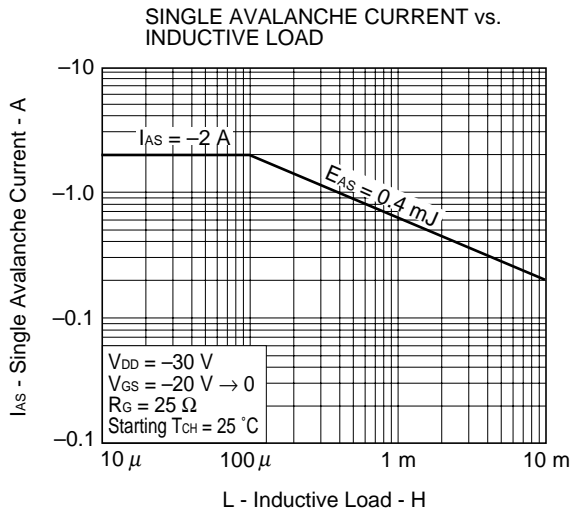
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







REFERENCE

Document Name	Document No.
NEC semiconductor for device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.