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P1 98.2

N-CHANNEL POWER MOS FET ARRAY  
SWITCHING TYPE

DESCRIPTION

The  $\mu$ PA1556A is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance  
 $I_{D(pulse)} = \pm 20$  A  
 $R_{DS(on)} = 0.20 \Omega$  TYP. ( $V_{GS} = 10$  V)  
 $R_{DS(on)} = 0.25 \Omega$  TYP. ( $V_{GS} = 4$  V)
- Low Capacitance  $C_{iss} = 700$  pF TYP.
- Gate Protector built in.
- 2.54 mm Pitch (0.1 inch)

ORDERING INFORMATION

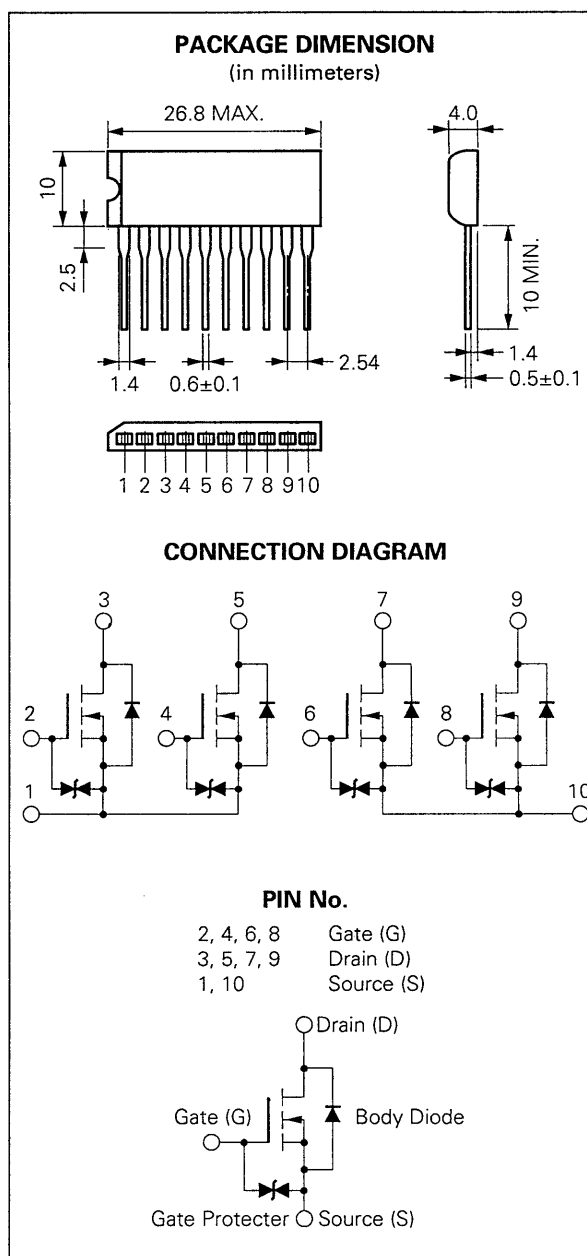
Part Number	Package	Quality Grade
$\mu$ PA1556AH	10 Pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ( $T_a = 25$  °C)

Drain to Source Voltage	$V_{DSS}$	100	V
Gate to Source Voltage (AC)	$V_{GSS}$	$\pm 20$	V
Gate to Source Voltage (DC)	$V_{GSS}$	+20, -10	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 5.0$	A/unit
Drain Current (pulse)	$I_{D(pulse)*}$	$\pm 20$	A/unit
Total Power Dissipation (4 circuits)			
< $T_c = 25$ °C>	$P_{T1}$	28	W
Total Power Dissipation (4 circuits)			
< $T_a = 25$ °C>	$P_{T2}$	3.5	W
Storage Temperature	$T_{stg}$	-55 to +150	°C
Junction Temperature	$T_j$	150	°C

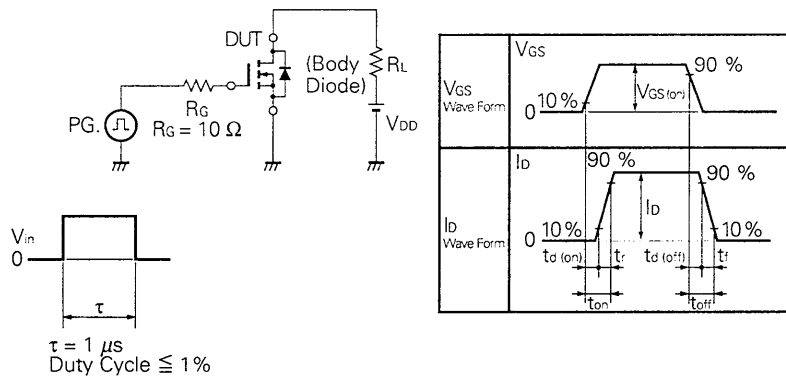
\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$



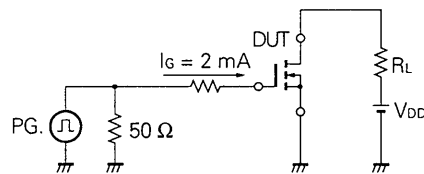
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	4.0			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3 A
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>		0.20	0.25	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A
Drain to Source On-state Resistance	R <sub>DS(on)2</sub>		0.25	0.33	Ω	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 3 A
Input Capacitance	C <sub>iss</sub>		700		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1.0 MHz
Output Capacitance	C <sub>oss</sub>		200		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		30		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		35		ns	I <sub>D</sub> = 3 A V <sub>GS</sub> = 10 V V <sub>CC</sub> = 50 V R <sub>L</sub> = 17 Ω, R <sub>in</sub> = 10 Ω See Fig. 1
Rise Time	t <sub>r</sub>		60		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		800		ns	
Fall Time	t <sub>f</sub>		200		ns	
Total Gate Charge	Q <sub>G</sub>		17		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 5 A V <sub>DD</sub> = 80 V See Fig. 2
Gate to Source Charge	Q <sub>GS</sub>		2.5		nC	
Gate to Drain Charge	Q <sub>GD</sub>		4		nC	
Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 5 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		120		ns	I <sub>F</sub> = 5 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		230		nC	

**Fig. 1 Switching Time Test Circuit**

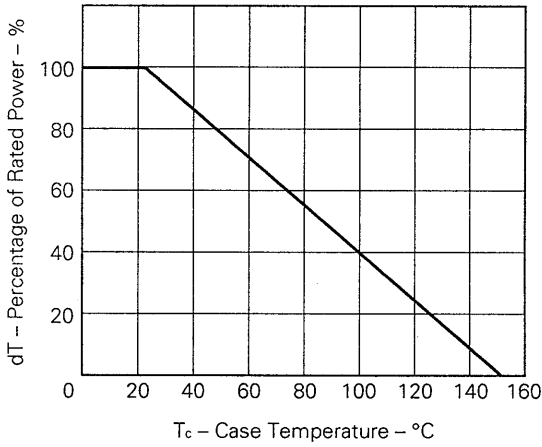


**Fig. 2 Gate Charge Test Circuit**

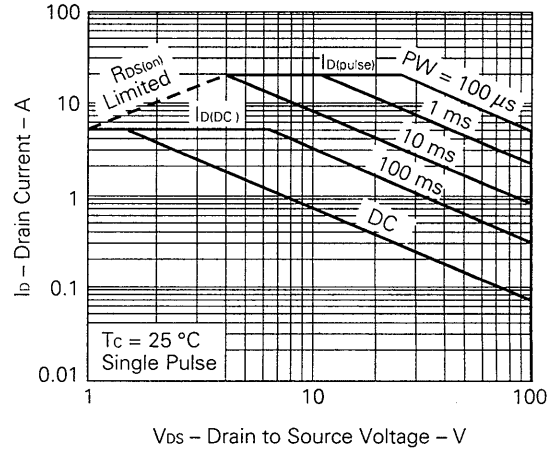


TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

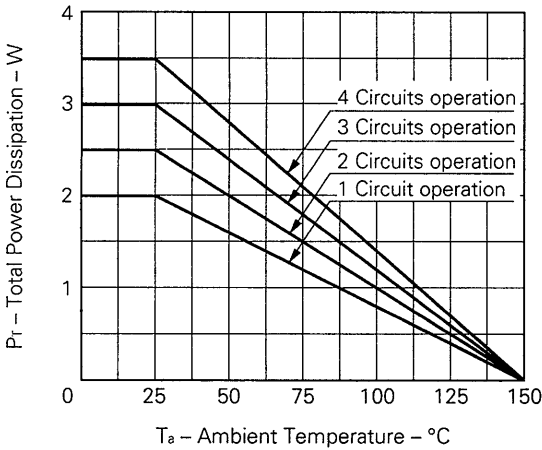
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



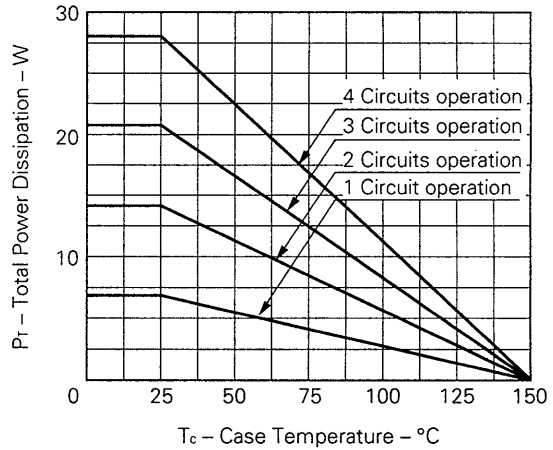
FORWARD BIAS SAFE OPERATING AREA



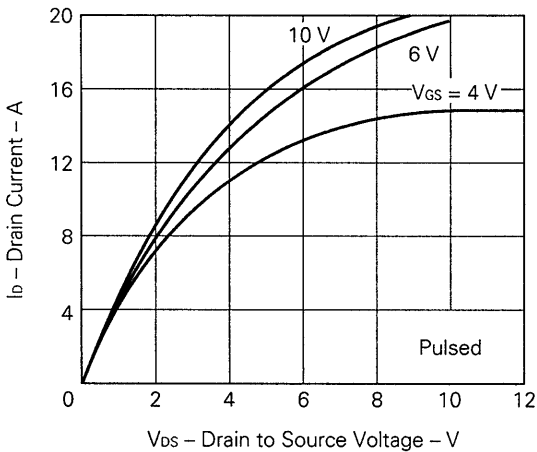
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



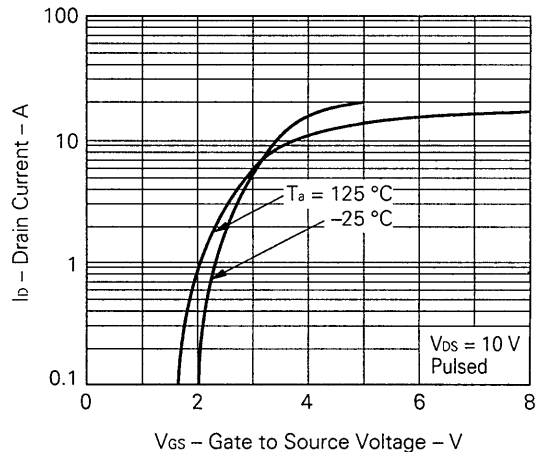
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



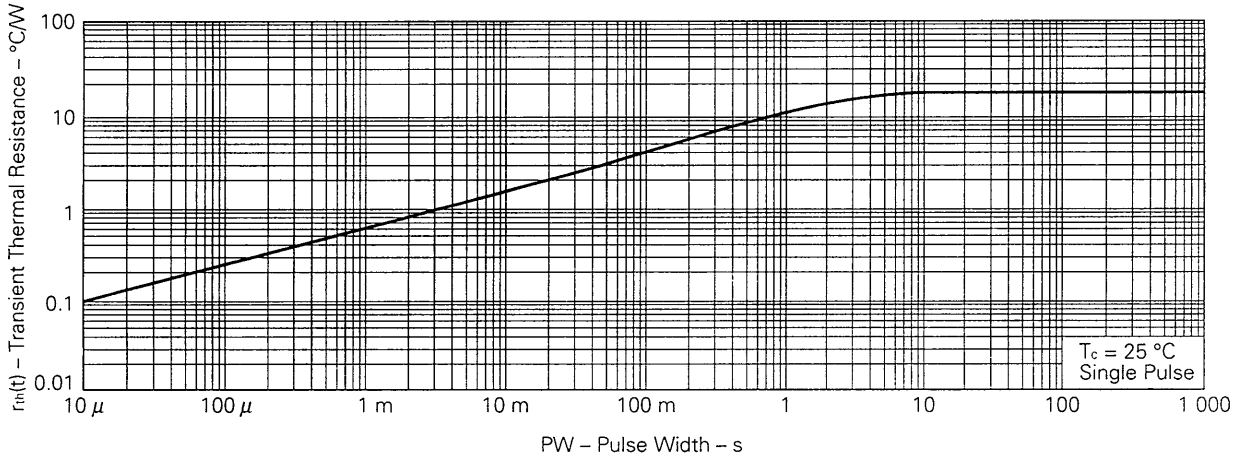
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



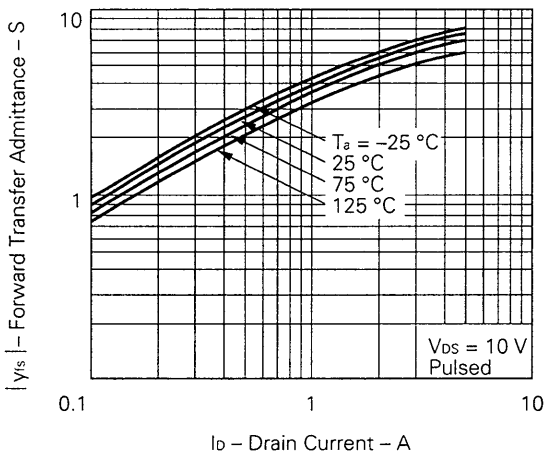
TRANSFER CHARACTERISTICS



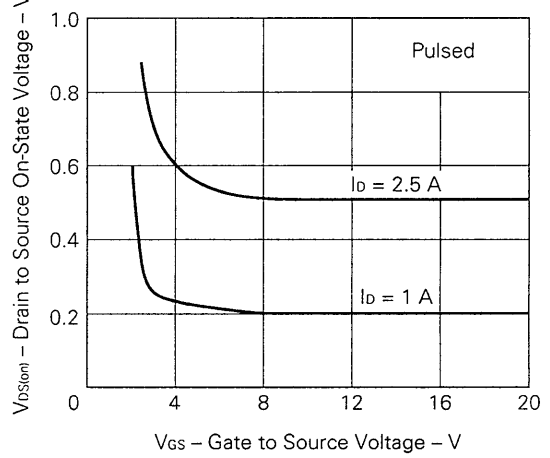
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



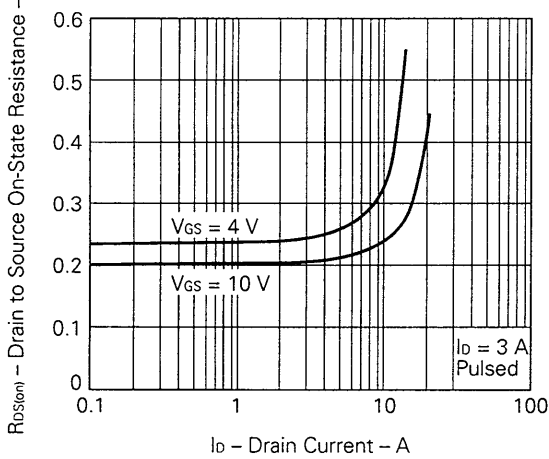
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



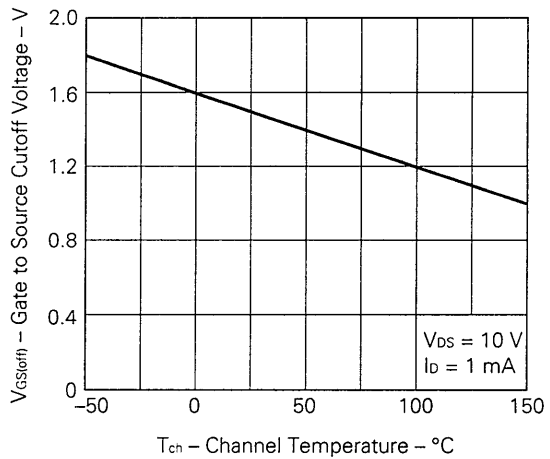
DRAIN TO SOURCE ON-STATE VOLTAGE vs. GATE TO SOURCE VOLTAGE

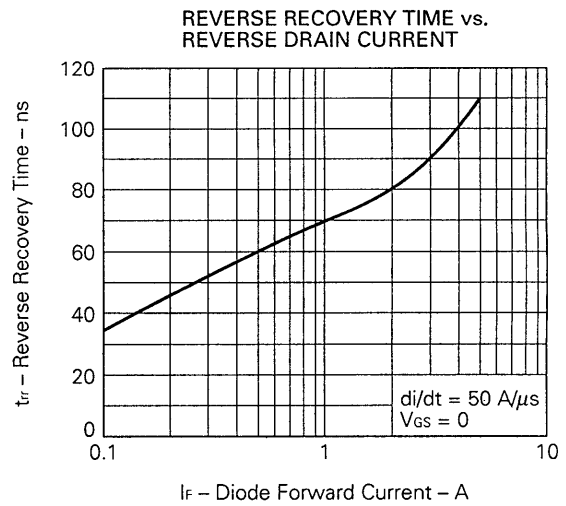
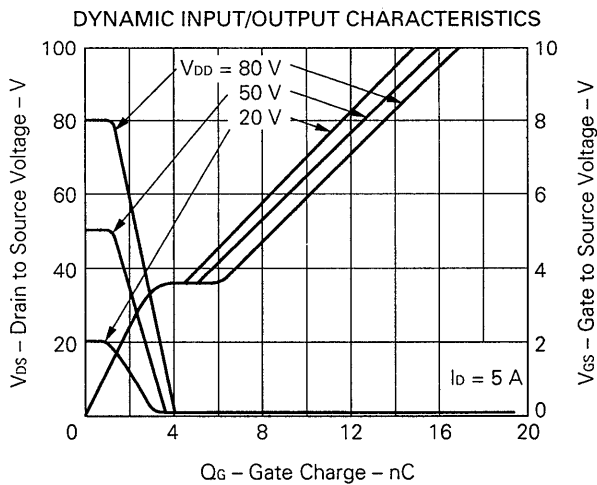
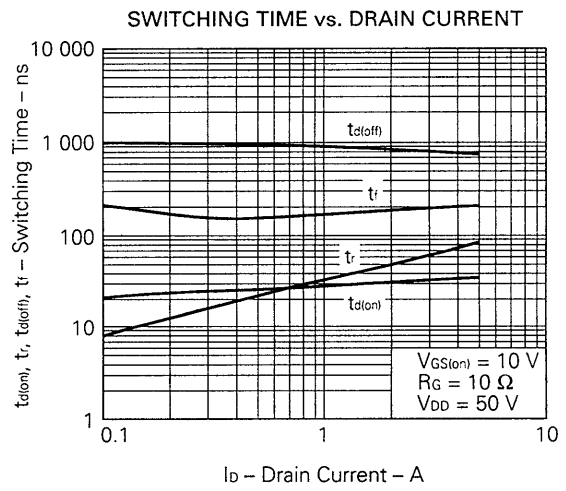
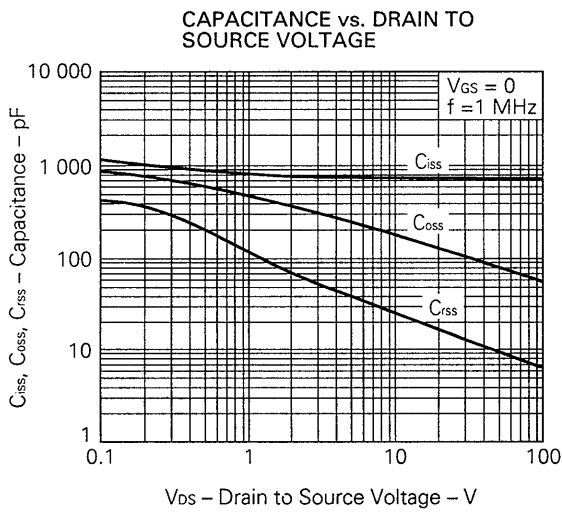
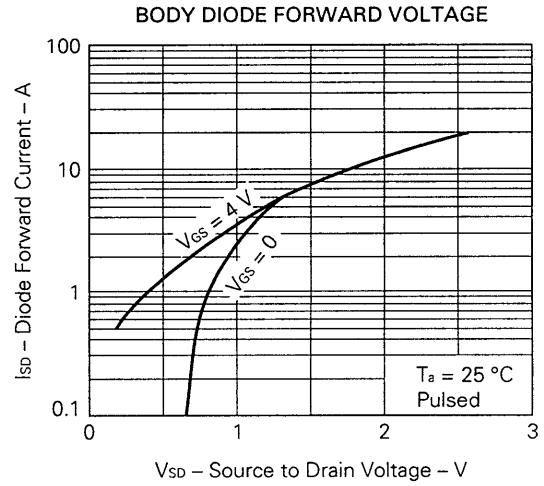
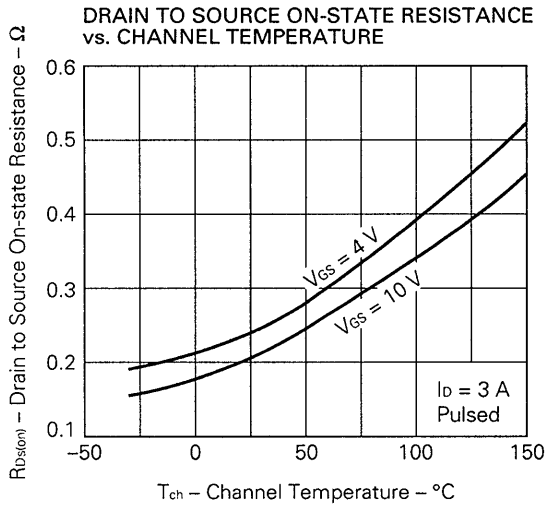


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





**Reference**

Document name	Document No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Appication circuit using Power MOS FET	TEA-1035

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