

mos field effect transistor $\mu PA505T$

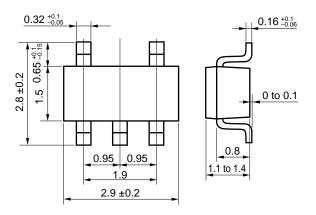
N-CHANNEL/P-CHANNEL MOS FET (5-PIN 2 CIRCUITS)

The μ PA505T is a mini-mold device provided with two MOS FET circuits. It achieves high-density mounting and saves mounting costs.

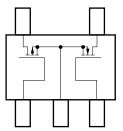
FEATURES

- Two source common MOS FET circuits in package the same size as SC-59
- Complementary MOS FETs are provided in one package.
- · Automatic mounting supported

PACKAGE DIMENSIONS (in millimeters)



PIN CONNECTION (Top View)



Marking: FA

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

PARAMETER	SYMBOL	RATINGS UN	
Drain to Source Voltage	Voss	50/–50	V
Gate to Source Voltage	Vgss	±20/∓16 V	
Drain Current (DC)	I _{D(DC)}	±100/∓100	mA
Drain Current (pulse)	ID(pulse)*	±200/∓200	mA
Total Power Dissipation	Рт	300 (TOTAL)	mW
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

^{*} PW ≤ 10 ms, Duty Cycle ≤ 50 %

Note The left and right values in the ratings column are correspond to N-ch and P-ch FETs, respectively.



ELECTRICAL CHARACTERISTICS (TA = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	IDSS	V _{DS} = 50/-50 V, V _{GS} = 0	_	-	1.0	μΑ
Gate Leakage Current	Igss	$V_{GS} = \pm 20/\mp 16 \text{ V}, V_{DS} = 0$	-	-	±1.0 ∓10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = 5.0/-5.0 \text{ V}, \text{ ID} = 1/-1 \ \mu\text{A}$	0.8	1.4	1.8	V
Forward Transfer Admittance	yfs	V _{DS} = 5.0/–5.0 V, I _D = 10/–10 mA	20 15	_	_	mS
Drain to Source On-State Resistance	RDS(on)1	Vss = 4/-4 V, I _D = 10/-10 mA	_	19 60	30 100	Ω
Drain to Source On-State Resistance	RDS(on)2	Vss = 10/-10 V, lb = 10/-10 mA	_	15 40	25 60	Ω
Input Capacitance	Ciss	V _{DS} = 5.0/-5.0 V V _{GS} = 0, f = 1.0 MHz	_	16 10	-	pF
Output Capacitance	Coss		_	12 4	-	pF
Reverse Transfer Capacitance	Crss		_	3 4	-	pF
Turn-On Delay Time	td(on)	V _{DD} = 5.0/-5.0 V, I _D = 10/-10 mA V _{GS(on)} = 5.0/-5.0 V	_	17 40	-	ns
Rise Time	tr	R _G = 10 Ω , R _L = 500 Ω	_	10 40	-	ns
Turn-Off Delay Time	td(off)		_	68 100	-	ns
Fall Time	t f		_	38 80	-	ns

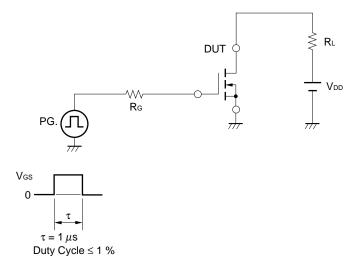
Marking: FA

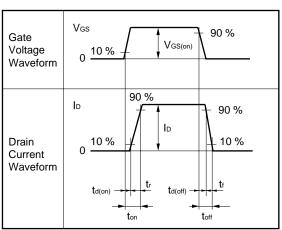
Note The left and right values in above table represent the N-ch and P-ch characteristics, respectively.



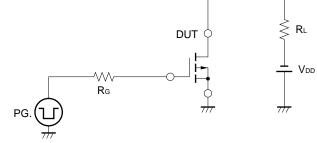
SWITCHING TIME MEASUREMENT CIRCUIT AND MEASUREMENT CONDITIONS (RESISTANCE LOADED)

N-ch part

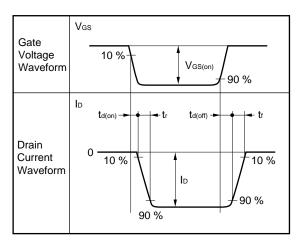




• P-ch part



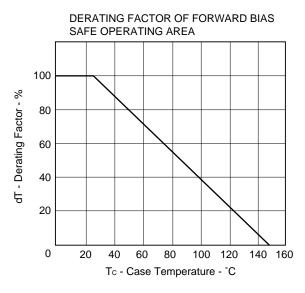




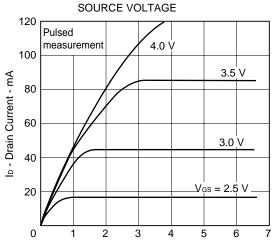


TYPICAL CHARACTERISTICS (TA = 25 °C)

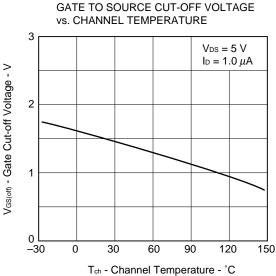
· N-ch part

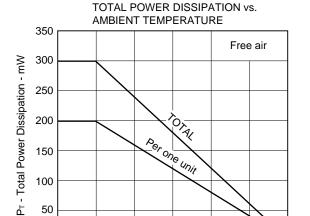


DRAIN CURRENT vs. DRAIN TO



V_{DS} - Drain to Source Voltage - V





TRANSFER CHARACTERISTICS

75

 T_{A} - Ambient Temperature - $^{\circ}\text{C}$

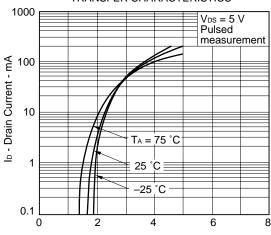
100

125

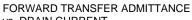
150

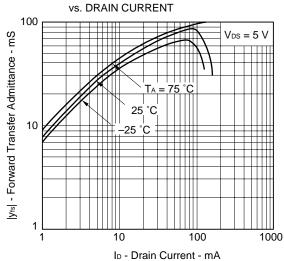
0

25

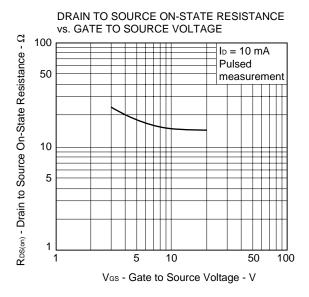


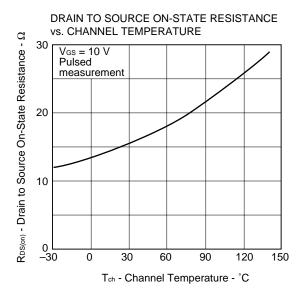
V_{GS} - Gate to Source Voltage - V

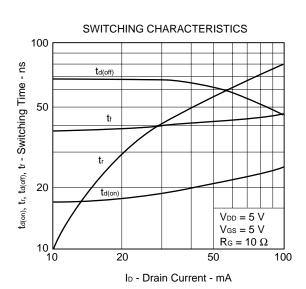


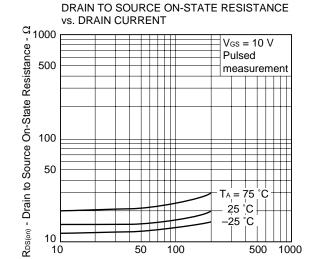


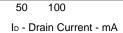


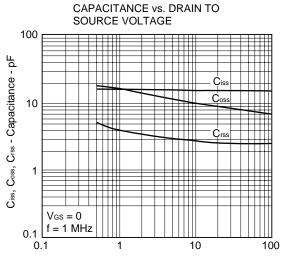




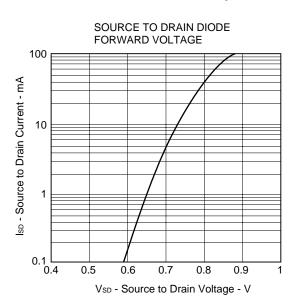






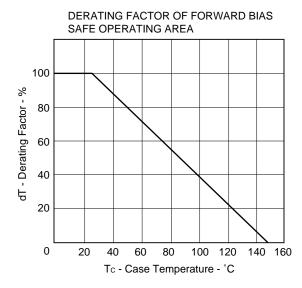


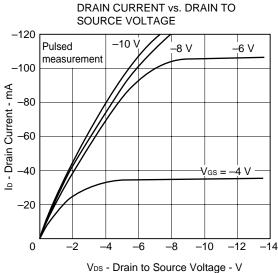
V_{DS} - Drain to Source Voltage - V

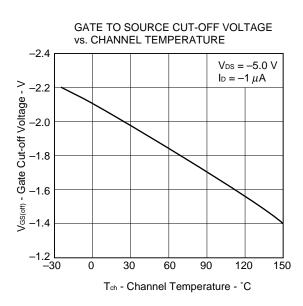


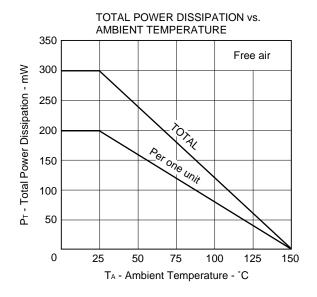


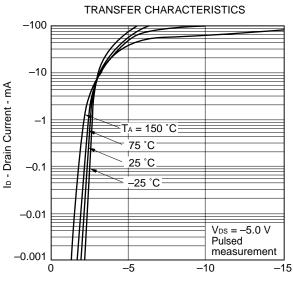
· P-ch part



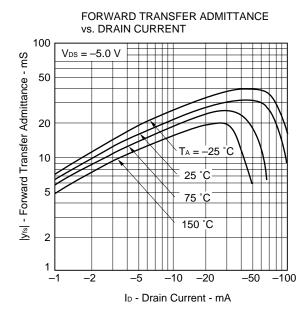




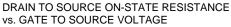


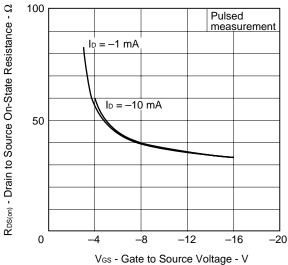


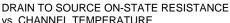
V_{GS} - Gate to Source Voltage - V

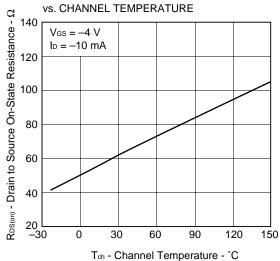




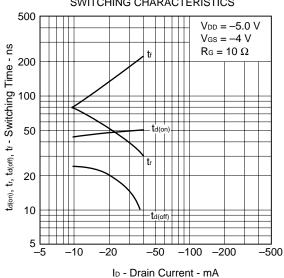




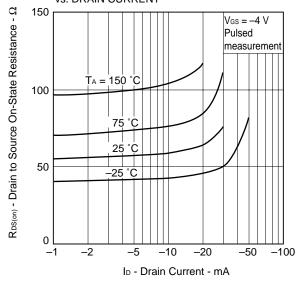




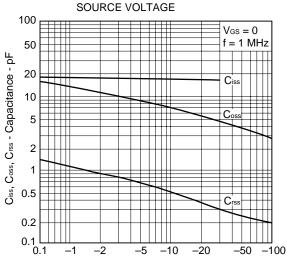
SWITCHING CHARACTERISTICS



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

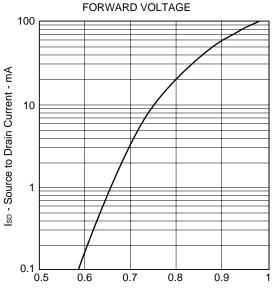


CAPACITANCE vs. DRAIN TO



V_{DS} - Drain to Source Voltage - V

SOURCE TO DRAIN DIODE



VsD - Source to Drain Voltage - V



REFERENCE

Document Name	Document No.	
NEC semiconductor device reliability/quality control system	TEI-1202	
Quality grade on NEC semiconductor devices	IEI-1209	
Semiconductor device mounting technology manual	C10535E	
Guide to quality assurance for semiconductor devices	MEI-1202	
Semiconductor selection guide	X10679E	



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Anti-radioactive design is not implemented in this product.