

## REFERENCE FREQUENCY 16.368 MHz, 2ND IF FREQUENCY 4.092 MHz RF/IF FREQUENCY DOWN-CONVERTER + PLL FREQUENCY SYNTHESIZER IC FOR GPS RECEIVER

### DESCRIPTION

The μPB1005K is a silicon monolithic integrated circuit for GPS receiver. This IC is designed as double conversion RF block integrated RF/IF down-converter + PLL frequency synthesizer on 1 chip.

The μPB1005K features 36-pin plastic QFN, fixed prescaler and supply voltage. The 36-pin plastic QFN package is suitable for high density surface mounting. The fixed division internal prescaler is needless to input serial counter data. Supply voltage is 3 V. Thus, the μPB1005K can make RF block fewer components and lower power consumption.

This IC is manufactured using NEC's 20 GHz fr NESAT™III silicon bipolar process. This process uses direct silicon nitride passivation film and gold electrodes. These materials can protect the chip surface from pollution and prevent corrosion/migration. Thus, this IC realizes excellent performance, uniformity and reliability.

### FEATURES

- Double conversion :  $f_{REFin} = 16.368 \text{ MHz}$ ,  $f_{2ndIFout} = 4.092 \text{ MHz}$
- Integrated RF block : RF/IF frequency down-converter + PLL frequency synthesizer
- High-density surface mountable : 36-pin plastic QFN (6.0 × 6.0 × 0.95 mm)
- Needless to input counter data : fixed division internal prescaler
  - VCO side division : ÷ 200 (÷ 25, ÷ 8 serial prescaler)
  - Reference division : ÷ 2
- Supply voltage :  $V_{CC} = 2.7 \text{ to } 3.3 \text{ V}$
- Low current consumption :  $I_{CC} = 45.0 \text{ mA TYP. @ } V_{CC} = 3.0 \text{ V}$
- Gain adjustable externally : Gain control voltage pin (control voltage up vs. gain down)

### APPLICATION

- Consumer use GPS receiver of reference frequency 16.368 MHz, 2nd IF frequency 4.092 MHz

### ORDERING INFORMATION

| Part Number | Package            | Supplying Form   |
|-------------|--------------------|--|
| μPB1005K-E1 | 36-pin plastic QFN | Embossed tape 12 mm wide.<br>Pin 1 is in pull-out direction.<br>Qty 2.5 kp/reel. |

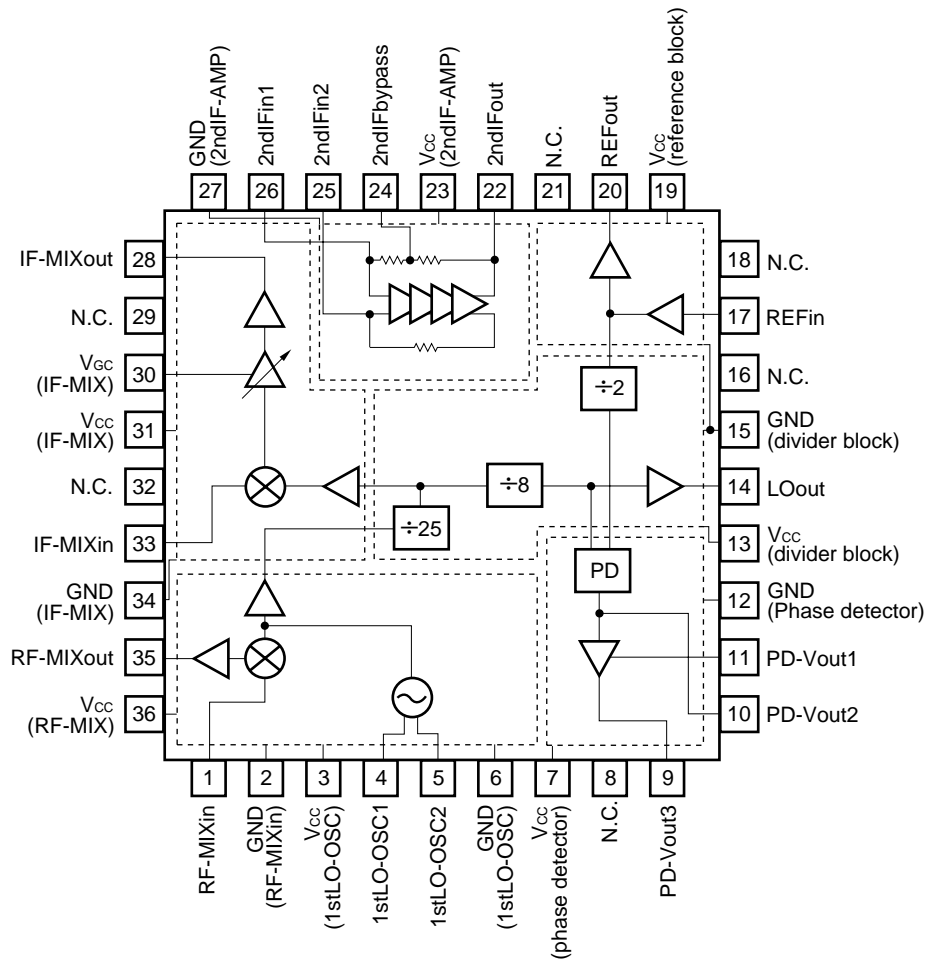
**Remark** To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: μPB1005K)

### Caution Electro-static sensitive device

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PIN CONNECTION AND INTERNAL BLOCK DIAGRAM



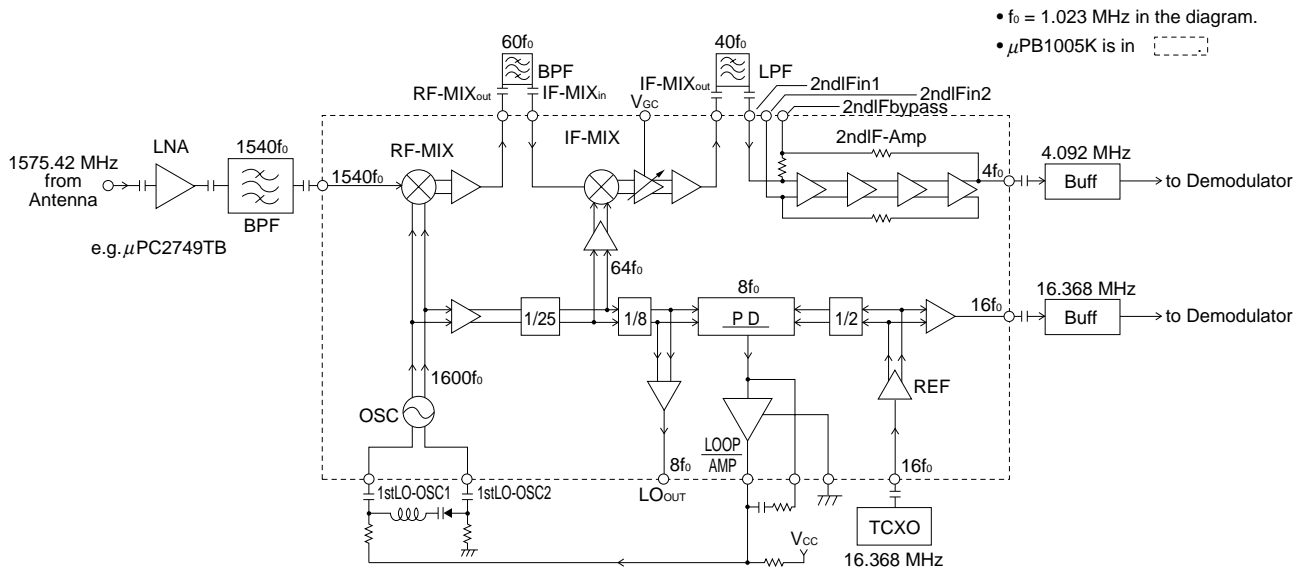
PRODUCT LINE-UP (T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.0 V)

| Type                                 | Part Number | Functions<br>(Frequency unit: MHz)   | V <sub>CC</sub><br>(V) | I <sub>CC</sub><br>(mA) | CG<br>(dB) | Package                       | Status       |
|--------------------------------------|-------------|--|------------------------|-------------------------|------------|-------------------------------|--------------|
| General Purpose Wideband Separate IC | μPC2756T    | RF down-converter with osc. Tr   | 2.7 to 3.3             | 6.0                     | 14         | 6-pin minimold                | Available    |
|                                      | μPC2756TB   |  |                        |                         |            | 6-pin super minimold          |              |
|                                      | μPC2753GR   | IF down-converter with gain control amplifier  | 2.7 to 3.3             | 6.5                     | 60 to 79   | 20-pin plastic SSOP (225 mil) |              |
| Clock Frequency Specific 1 chip IC   | μPB1003GS   | RF/IF down-converter + PLL synthesizer<br>REF = 18.414<br>1stIF = 28.644/2ndIF = 1.023 | 2.7 to 3.3             | 37.5                    | 72 to 92   | 30-pin plastic SSOP (300 mil) | Discontinued |
|                                      | μPB1004GS   | RF/IF down-converter + PLL synthesizer<br>REF = 16.368                                 | 2.7 to 3.3             | 37.5                    | 72 to 92   |                               |              |
|                                      | μPB1005GS   | RF/IF down-converter + PLL synthesizer<br>REF = 16.368                                 | 2.7 to 3.3             | 45.0                    | 72 to 92   | 36-pin plastic QFN            | Available    |
|                                      | μPB1005K    | 1stIF = 61.380/2ndIF = 4.092   |                        |                         |            |                               |              |

**Notice** Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.  
To know the associated products, please refer to their latest data sheets.

SYSTEM APPLICATION EXAMPLE

GPS receiver RF block diagram



**Caution** This diagram schematically shows only the μPB1005K's internal functions on the system.  
This diagram does not present the actual application circuits.

**ABSOLUTE MAXIMUM RATINGS**

| Parameter                     | Symbol           | Conditions  | Rating      | Unit |
|-------------------------------|------------------|---|-------------|------|
| Supply Voltage                | V <sub>CC</sub>  | T <sub>A</sub> = +25 °C   | 3.6         | V    |
| Total Circuit Current         | I <sub>CC</sub>  | T <sub>A</sub> = +25 °C   | 120         | mA   |
| Power Dissipation             | P <sub>D</sub>   | Mounted on double-sided copper clad<br>50 × 50 × 1.6 mm epoxy glass PWB (T <sub>A</sub> = +85 °C) | 430         | mW   |
| Operating Ambient Temperature | T <sub>A</sub>   |   | -40 to +85  | °C   |
| Storage Temperature           | T <sub>stg</sub> |   | -55 to +150 | °C   |

**RECOMMENDED OPERATING RANGE**

| Parameter                        | Symbol  | MIN.    | TYP.    | MAX.    | Unit |
|----------------------------------|---|---------|---------|---------|------|
| Supply Voltage                   | V <sub>CC</sub>                               | 2.7     | 3.0     | 3.3     | V    |
| Operating Ambient Temperature    | T <sub>A</sub>                                | -40     | +25     | +85     | °C   |
| RF Input Frequency               | f <sub>RFIn</sub>                             | —       | 1575.42 | —       | MHz  |
| 1st LO Oscillating Frequency     | f <sub>1stLOin</sub>                          | 1616.80 | 1636.80 | 1656.80 | MHz  |
| 1st IF Input Frequency           | f <sub>1stIFin</sub>                          | —       | 61.38   | —       | MHz  |
| 2nd LO Input Frequency           | f <sub>2ndLOin</sub>                          | —       | 65.472  | —       | MHz  |
| 2nd IF Input/output Frequency    | f <sub>2ndIFin</sub><br>f <sub>2ndIFout</sub> | —       | 4.092   | —       | MHz  |
| Reference Input/output Frequency | f <sub>REFin</sub><br>f <sub>REFout</sub>     | —       | 16.368  | —       | MHz  |
| LO Output Frequency              | f <sub>LOout</sub>                            | —       | 8.184   | —       | MHz  |

**ELECTRICAL CHARACTERISTICS (Unless otherwise specified  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.0\text{ V}$ )**

| Parameter  | Symbol                | Conditions  | MIN.  | TYP.  | MAX. | Unit              |
|--|-----------------------|---|-------|-------|------|-------------------|
| Total Circuit Current  | I <sub>ccTotal</sub>  | I <sub>cc1</sub> + I <sub>cc2</sub> + I <sub>cc3</sub> + I <sub>cc4</sub> | 32.0  | 45.0  | 60.0 | mA                |
| RF Down-converter Block (f <sub>RFIn</sub> = 1575.42 MHz, f <sub>1stLOIn</sub> = 1636.80 MHz, P <sub>LOIn</sub> = -10 dBm, Z <sub>S</sub> = Z <sub>L</sub> = 50 Ω) |                       |   |       |       |      |                   |
| Circuit Current 1  | I <sub>cc1</sub>      | No Signals  | 6.0   | 10.0  | 14.0 | mA                |
| RF Conversion Gain   | CG <sub>RF</sub>      | P <sub>RFIn</sub> = -40 dBm   | 12.5  | 15.5  | 18.5 | dB                |
| RF-SSB Noise Figure  | NF <sub>RF</sub>      | P <sub>RFIn</sub> = -40 dBm   | 7.0   | 10.0  | 13.0 | dB                |
| Maximum IF Output  | P <sub>O(sat)RF</sub> | P <sub>RFIn</sub> = -10 dBm   | -5.5  | -2.5  | +0.5 | dBm               |
| IF Down-converter Block (f <sub>1stIFIn</sub> = 61.38 MHz, f <sub>2ndLOIn</sub> = 65.472 MHz, Z <sub>S</sub> = 50 Ω, Z <sub>L</sub> = 2 kΩ)                        |                       |   |       |       |      |                   |
| Circuit Current 2  | I <sub>cc2</sub>      | No Signals  | 3.4   | 5.3   | 7.2  | mA                |
| IF Conversion Voltage Gain   | CG <sub>(GV)IF</sub>  | at Maximum Gain, P <sub>1stIFIn</sub> = -50 dBm                           | 38    | 41    | 44   | dB                |
| IF-SSB Noise Figure  | NF <sub>IF</sub>      | at Maximum Gain, P <sub>1stIFIn</sub> = -50 dBm                           | 8.5   | 11.5  | 14.5 | dB                |
| Maximum 2ndIF Output   | P <sub>O(sat)IF</sub> | at Maximum Gain, P <sub>1stIFIn</sub> = -20 dBm                           | -9.5  | -6.5  | -3.5 | dBm               |
| Gain Control Voltage   | V <sub>GC</sub>       | Voltage at Maximum Gain CG <sub>IF</sub>                                  | —     | —     | 1.0  | V                 |
| Gain Control Range   | D <sub>GC</sub>       | P <sub>1stIFIn</sub> = -50 dBm  | 20    | —     | —    | dB                |
| 2nd IF Amplifier (f <sub>2ndIF</sub> = 4.092 MHz, Z <sub>S</sub> = 50 Ω, Z <sub>L</sub> = 2 kΩ)  |                       |   |       |       |      |                   |
| Circuit Current 3  | I <sub>cc3</sub>      | No Signals  | 1.55  | 2.40  | 3.25 | mA                |
| Voltage Gain   | G <sub>V</sub>        | P <sub>2ndIFIn</sub> = -60 dBm  | 37    | 40    | 43   | dB                |
| Output Power   | P <sub>2ndIFout</sub> | P <sub>2ndIFIn</sub> = -30 dBm  | -14.5 | -11.5 | -8.5 | dBm               |
| PLL Synthesizer Block  |                       |   |       |       |      |                   |
| Circuit Current 4  | I <sub>cc4</sub>      | PLL All Block Operating   | 18.5  | 28.5  | 38.5 | mA                |
| Phase Comparing Frequency  | f <sub>PD</sub>       | PLL Loop  | 8.0   | 8.184 | 8.4  | MHz               |
| Reference Input Minimum Level  | V <sub>REFIn</sub>    | Z <sub>L</sub> = 10 kΩ//20 pF <sup>Note</sup>                             | 200   | —     | —    | mV <sub>P-P</sub> |
| Loop Filter Output Level (H)   | V <sub>LP(H)</sub>    |   | 2.8   | —     | —    | V                 |
| Loop Filter Output Level (L)   | V <sub>LP(L)</sub>    |   | —     | —     | 0.4  | V                 |
| Reference Output Swing   | V <sub>REFout</sub>   | Z <sub>L</sub> = 10 kΩ//2 pF <sup>Note</sup>                              | 1.0   | —     | —    | V <sub>P-P</sub>  |

**Note** Impedance of measurement equipment

**STANDARD CHARACTERISTICS (Unless otherwise specified  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.0\text{ V}$ )**

| Parameter  | Symbol              | Conditions   | Reference | Unit   |
|--|---------------------|--|-----------|--------|
| RF Down-converter Block ( $P_{1stLOin} = -10\text{ dBm}$ , $Z_s = Z_L = 50\ \Omega$ )        |                     |  |           |        |
| LO Leakage to IF Pin   | LO <sub>if</sub>    | $f_{1stLOin} = 1\ 636.80\text{ MHz}$   | -30       | dBm    |
| LO Leakage to RF Pin   | LO <sub>rf</sub>    | $f_{1stLOin} = 1\ 636.80\text{ MHz}$   | -30       | dBm    |
| Input 3rd Order Intercept Point  | IIP <sub>3RF</sub>  | $f_{RFin1} = 1\ 600\text{ MHz}$ , $f_{RFin2} = 1605\text{ MHz}$<br>$f_{1stLOin} = 1\ 660\text{ MHz}$       | -13       | dBm    |
| IF Down-converter Block (1st LO oscillating, $Z_s = 50\ \Omega$ , $Z_L = 2\text{ k}\Omega$ ) |                     |  |           |        |
| LO Leakage to 2nd IF   | LO <sub>2ndif</sub> | $f_{2ndLOin} = 65.472\text{ MHz}$  | -20       | dBm    |
| LO Leakage to 1st IF   | LO <sub>1stif</sub> | $f_{2ndLOin} = 65.472\text{ MHz}$  | -40       | dBm    |
| Input 3rd Order Intercept Point  | IIP <sub>3IF</sub>  | $f_{1stIFin1} = 61.38\text{ MHz}$ , $f_{1stIFin2} = 61.48\text{ MHz}$<br>$f_{2ndLOin} = 65.472\text{ MHz}$ | -34       | dBm    |
| VCO Block  |                     |  |           |        |
| Phase Noise  | C/N                 | PLL Loop, $\Delta 1\text{kHz}$ of VCO wave   | -78       | dBc/Hz |

PIN EXPLANATION

| Pin No. | Pin Name             | Applied Voltage (V)   | Pin Voltage (V)                            | Function and Application   | Internal Equivalent Circuit |
|---------|----------------------|-----------------------|--|--|-----------------------------|
| 35      | RX-MIXout            | —                     | 1.68                                       | Output pin of RF mixer. 1st IF filter must be inserted between pin 33 & 35.  |                             |
| 36      | Vcc (RF-MIX)         | 2.7 to 3.3            | —  | Supply voltage pin of RF mixer block. This pin must be decoupled with capacitor (example: 1 000 pF).   |                             |
| 1       | RF-MIXin             | —                     | 1.20                                       | Input pin of RF mixer. 1 575.42 MHz band pass filter can be inserted between pin 1 and external LNA.   |                             |
| 2       | GND (RF-MIX)         | 0                     | —  | Ground pin RF mixer.   |                             |
| 3       | Vcc (1stLO-OSC)      | 2.7 to 3.3            | —  | Supply voltage pin of differential amplifier for 1st LO oscillator circuit.  |                             |
| 4       | 1stLO-OSC1           | —                     | 1.88                                       | Pin 4 & 5 are each base pin of differential amplifier for 1st LO oscillator. These pins should be equipped with LC and varactor to oscillate on 1 636.80 MHz as VCO.   |                             |
| 5       | 1stLO-OSC2           | —                     | 1.88                                       |  |                             |
| 6       | GND (1stLO-OSC)      | 0                     | —  | Ground pin of differential amplifier for 1st LO oscillator circuit.  |                             |
| 7       | Vcc (phase detector) | 2.7 to 3.3            | —  | Supply voltage pin of phase detector and active loop filter.   |                             |
| 8       | N.C.                 | —                     | —  | Non connection   |                             |
| 9       | PD-Vout3             | Pull-up with resistor | —  | Pins of active loop filter for tuning voltage output. The active transistors configured with darlington pair are built on chip. Pin 11 should be pulled down with external resistor. Pin 9 to 10 should be equipped with external RC in order to adjust dumping factor and cutoff frequency. This tuning voltage output must be connected to varactor diode of 1st LO-OSC. |                             |
| 10      | PD-Vout2             | —                     | Output in accordance with phase difference |  |                             |
| 11      | PD-Vout1             | Pull-up with resistor | —  |  |                             |
| 12      | GND (phase detector) | 0                     | —  | Ground pin of phase detector + active loop filter.   |                             |

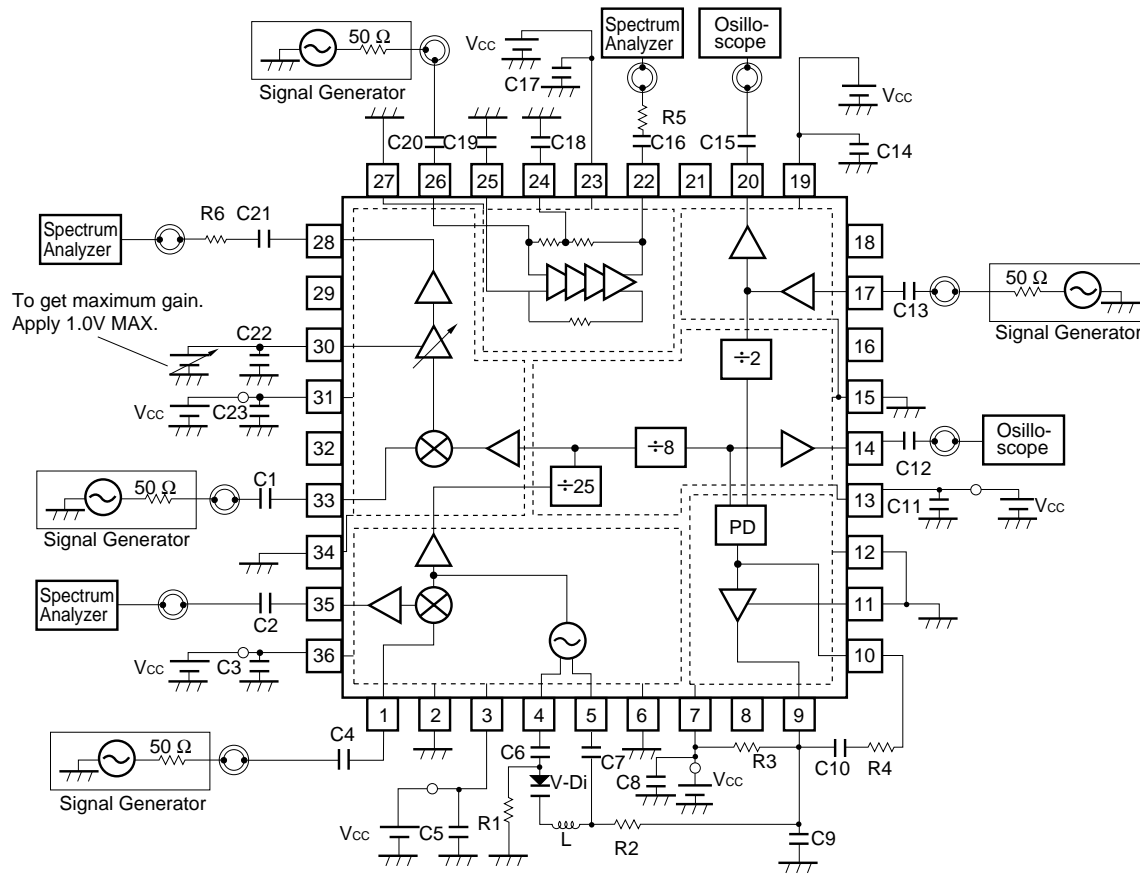
| Pin No. | Pin Name                             | Applied Voltage (V) | Pin Voltage (V) | Function and Application   | Internal Equivalent Circuit |
|---------|--------------------------------------|---------------------|-----------------|--|-----------------------------|
| 13      | V <sub>cc</sub><br>(divider block)   | 2.7 to 3.3          | —               | Supply voltage pin of prescalers.  |                             |
| 14      | LOout                                | —                   | 2.08            | Monitor pin of comparison frequency at phase detector.   |                             |
| 15      | GND<br>(divider block)               | 0                   | —               | Ground pin of prescalers + LOout amplifier   |                             |
| 16      | N.C.                                 | —                   | —               | Non connection   | —                           |
| 17      | REFin                                | —                   | 1.96            | Input pin of reference frequency. This pin should be equipped with external 16.368 MHz oscillator (example: TCXO).   |                             |
| 18      | N.C.                                 | —                   | —               | Non connection   |                             |
| 19      | V <sub>cc</sub><br>(reference block) | 2.7 to 3.3          | —               | Supply voltage pin of input/output amplifiers in reference block.  |                             |
| 20      | REFout                               | —                   | 1.65            | Output pin of reference frequency. The frequency from pin 17 can be took out as 1 V <sub>P-P</sub> swing.  |                             |
| 21      | N.C.                                 | —                   | —               | Non connection   | —                           |
| 22      | 2ndIFout                             | —                   | 1.56            | Output pin of 2nd IF amplifier. This pin output 4.092 MHz clipped sinewave. This pin should be equipped with external inverter to adjust level to next stage on user's system. |                             |
| 23      | V <sub>cc</sub><br>(2ndIF-AMP)       | 2.7 to 3.3          | —               | Supply voltage pin of 2nd IF amplifier.  |                             |
| 24      | 2ndIF bypass                         | —                   | 2.30            | Bypass pin of 2nd IF amplifier input 1. This pin should be grounded through capacitor.   |                             |
| 25      | 2ndIFin2                             | —                   | 2.35            | Pin of 2nd IF amplifier input 2. This pin should be grounded through capacitor.  |                             |
| 26      | 2ndIFin1                             | —                   | 2.35            | Pin of 2nd IF amplifier input 1. 2nd IF filter can be inserted between pin 26 & 28.  |                             |
| 27      | GND<br>(2ndIF-AMP)                   | 0                   | —               | Ground pin of 2nd IF amplifier.  |                             |



| Pin No. | Pin Name                 | Applied Voltage (V) | Pin Voltage (V) | Function and Application   | Internal Equivalent Circuit |
|---------|--------------------------|---------------------|-----------------|--|-----------------------------|
| 28      | IF-MIXout                | —                   | 1.15            | Output pin from IF mixer. IF mixer output signal goes through gain control amplifier before this emitter follower output port. |                             |
| 29      | N.C.                     | —                   | —               | Non connection   |                             |
| 30      | V <sub>GC</sub> (IF-MIX) | 0 to 3.3            | —               | Gain control voltage pin of IF mixer output amplifier. This voltage performs forward control (V <sub>GC</sub> up → Gain down). |                             |
| 31      | V <sub>CC</sub> (IF-MIX) | 2.7 to 3.3          | —               | Supply voltage pin of IF mixer, gain control amplifier and emitter follower transistor.  |                             |
| 32      | N.C.                     | —                   | —               | Non connection   |                             |
| 33      | IF-MIXin                 | —                   | 2.00            | Input pin of IF mixer.   |                             |
| 34      | GND (IF-MIX)             | 0                   | —               | Ground pin of IF mixer.  |                             |

**Caution** Ground pattern on the board must be formed as wide as possible to minimize ground impedance.

TEST CIRCUIT



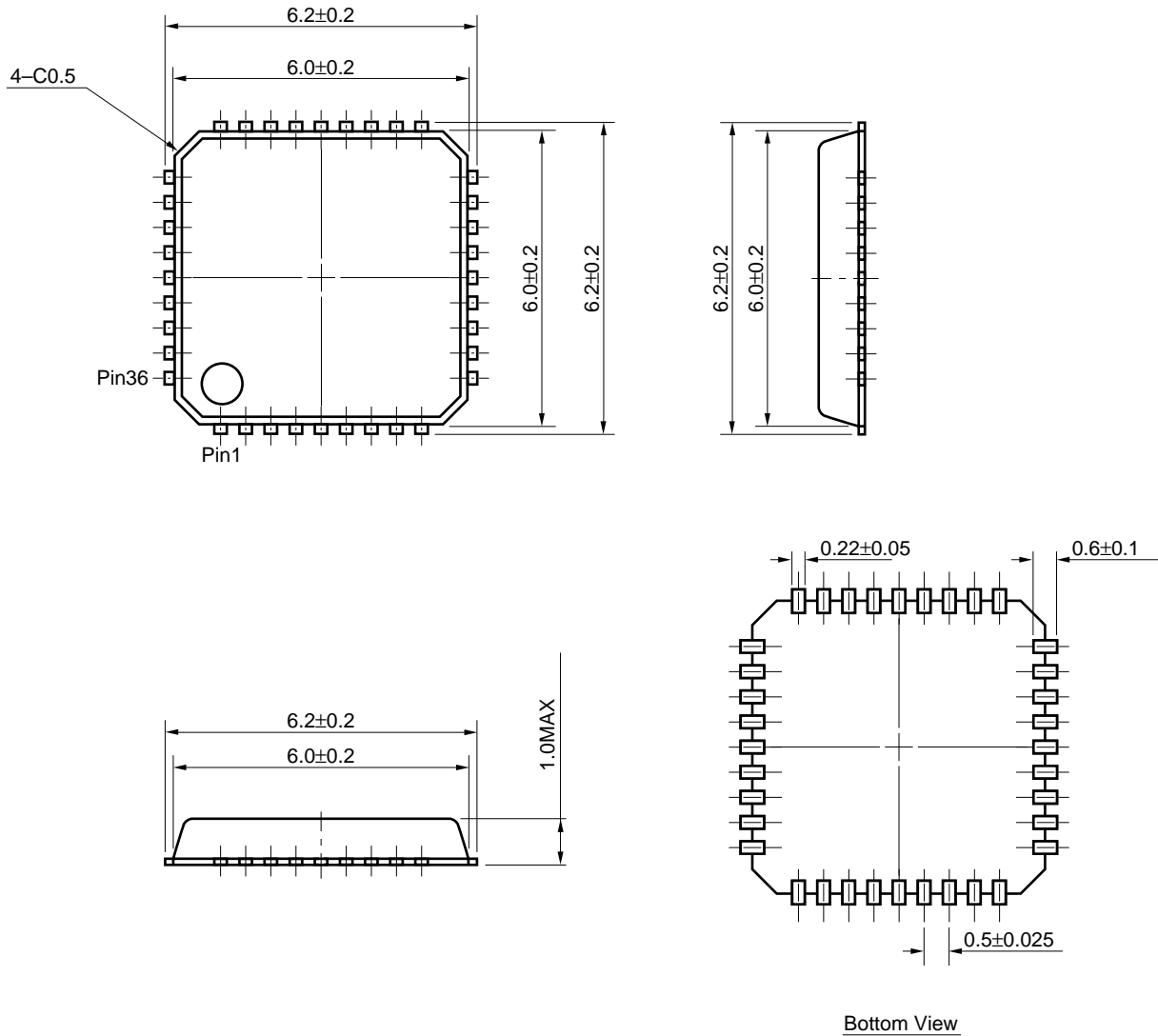
Spectrum Analyzer : measure frequency  
 Oscilloscope : measure output voltage swing

Component List

| Form           | Symbol                                  | Value      |
|----------------|---|------------|
| Chip capacitor | C1 to C5, C8, C11 to C15, C17, C18, C22 | 1 000 pF   |
|                | C6, C7                                  | 24 pF (UJ) |
|                | C9                                      | 1800 pF    |
|                | C10                                     | 33 nF      |
|                | C19                                     | 10 000 pF  |
|                | C23                                     | 1 μF       |
|                | C16, C20                                | 0.1 μF     |
|                | C21                                     | 0.01 μF    |
| Chip resistor  | R1, R2                                  | 4.7 kΩ     |
|                | R3                                      | 6.2 kΩ     |
|                | R4                                      | 1.2 kΩ     |
|                | R5, R6                                  | 1.95 kΩ    |
| Varactor Diode | V-Di                                    | 1SV285     |
| Chip Inductor  | L                                       | 3.9 nH     |

PACKAGE DIMENSIONS

36 PIN PLASTIC QFN (UNIT: mm)



**NOTE ON CORRECT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent abnormal oscillation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (example: 1 000 pF) to the V<sub>CC</sub> pin.
- (5) Frequency signal input/output pins must be each coupled with external capacitor for DC cut.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

| Soldering Method | Soldering Conditions   | Recommended Condition Symbol |
|------------------|--|------------------------------|
| Infrared Reflow  | Package peak temperature: 235 °C or below<br>Time: 30 seconds or less (at 210 °C)<br>Count: 2, Exposure limit <sup>Note</sup> : None | IR35-00-2                    |
| Partial Heating  | Pin temperature: 300 °C<br>Time: 3 seconds or less (per side of device)<br>Exposure limit <sup>Note</sup> : None                     | -                            |

**Note** After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

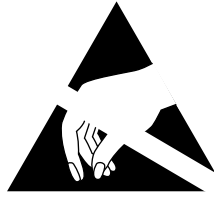
**Caution** Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

[MEMO]

[MEMO]

[MEMO]



## ATTENTION

OBSERVE PRECAUTIONS  
FOR HANDLING  
ELECTROSTATIC  
SENSITIVE  
DEVICES

**NESAT (NEC Silicon Advanced Technology) is a trademark of NEC Corporation.**

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
  - No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
  - NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
  - Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
  - While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
  - NEC devices are classified into the following three quality grades:  
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
    - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
    - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
    - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
- The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.