NEC

BiCMOS INTEGRATED CIRCUIT

μPC1935

DC-DC CONVERTER CONTROL IC

DESCRIPTION

The μPC1935 is a low-voltage input DC-DC converter control IC that can configure a three-output (step-up × 2, inverted output × 1) DC-DC converter at an input voltage of 3, 3.3, or 5 V.

Because of its wide operating voltage range, this IC can also be used to control DC-DC converters using an AC adapter for input.

FEATURES

- Low supply voltage: 2.5 V (MIN.)
- Operating voltage range: 2.5 to 20 V (breakdown voltage: 30 V)
- Can control three output channels.
- Timer latch circuit for short-circuit protection.
- Ceramic capacitor with low capacitance (0.1 μF) can be used for short-circuit protection.
- Dead times of channels 2 (step-up) and 3 (inverted output) can be set from external resistors. Dead time of channel 1 (step-up) is internally fixed to 85 %.
- Soft start of each channel can be set independently.
- Each channel can be turned ON/OFF independently.

ORDERING INFORMATION

Part Number	Package
μPC1935GR	16-pin plastic TSSOP (5.72 mm (225))

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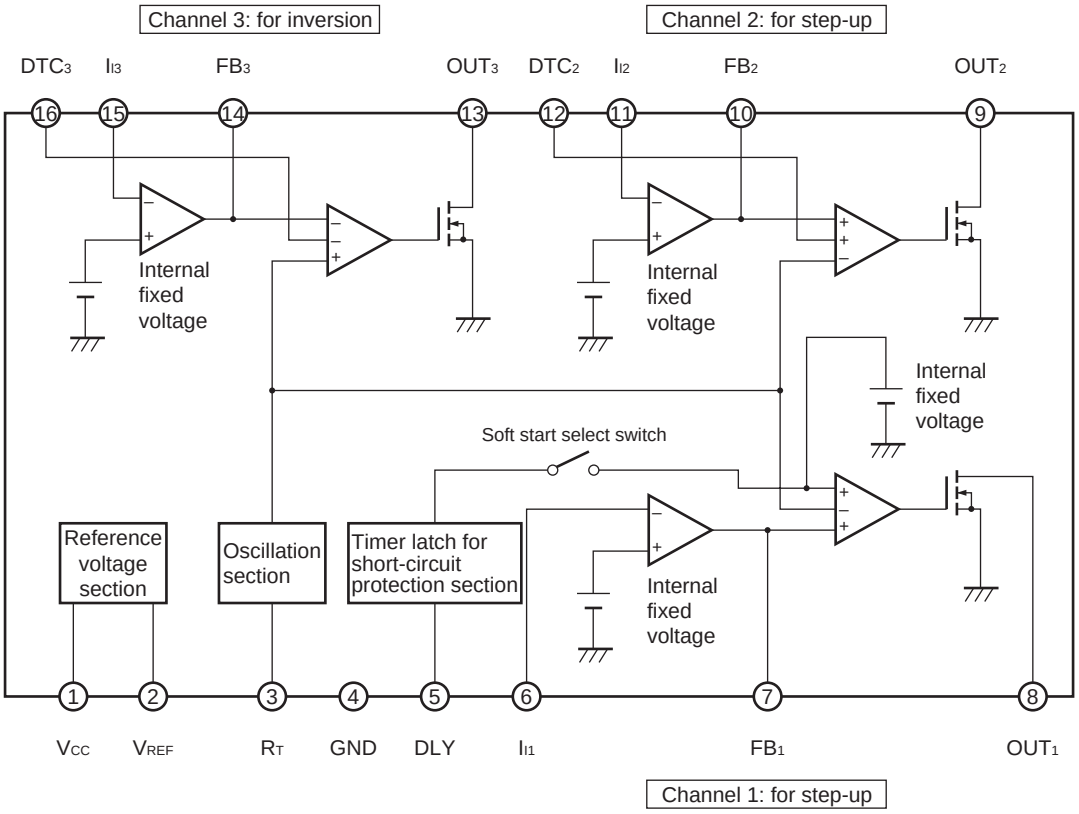
Printed in Japan

The mark ★ shows major revised points.

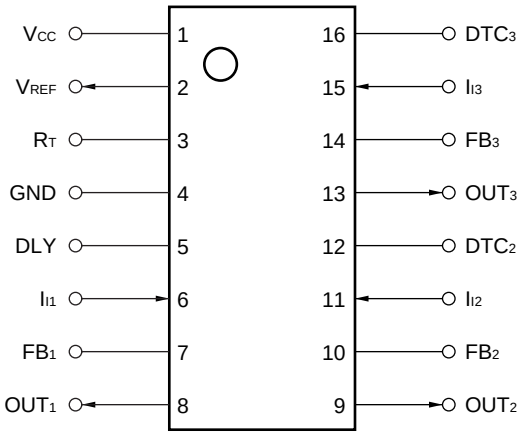
BLOCK DIAGRAM



PIN CONFIGURATION (Top view)

16-pin plastic TSSOP (5.72 mm (225))

• μPC1935GR



PIN FUNCTIONS

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	V_{CC}	Power supply	9	OUT_2	Channel 2 open-drain output
2	V_{REF}	Reference voltage output	10	FB_2	Channel 2 error amplifier output
3	R_T	Frequency setting resistor connection	11	I_{I2}	Channel 2 error amplifier inverted input
4	GND	Ground	12	DTC_2	Channel 2 dead time setting
5	DLY	Short-circuit protection/channel 1 soft start capacitor connection	13	OUT_3	Channel 3 open-drain output
6	I_{I1}	Channel 1 error amplifier inverted input	14	FB_3	Channel 3 error amplifier output
7	FB_1	Channel 1 error amplifier output	15	I_{I3}	Channel 3 error amplifier inverted input
8	OUT_1	Channel 1 open-drain output	16	DTC_3	Channel 3 dead time setting

CONTENTS

1. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (unless otherwise specified, T_A = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	30	V
Output voltage	V_O	30	V
Output current (open drain output)	I_O	21	mA
Total power dissipation	P_T	400	mW
Operating ambient temperature	T_A	–20 to + 85	°C
Storage temperature	T_{stg}	–55 to + 150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

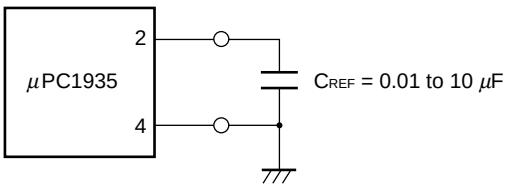
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	2.5		20	V
Output voltage	V_O	0		20	V
Output current	I_O			20	mA
Operating temperature	T_A	–20		+85	°C
Oscillation frequency	f_{OSC}	20		800	kHz

★ **Caution The recommended operating range may be exceeded without causing any problems provided that the absolute maximum ratings are not exceeded. However, if the device is operated in a way that exceeds the recommended operating conditions, the margin between the actual conditions of use and the absolute maximum ratings is small, and therefore thorough evaluation is necessary. The recommended operating conditions do not imply that the device can be used with all values at their maximum values.**

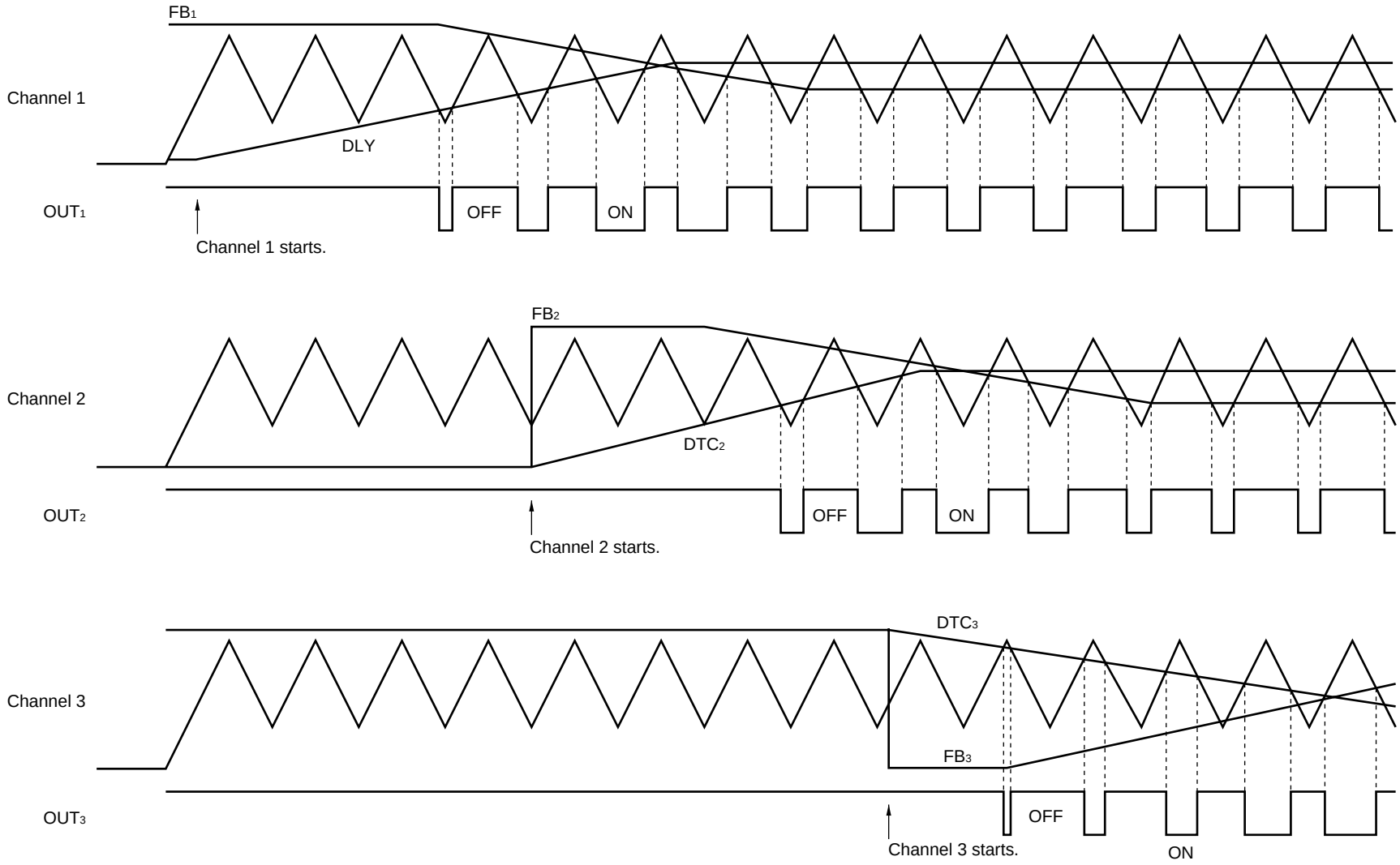
Electrical Characteristics (unless otherwise specified, T_A = 25 °C, V_{CC} = 3 V, f_{OSC} = 100 kHz)

	Block	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Under voltage lock-out section	Start-up voltage	$V_{CC\ (L-H)}$	I_{REF} = 0.1 mA		1.57		V
		Operation stop voltage	$V_{CC\ (H-L)}$	I_{REF} = 0.1 mA		1.5		V
		Hysteresis voltage	V_H	I_{REF} = 0.1 mA	30	70		mV
		Reset voltage (timer latch)	V_{CCR}	I_{REF} = 0.1 mA		1.0		V
	Reference voltage section	Reference voltage	V_{REF}	I_{REF} = 1 mA	2.0	2.1	2.2	V
		Line regulation	REG_{IN}	2.5 V≤V_{CC}≤20 V		2	12.5	mV
		Load regulation	REG_L	0.1 mA≤I_{REF}≤1 mA		1	7.5	mV
		Temperature coefficient	$\Delta V_{REF}/\Delta T$	–20 °C≤T_A≤+85 °C, I_{REF} = 0 A		0.5		%
	Oscillation section	f_{OSC} setting accuracy	Δf_{OSC}	R_T = 18 kΩ	–20		+30	%
		f_{OSC} total stability	Δf_{OSC}	–20 °C≤T_A≤+85 °C, 2.5 V≤V_{CC}≤20 V	–30		+50	%
	Duty setting section	Input bias current	I_{BD}	(Channels 2 and 3 only)			1.0	μA
		Channel 1 maximum duty	$D_{MAX.}$			85		%
		Channel 1 soft start time	t_{SS}	C_{DLY} = 0.1 μF		50		ms
		Low-level threshold voltage	$V_{TH\ (L)}$	Duty = 0 % (channels 1 and2) Duty = 100 % (channel 3)		1.2		V
		High-level threshold voltage	$V_{TH\ (H)}$	Duty = 100 % (channel 2) Duty = 0 % (channel 3)		1.6		V
	Error amplifier section	Input threshold voltage	V_{ITH}		0.285	0.3	0.315	V
		Input bias current	I_B		–100		+100	nA
		Open loop gain	A_V	V_O = 0.3 V	70	80		dB
		Unity gain	f_{unity}	V_O = 0.3 V		1.5		MHz
★		Maximum output voltage (+)	V_{OM}^+	I_O = –45 μA	1.6	2		V
★		Maximum output voltage (–)	V_{OM}^-	I_O = 45 μA		0.02	0.5	V
		Maximum sink current	I_{Osink}	V_{FB} = 0.5 V	0.8	1.4		μA
		Output source current	$I_{Osource}$	V_{FB} = 1.6 V		–70	–45	μA
★	Output section	Output ON voltage	V_{OL}	R_L = 150 Ω		0.2	0.6	V
		Rise time	t_r	R_L = 150 Ω		50		ns
		Fall time	t_f	R_L = 150 Ω		50		ns
★	Short-circuit protection section	Input sense voltage	V_{TH1}, V_{TH2}	Channels 1 and 2	1.75	1.9	2.05	V
★			V_{TH3}	Channel 3	0.5	0.63	0.75	V
★		UV sense voltage	V_{UV}			0.8	0.85	V
		Source current on short-circuiting	I_{OUV}		1.0	1.6	2.7	μA
		Delay time	t_{DLY}	C_{DLY} = 0.1 μF		50		ms
★	Overall	Circuit operation current	I_{CC}	V_{CC} = 3 V	1.8	3.1	5.1	mA

Caution Connect a capacitor of 0.01 to 10 μF to the V_{REF} pin.

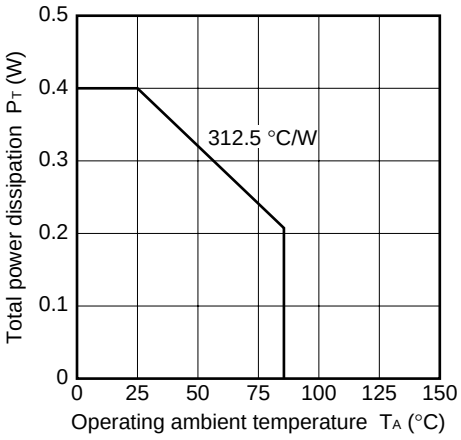


Timing Charts (sequence operation of power application → channel 1 → channel 2 → channel 3)

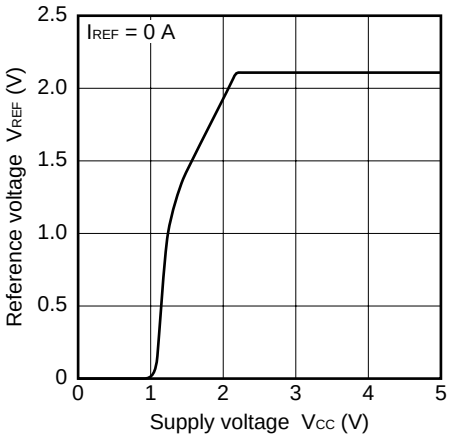


Typical Characteristic Curves (unless otherwise specified, V_{CC} = 3 V, f_{OSC} = 100 kHz, T_A = 25 °C) (Nominal)

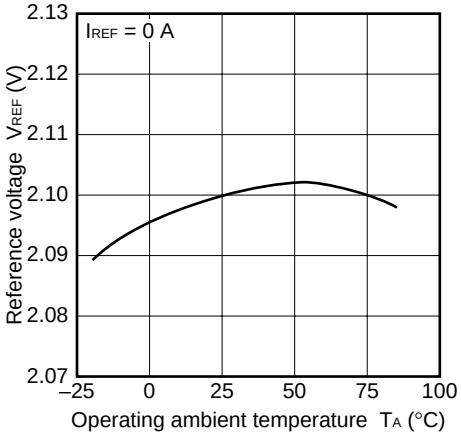
P_T vs T_A



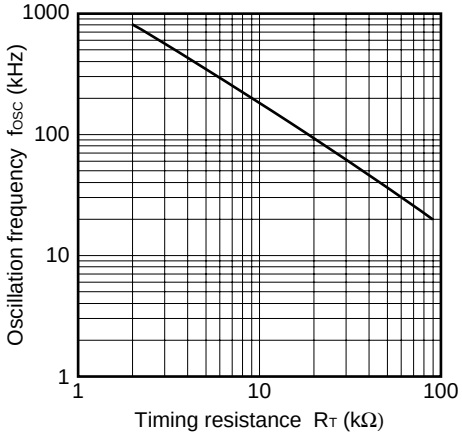
V_{REF} vs V_{CC}



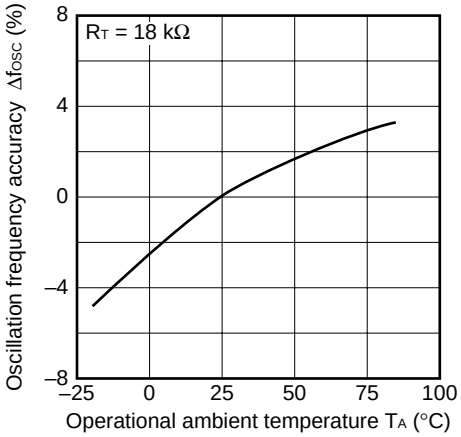
V_{REF} vs T_A



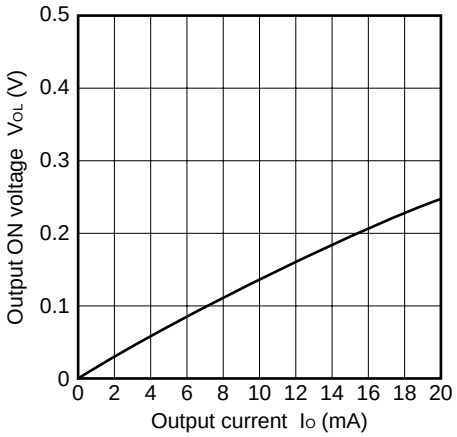
f_{OSC} vs R_T



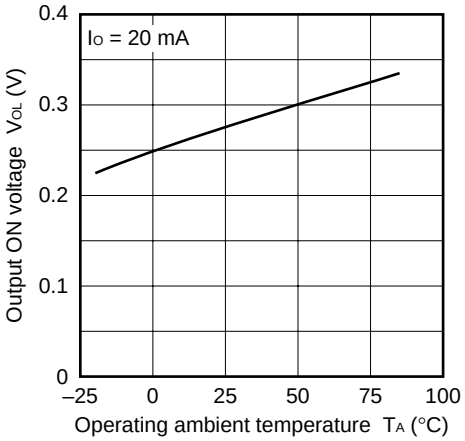
Δf_{OSC} vs T_A



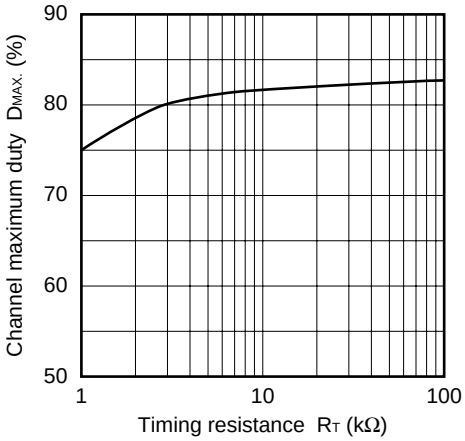
V_{OL} vs I_O



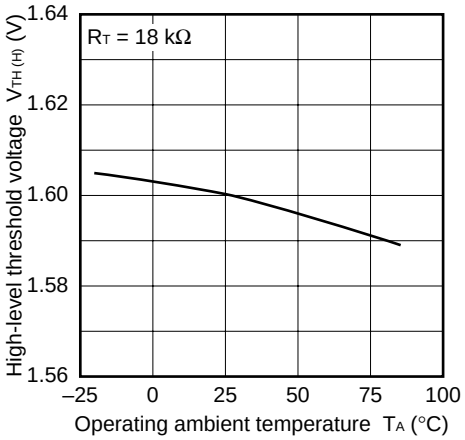
V_{OL} vs T_A



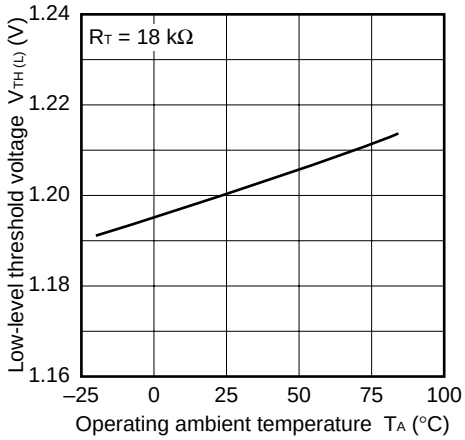
$D_{MAX.}$ vs R_T



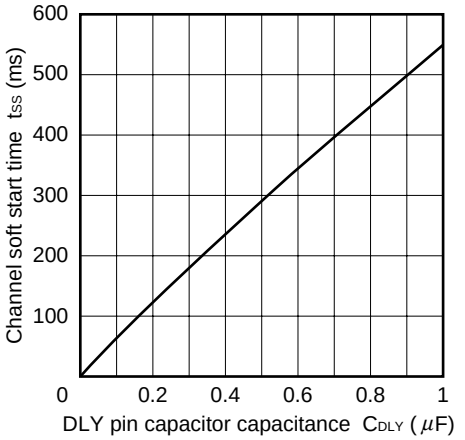
$V_{TH\,(H)}$ vs T_A



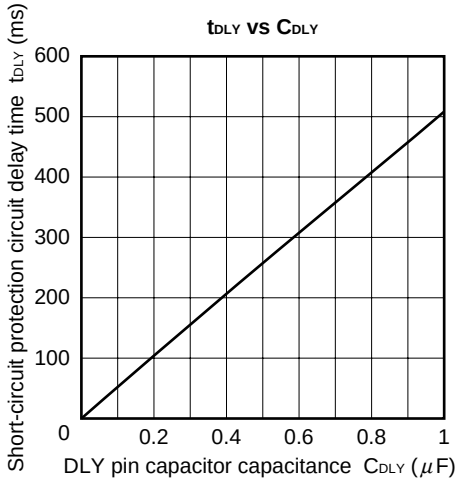
$V_{TH\,(L)}$ vs T_A



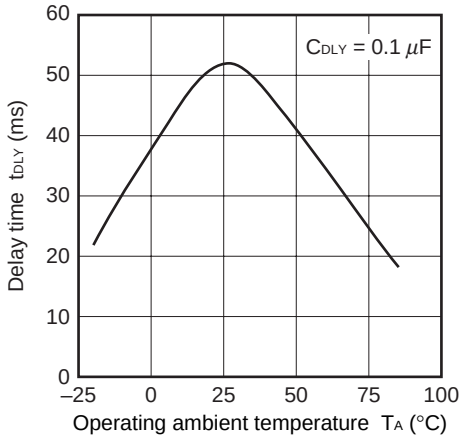
t_{SS} vs C_{DLY}



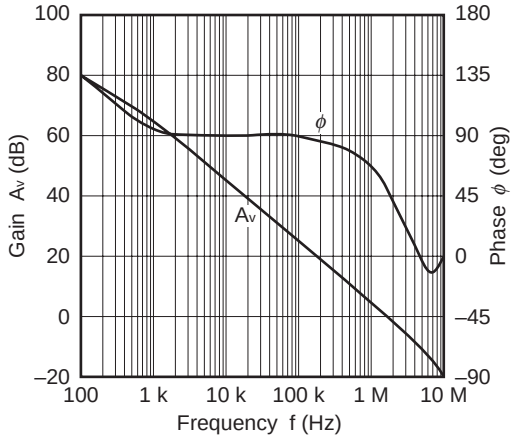
t_{DLY} vs C_{DLY}



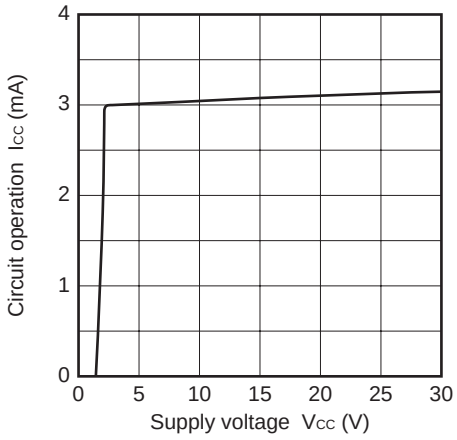
t_{DLY} vs T_A



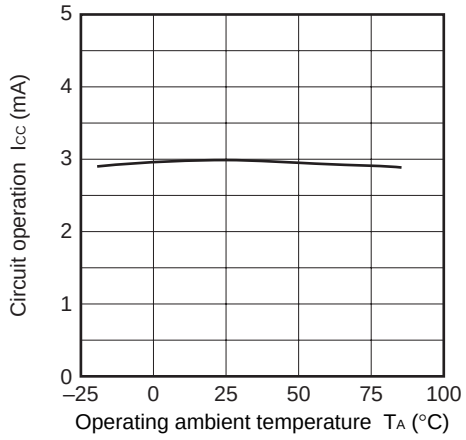
A_v, ϕ vs f



I_{CC} vs V_{CC}

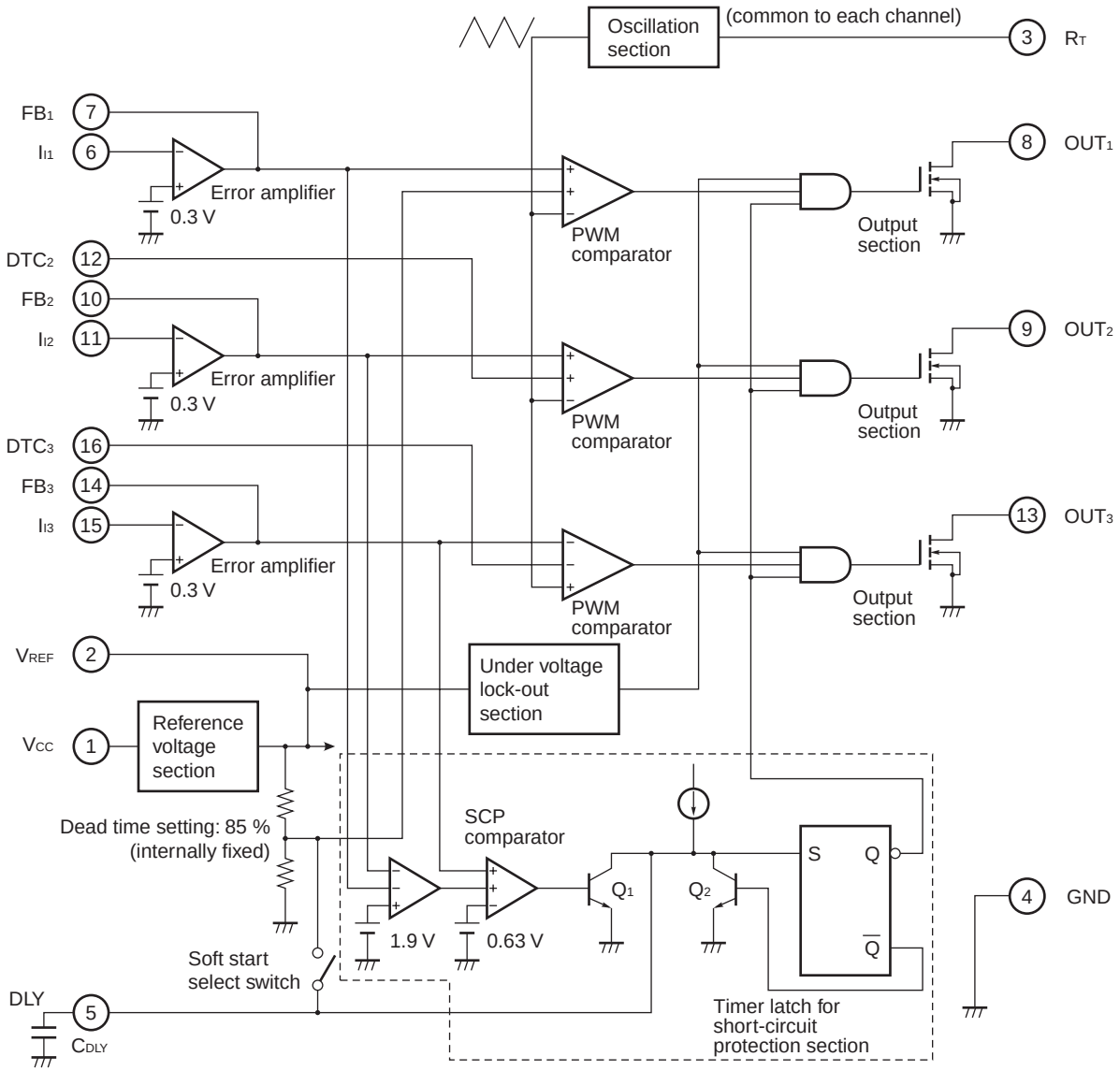


I_{CC} vs T_A



★ 2. CONFIGURATION AND OPERATION OF EACH BLOCK

Figure 2-1 Block Diagram



2.1 Reference Voltage Generator

The reference voltage generator is comprised of a band-gap reference circuit, and outputs a temperature-compensated reference voltage (2.1 V). The reference voltage can be used as the power supply for internal circuits, or as a reference voltage, and can also be accessed externally via the V_{REF} pin (pin 2).

2.2 Oscillator

The oscillator self-oscillates if a timing resistor is attached to the R_T pin (pin 3). This oscillator waveform is input to the inverted input pins (channel 1 and 2) or non-inverted input pin (channel 3) of the three PWM comparators to determine the oscillation frequency.

2.3 Under Voltage Lock-out Circuit

The under voltage lock-out circuit prevents malfunctioning of the internal circuits when the supply voltage is low, such as when the supply voltage is first applied, or when the power supply is interrupted. When the voltage is low, the three output transistors are cut off at the same time.

2.4 Error Amplifiers

The non-inverted input pins of the error amplifiers E/A_1, E/A_2, and E/A_3 are connected internally to 0.3 V (the input threshold voltages are all 0.3 V (TYP.)). The circuits of the error amplifiers E/A_1, E/A_2, and E/A_3 are exactly the same. The first stage of the error amplifier is a P-channel MOS transistor input.

2.5 PWM Comparators

The output ON duty is controlled according to the outputs of the error amplifiers and the voltage input to the Dead Time Control pin (fixed internally for channel 1).

A triangular waveform is input to the inverted pin, and the error amplifier output and Dead Time Control pin voltage (fixed internally for channel 1) are input to the non-inverted pins of the PWM comparators for channel 1 and channel 2. Therefore, the output transistor ON period is the period when the triangular waveform is lower than the error amplifier output and Dead Time Control pin voltage (fixed internally for channel 1).

Channel 3 is the logical inverse of channel 1 and channel 2. Consequently, the triangular waveform is input to the non-inverted input pin, and the error amplifier output and Dead Time Control pin voltage are input to the inverted input pins of the PWM comparator for channel 3. Therefore, the transistor ON period is the period when the triangular waveform is higher than the error amplifier output and Dead Time Control pin voltage (refer to **Timing Charts**).

2.6 Timer Latch-Method Short Circuit Protection Circuit

When the outputs of the converters for each channel drop, the FB outputs of the error amplifiers of those outputs go high (FB_3 output goes low). If the FB output exceeds the timer latch input detection voltage (V_{TH} = 1.9 V) (FB_3 output goes lower than the timer latch input detection voltage (V_{TH} = 0.63 V)), then the output of the SCP comparator goes low, and Q_1 goes off.

When Q_1 turns OFF, the constant-current supply charges C_{DLY} via the DLY pin. The DLY pin is internally connected to a flip-flop. When the DLY pin voltage reaches the UV detection voltage (V_{UV} = 0.8 V (TYP.)), the output Q of the flip-flop goes low, and the output stage of each channel is latched to OFF (refer to **Figure 2-1 Block Diagram**).

The logic of channels 1 and 2 is reverse to that of channel 3. Consequently, an inverter circuit is inserted between the FB output of channels 1 and 2, and SCP comparator input.

Make the power supply voltage briefly less than the reset voltage (V_{CCR}, 1.0 V TYP.) to reset the latch circuit when the short-circuit protection circuit has operated.

2.7 Output Circuit

The output circuit has an N-channel open-drain output providing an output withstand voltage of 30 V (absolute maximum rating), and an output current of 21 mA (absolute maximum rating).

★ 3. NOTES ON USE

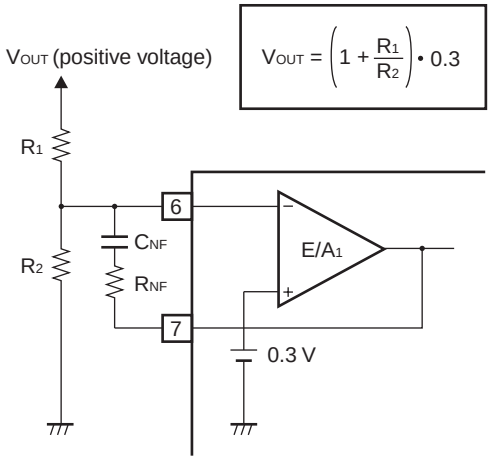
3.1 Setting the Output Voltage

Figure 3-1 illustrates the method of setting the output voltage. The output voltage is obtained using the formula shown in the figure.

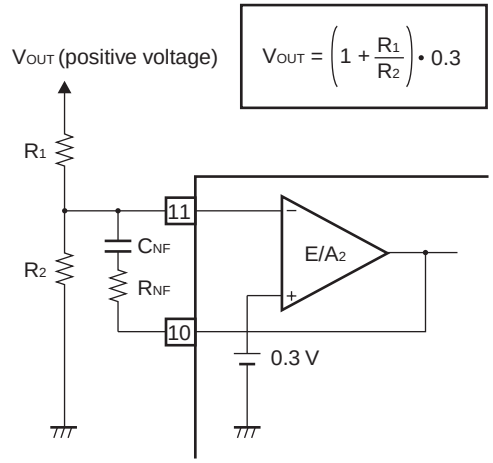
The input threshold value of the error amplifier is 0.3 V (TYP.) for all the error amplifiers, E/A1, E/A2, and E/A3. Therefore, select a resistor value that gives this voltage.

Figure 3-1 Setting the Output Voltage

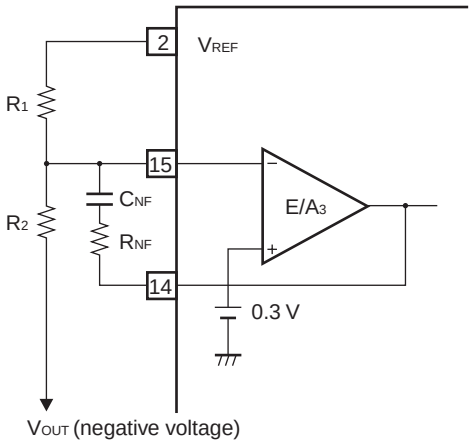
(1) When setting a positive output voltage using error amplifier E/A1.



(2) When setting a positive output voltage using error amplifier E/A2.



(3) When setting a negative output voltage using error amplifier E/A3.



$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \cdot 0.3 - \frac{R_2}{R_1} \cdot V_{REF}$$

3.2 Setting the Oscillation Frequency

Choose R_T according to the oscillation frequency (f_{OSC}) vs timing resistor (R_T) characteristics (refer to **Typical Characteristics Curves f_{OSC} vs R_T**). The formula below (3-1) gives an approximation of f_{OSC}. However, the result of formula 3-1 is only an approximation, and the value must be confirmed in actual operation, especially for high-frequency operation.

$f_{OSC}[Hz] \cong 1.856 \times 10^9 / R_T[\Omega]$ (3-1)

3.3 Preventing Malfunction of the Timer Latch-Method Short Circuit Protection Circuit

The timer latch short-circuit protection circuit operates when the error amplifier outputs of channel 1 or channel 2 (pin 7 and 10) exceed approximately 1.9 V, or when the error amplifier output of channel 3 (pin 14) goes below approximately 0.63 V, and cuts off the output. However, if the rise of the power supply voltage is fast, or if there is noise on the DLY pin (pin 5), the latch circuit may malfunction and cut the output off.

To prevent this, keep the wiring impedance between the DLY pin and the GND pin (pin 4) low, and avoid applying noise to the DLY pin.

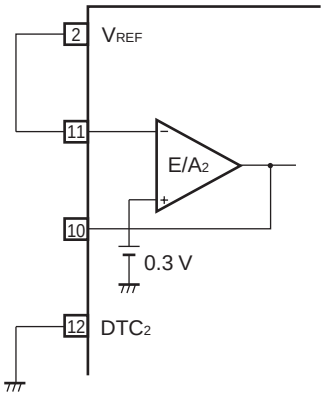
3.4 Connecting Unused Error Amplifiers

When the unused circuit of the three control circuits provided internally is error amplifier E/A2, connect the circuit in such a way as to make sure that the output of the error amplifier is low. When the unused circuit is error amplifier E/A3, connect the circuit in such a way as to make sure that the output of the error amplifier is high. In the case of error amplifier E/A1, the Dead Time Control pin is fixed internally, so be sure to always use this amplifier.

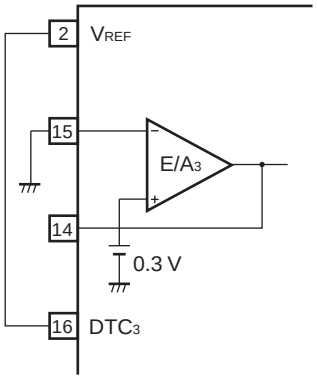
Figure 3-2 shows examples of how to connect unused error amplifiers.

Figure 3-2 Examples of Connecting Unused Error Amplifiers

(1) Error amplifier E/A2



(2) Error amplifier E/A3

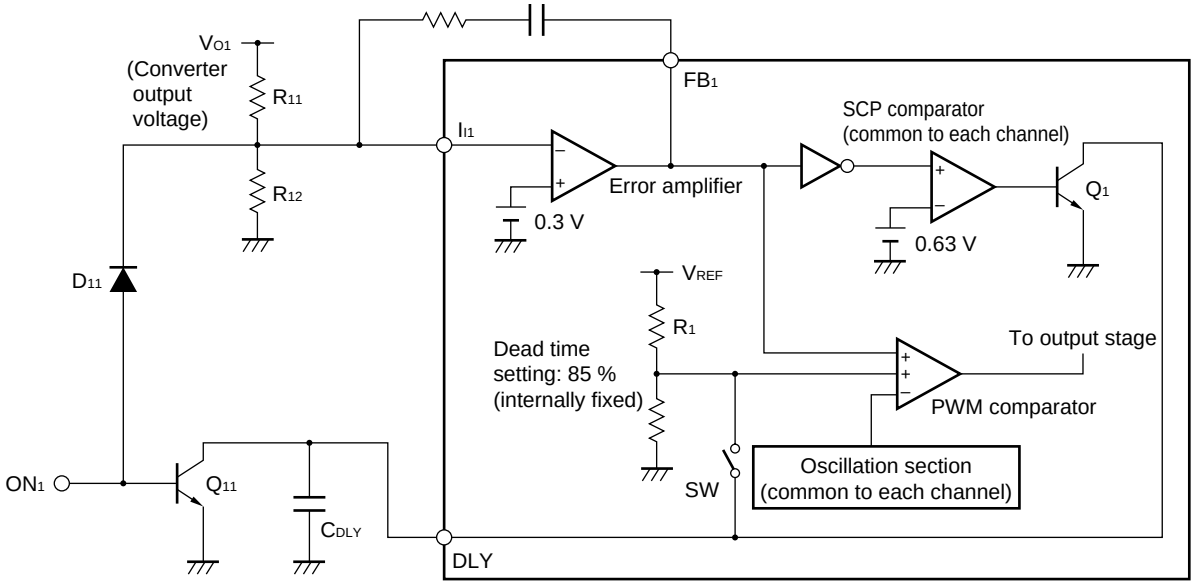


3.5 ON/OFF Control

3.5.1 Channel 1 (for step-up)

The ON/OFF signal control method of the output oscillation of channel 1 is to input the ON/OFF signal from ON_1 as shown in Figure 3-3. For channel 1, soft start or timer latch (SCP) is internally selected. Soft start is executed when the first start signal is input. When the end of soft start is detected, the soft start select switch is turned OFF and the timer latch circuit operates.

Figure 3-3 ON/OFF Control (channel 1 for step-up)



(1) When ON_1 is high: OFF status

Q_{11}: ON → DLY pin: Low level → Output duty of PWM comparator: 0 %

D_{11}: ON → I_{I1} pin: High level → FB_1 output: Low level

(2) When ON_1 is low: ON status (start up)

Q_{11}: OFF → C_{DLY} is charged in the sequence of [V_{REF} → R_1 → SW → DLY pin → C_{DLY}] → Soft start

D_{11}: OFF → I_{I1} pin: Low level → FB_1 output: High level

(3) When ON_1 goes high again after start up (SW: OFF): OFF status

Q_{11}: ON → DLY pin: Low level (Nothing happens because SW is OFF.)

D_{11}: ON → I_{I1} pin: High level → FB_1 output: Low level → PWM comparator output duty: 0 %

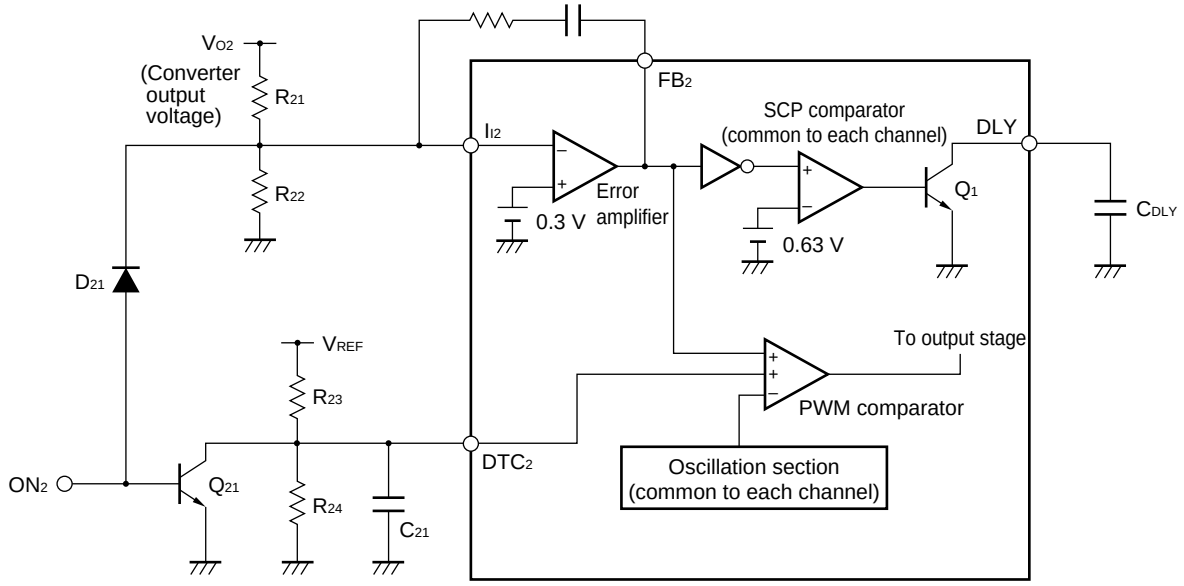
→ Converter output voltage (V_{O1}) drops.

Caution Even if start up is executed by making ON_1 low again after (3), soft start is not executed because the soft start select switch (SW) remains OFF. To execute soft start of channel 1 again, drop V_{CC} to 0 V once.

3.5.2 Channel 2 (for step-up)

The ON/OFF signal control method of the output oscillation of channel 2 is to input the ON/OFF signal from ON_2 as shown in Figure 3-4. The PWM converter can be turned ON/OFF by controlling the level of the DTC_2 pin. However, it is necessary to keep the level of the FB_2 output low (the SCP comparator input high) so that the timer latch does not start when the PWM converter is OFF. In this circuit example, the FB_2 output level is controlled by controlling the level of the I_{I2} pin.

Figure 3-4 ON/OFF Control (channel 2: step-up)



(1) When ON_2 is high: OFF status

Q_{21}: ON → DTC_2 pin: Low level → Output duty of PWM comparator: 0 %

D_{21}: ON → I_{I2} pin: High level → FB_2 output: Low level → SCP comparator output: High level → Timer latch stops.

(2) When ON_2 is low: ON status

Q_{21}: OFF → C_{21} is charged in the sequence of [V_{REF} → R_{23} → C_{21}] → DTC_2 pin voltage rises → Soft start

D_{21}: OFF → I_{I2} pin: Low level → FB_2 output: High level → SCP comparator output: Low level → Q_1 is OFF

→ Charging C_{DLY} starts (timer latch start).

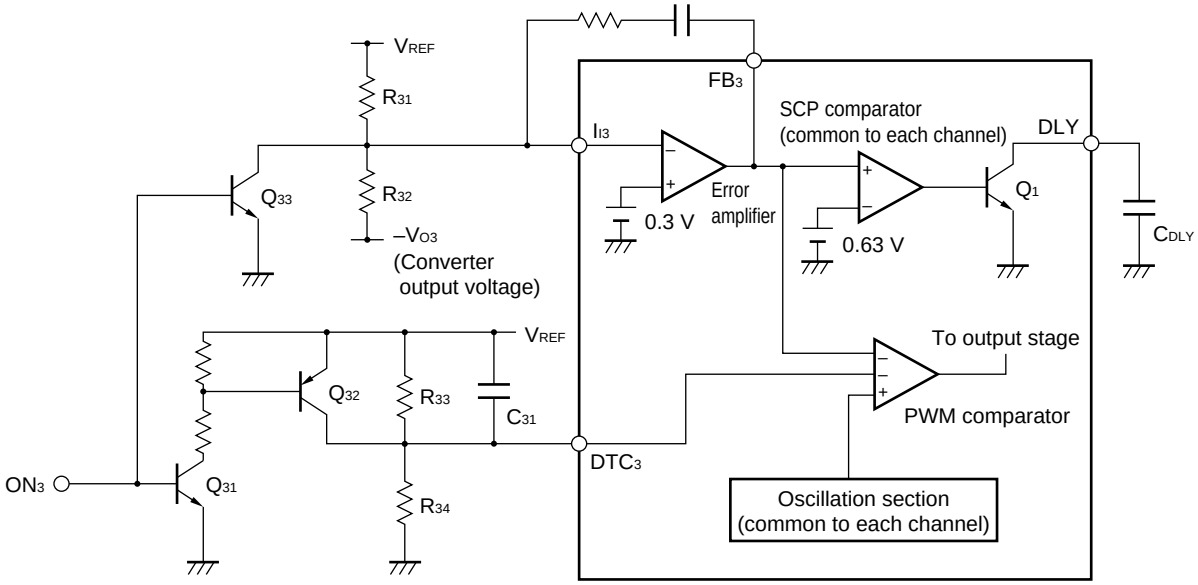
Caution Keep the low-level voltage of the DTC_2 pin within 1.2 V and the high-level voltage of the I_{I2} pin at 0.3 V or higher. The maximum voltage that is applied to the I_{I2} pin must be equal to or lower than V_{REF}.

3.5.3 Channel 3 (for inverted output)

The ON/OFF signal control method of the output oscillation of channel 3 is to input the ON/OFF signal from ON_3 as shown in Figure 3-5. The PWM converter can be turned ON/OFF by controlling the level of the DTC_3 pin. However, it is necessary to keep the level of the FB_3 output high so that the timer latch does not start when the PWM converter is OFF. In this circuit example, the FB_3 output level is controlled by controlling the level of the I_{I3} pin.

Because channel 3 supports an inverted converter, its PWM comparator logic is different from that of channels 1 and 2.

Figure 3-5 ON/OFF Control (channel 3: for inverted output)



(1) When ON_3 is high: OFF status

Q_{31}: ON → Q_{32}: ON → DTC_3 pin: High level → Output duty of PWM comparator: 0 %

Q_{33}: ON → I_{I3} pin: Low level → FB_3 output: High level → SCP comparator output: High level → Q_1 is ON.

→ Timer latch stops.

(2) When ON_3 is low: ON status

Q_{31}: OFF → Q_{32} is OFF. → C_{31} is charged in the sequence of [V_{REF} → C_{31} → R_{34}] → DTC_3 pin voltage drops.

→ Soft start

Q_{33}: OFF → I_{I3} pin: High level → FB_3 output: Low level → SCP comparator output: Low level → Q_1: OFF

→ Charging C_{DLY} starts (timer latch start).

Caution Keep the high-level voltage of the DTC_3 pin at 1.6 V or higher and the low-level voltage of the I_{I3} pin within 0.3 V. The maximum voltage that is applied to the I_{I3} pin must be equal to or lower than V_{REF}.

3.6 Maximum Duty Limit

Channel 1 is switched internally between Soft Start and Timer Latch. For this reason, the DTC voltage is fixed internally, and the maximum duty is limited to 85%.

The DTC voltage for channel 2 and channel 3 can be set externally, so the maximum duty is not limited.

3.7 Notes on Actual Pattern Wiring

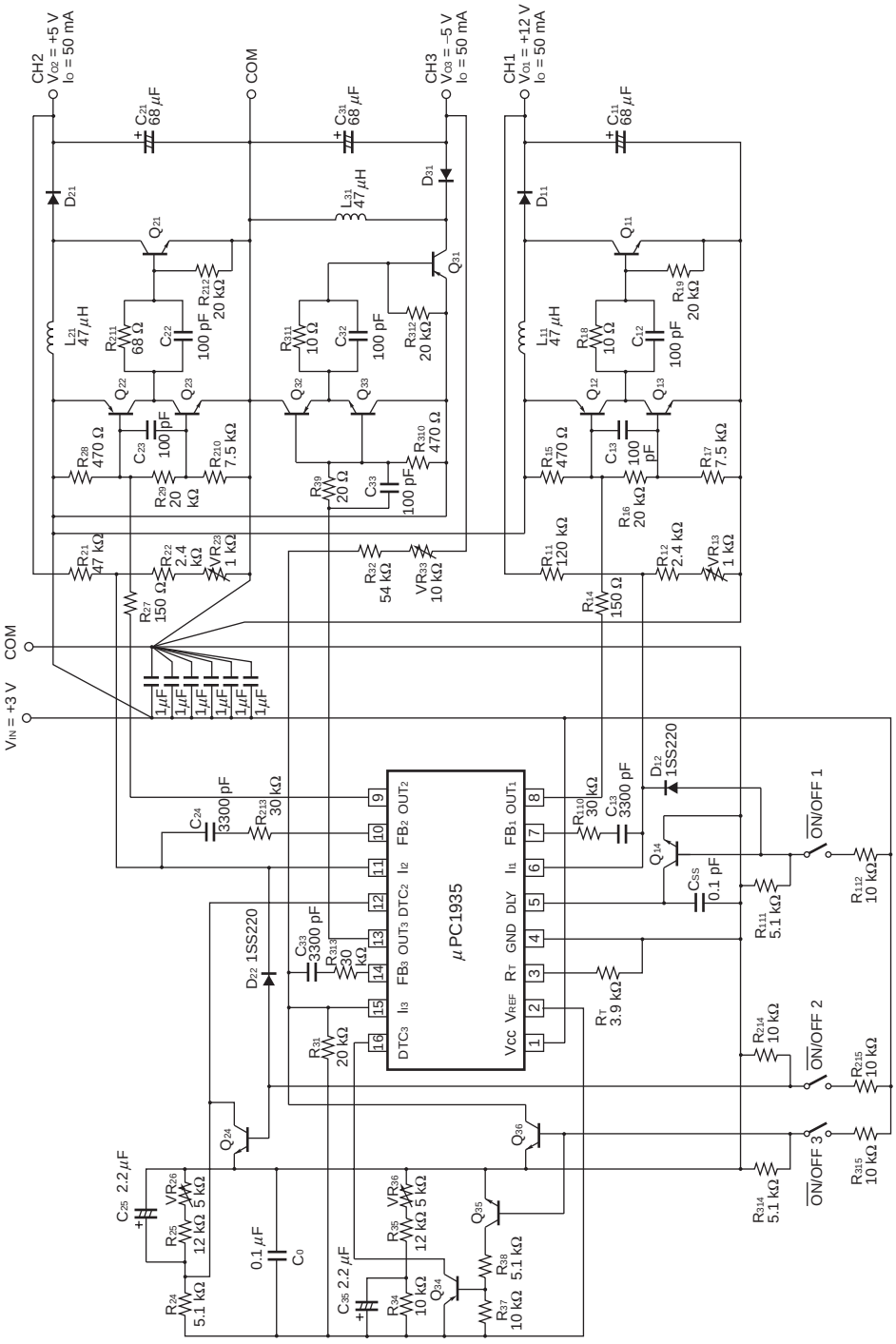
When actually carrying out the pattern wiring, it is necessary to separate control-related grounds and power-related grounds, and make sure that they do not share impedances as far as possible. In addition, make sure the high-frequency impedance is lowered using capacitors and other components to prevent noise input to the V_{REF} pin.

★ 4. APPLICATION EXAMPLE

4.1 Application Example

Figure 4-1 shows an example circuit for obtaining ±5 V/50 mA and +12 V/50 mA from a +3 V power supply.

Figure 4-1 Chopper-Method/Inverting-Type Switching Regulator



4.2 List of External Parts

The list below shows the external parts.

Table 4-1 List of External Parts

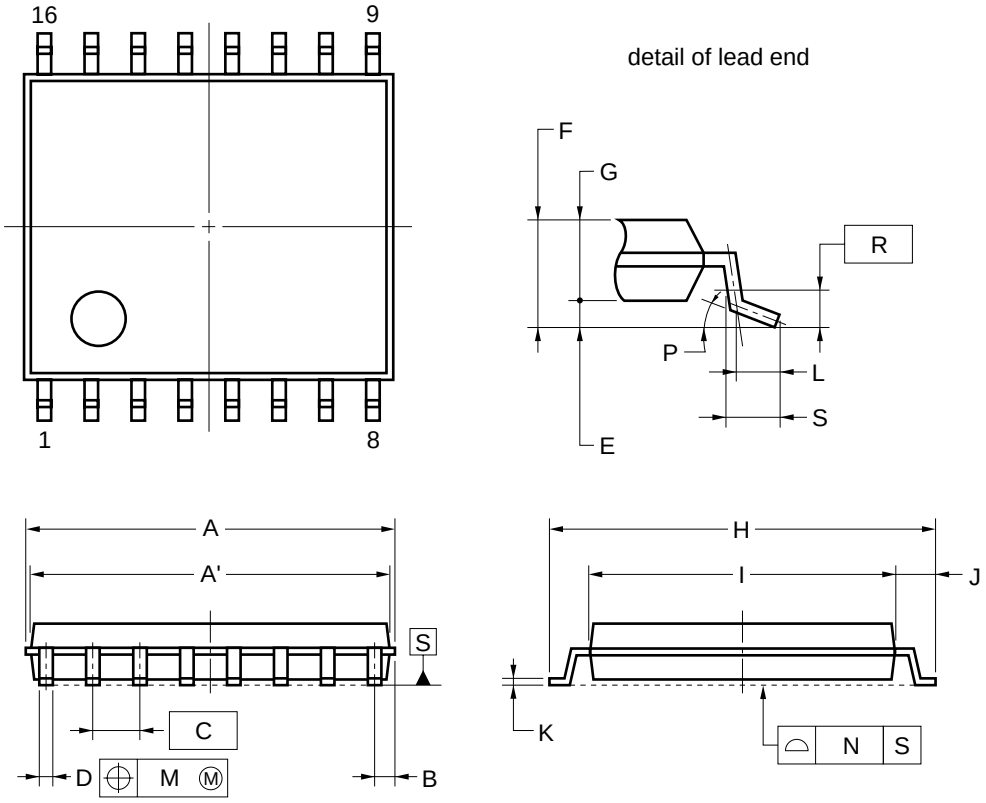
Symbol	Parameter	Function	Part number	Maker	Remark
C_{11}	68 μF	Output capacitor	20SA68M	SANYO	OS-CON, SA series
D_{11}		Schottkey diode	D1FS4	SHINDENGEN	
L_{11}	47 μH	Choke inductor	636FY-470M	TOKO	D73F series
Q_{11}		Switching transistor	2SD2403	NEC	
Q_{12}		Buffer transistor	2SA812	NEC	
Q_{13}		Buffer transistor	2SC1623	NEC	
D_{12}		Switching diode	1SS220	NEC	
Q_{14}		Transistor for switch	2SK2158	NEC	
C_{21}	68 μF	Output capacitor	20SA68M	SANYO	OS-CON, SA series
D_{21}		Schottkey diode	D1FS4	SHINDENGEN	
L_{21}	47 μH	Choke inductor	636FY-470M	TOKO	D73F series
Q_{21}		Switching transistor	2SD2403	NEC	
Q_{22}		Buffer transistor	2SA812	NEC	
Q_{23}		Buffer transistor	2SC1623	NEC	
D_{22}		Switching diode	1SS220	NEC	
Q_{24}		Transistor for switch	2SK2158	NEC	
C_{31}	68 μF	Output capacitor	20SA68M	SANYO	OS-CON, SA series
D_{31}		Schottkey diode	D1FS4	SHINDENGEN	
L_{31}	47 μH	Choke inductor	636FY-470M	TOKO	D73F series
Q_{31}		Switching transistor	2SB1572	NEC	
Q_{32}		Buffer transistor	2SA812	NEC	
Q_{33}		Buffer transistor	2SC1623	NEC	
Q_{34}		Transistor for switch	2SA812	NEC	
Q_{35}		Transistor for switch	2SC1623	NEC	
Q_{36}		Transistor for switch	2SC1624	NEC	

Remarks 1. The capacitors that are not specified in the above list are multilayer ceramic capacitors.

2. The resistors that are not specified in the above list are 1/4W resistors.

5. PACKAGE DRAWING

16-PIN PLASTIC TSSOP (5.72 mm (225))



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.15±0.15
A'	5.0±0.1
B	0.375 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.06}_{-0.04}$
E	$0.09^{+0.06}_{-0.04}$
F	$1.01^{+0.09}_{-0.06}$
G	0.92
H	6.4±0.2
I	4.4±0.1
J	1.0±0.2
K	$0.145^{+0.055}_{-0.045}$
L	0.5
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.6±0.15

S16GR-65-PJG-1

6. RECOMMENDED SOLDERING CONDITIONS

Recommended solder conditions for this product are described below.

For details on recommended soldering conditions, refer to Information Document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Surface Mount Type

μPC1935GR: 16-pin plastic TSSOP (5.72 mm (225))

Soldering Method	Soldering Conditions	Symbol of Recommended Conditions
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX. (210 °C MIN.), Number of times: 3 MAX.	IR35-00-3
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX. (200 °C MIN.), Number of times: 3 MAX.	VP15-00-3
Wave soldering	Soldering bath temperature: 260 °C MAX., Time: 10 seconds MAX., Number of times: 1, Preheating temperature: 120 °C MAX. (package surface temperature)	WS60-00-1

Caution Do not use two or more soldering methods in combination.

[MEMO]

[MEMO]

NOTES FOR BiCMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS

Note:

No connection for device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. Input levels of devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF BiCMOS DEVICES

Note:

Power-on does not necessarily define initial status of device. Production process of BiCMOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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