NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8125GR

UP-CONVERTER WITH AGC FUNCTION + QUADRATURE MODULATOR IC FOR DIGITAL MOBILE COMMUNICATION SYSTEMS

DESCRIPTION

The μPC8125GR is a sillicon monolithic integrated circuit designing as indirect quadrature modulator for digital mobile communication systems. This modulator consists of 1.8 GHz to 2.0 GHz up-converter with AGC function and 220 MHz to 270 MHz quadrature modulator which are packaged in 20-pin SSOP. The device has power save function and can operate 2.7 to 5.5 V supply voltage. Therefore, it can contribute to make RF block small, high performance and low power consumption.

FEATURES

- LPF is incorporated in the latter of 90° phase shifter for Lo1 Carrier leak and its Lo1 × n spurious level.
- Supply voltage: V_{CC} = 2.7 to 5.5 V
- External IF filter can be applied between modulator output and up-converter input terminal.
- Equipped with power save function.
- Equipped with AGC function : Gain control range 40 dB TYP. @f = 1.9 GHz

APPLICATIONS

- Digital cordless phones: ex) PHS (Personal Handy Phone System)

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPC8125GR-E1	20 pin plastic SSOP (225 mil)	Embossed tape, 12 mm wide. Pins 1 through 10 are in pull-out direction. Qty 2.5 kp/reel.

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μPC8125GR, Quantity: 20 pcs/unit)

Caution Electro-static sensitive device

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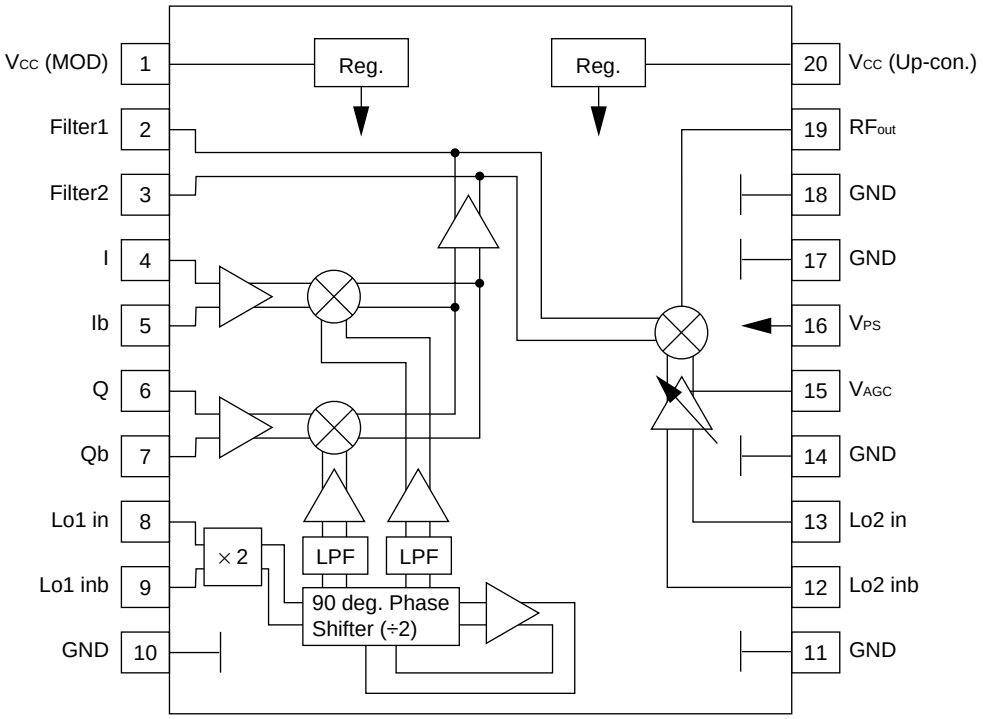
Printed in Japan

The mark ★ shows major revised points.

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS (Top View)

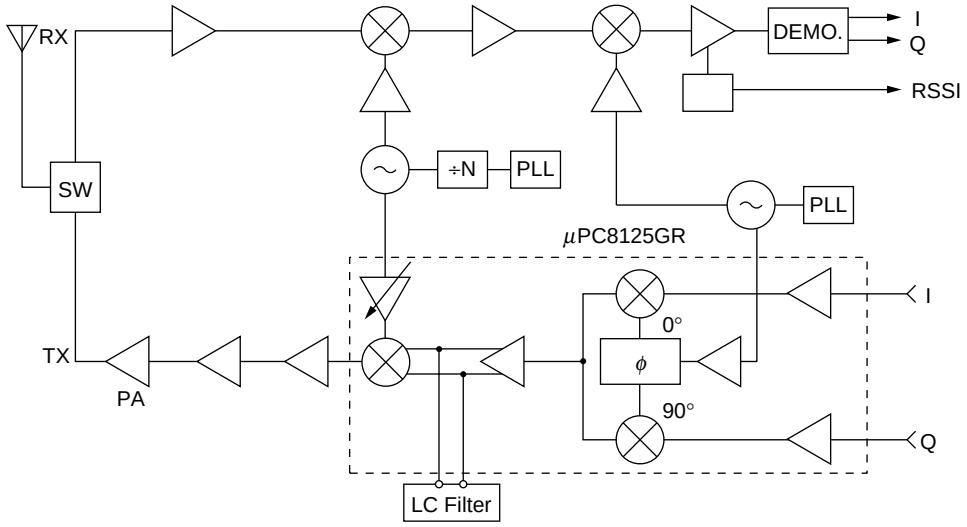


★ QUADRATURE MODULATOR SERIES PRODUCT

Part Number	Functions	I_{CC} (mA)	f_{LO1in} (MHz)	f_{MODout} (MHz)	RF Mixer f_{RFout} (MHz)	Phase Shifter	Package	Application
μPC8101GR	150 MHz Quad.Mod	15/@2.7 V	100 to 300	50 to 150	External	F/F	20-pin SSOP (225 mil)	CT-2 etc.
μPC8104GR	RF Up-Converter + IF Quad.Mod	28/@3.0 V	100 to 400		900 to 1 900	Doubler + F/F		Digital Comm.
μPC8105GR	400 MHz Quad.Mod	16/@3.0 V	100 to 400		External		16-pin SSOP (225 mil)	
μPC8110GR	1 GHz Direct Quad.Mod	24/@3.0 V	800 to 1 000		External		20-pin SSOP (225 mil)	PDC800 MHz, etc.
μPC8125GR	RF Up-Converter + IF Quad.Mod + AGC	36/@3.0 V	220 to 270		1 800 to 2 000			PHS
μPC8126GR	900 MHz Direct Quad.Mod with Offset-Mixer	35/@3.0 V	915 to 960		915 to 960			PDC800 MHz
μPC8126K			889 to 960		889 to 960		28-pin QFN	
μPC8129GR	×2LO IF Quad. Mod+RF Up-Converter	28/@3.0 V	200 to 800	100 to 400	800 to 1 900	F/F	20-pin SSOP (225 mil)	GSM, DCS1800, etc.
μPC8139GR-7JH	Transceiver IC (1.9 GHz Indirect Quad. Mod + RX-IF + IF VCO)	TX: 32.5 RX: 4.8 /@3.0 V	220 to 270		1 800 to 2 000	CR	30-pin TSSOP (225 mil)	PHS
μPC8158K	RF Up-Converter + IF Quad.Mod + AGC	28/@3.0 V	100 to 300		800 to 1 500		28-pin QFN	PDC800 M/1.5 G

Remark Please refer to the data sheet of each part number.

APPLICATION EXAMPLE (PHS)



CONTENTS

1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{CC}	T_A = +25 °C	6.0	V
Power Save Control Voltage	V_{PS}	T_A = +25 °C	6.0	V
AGC Control Voltage	V_{AGC}	T_A = +25 °C	6.0	V
IQ DC Offset Voltage	$IQ_{(DC)}$	T_A = +25 °C, 4 to 7 pins	4.0	V
Power Dissipation	P_D	T_A = +85 °C Note	430	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C

Note Mounted on a 50 × 50 × 1.6 mm double copper clad epoxy glass PWB.

2. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		2.7	3.0	5.5	V
Operating Ambient Temperature	T_A		–40	+25	–85	°C
Up-converter RF Frequency	f_{RFout}		1 800	–	2 000	MHz
Up-converter Input Frequency	$f_{UPCONin}$		220	–	270	MHz
Modulator Output Frequency	f_{MODout}					
Lo1 Input Frequency	f_{Lo1in}	P_{Lo1in} = –10 dBm				
Lo2 Input Frequency	f_{Lo2in}	P_{Lo2in} = –10 dBm	1 500	–	1 800	MHz
I/Q Input Frequency	$f_{I/Qin}$	$V_{I/Qin}$ = 500 mVp-p max. (Single ended Input) $V_{I/Qin}$ = 250 mVp-p max. (Differential Input)	DC	–	10	MHz
Lo1 Input Level	P_{Lo1in}		–11.5	–10	–5	dBm
Lo2 Input Level	P_{Lo2in}		–15	–10	–5	dBm
I/Q Input amplitude	$V_{I/Qin}$	Single ended Input	–	–	500	mVp-p
		Differential Input			250	

3. ELECTRICAL CHARACTERISTICS

(T_A = +25 °C, V_{CC} = 3.0 V, unless otherwise specified V_{AGC} = 3.0 V, Vps = 3.0 V, R_{AGC} = 10 kΩ, Rps = 1 kΩ, I/Q (DC) = Ib/Qb (DC) = V_{CC}/2 = 1.5 V, $f_{I/Qin}$ = 24 kHz, $V_{I/Qin}$ = 500 mVp-p (Single ended) or 250 mVp-p (Differential Input), π/4DQPSK modulation, Data rate: 384 kbps, Filter roll off: α = 0.5, MOD pattern: all zero [0000], f_{Lo1in} = 250 MHz, P_{Lo1in} = –10 dBm, f_{Lo2in} = 1 650 MHz, P_{Lo2in} = –10 dBm, f_{RFout} = 1 900 MHz + $f_{I/Qin}$)

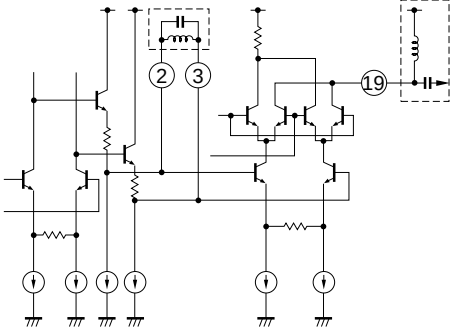
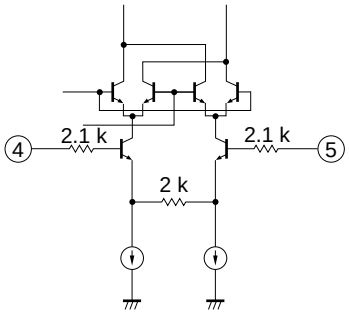
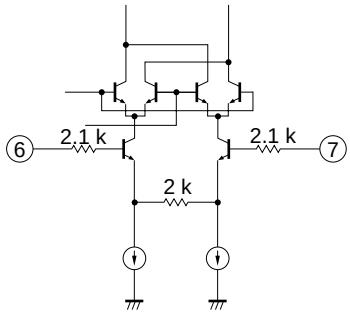
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
UP-CONVERTER + QUADRATURE MODULATOR TOTAL						
Total Circuit Current	$I_{CC\ TOTAL}$	No input signal	30	36	48	mA
Total Circuit Current at Sleep Mode	$I_{CC(PS)\ TOTAL}$	V_{PS} ≤ 0.5 V (Low)	–	0.3	10	μA
Total Output Power 1	$P_{RFout\ 1}$	V_{AGC} = 3.0 V	–13	–9	–5	dBm
Lo Carrier Leakage	LoL	f_{Lo1} + f_{Lo2}	–	–37	–30	dBc
Image Rejection (Side Band Leakage)	ImR		–	–35	–30	dBc
I/Q 3rd Order Intermodulation Distortion	$IM_{3(I/Q)}$		–	–50	–30	dBc
AGC Amp. Gain control range	GCR	V_{AGC} = 2.5 V to 0 V	28	40	–	dB
Power Save Rise Time	$T_{PS(Rise)}$	$V_{PS(Low)}$ → $V_{PS(High)}$	–	2	5	μs
Power Save Fall Time	$T_{PS(Fall)}$	$V_{PS(Low)}$ → $V_{PS(High)}$	–	5	10	μs
Error Vector Magnitude	EVM	MOD Pattern: PN9	–	2.5	4.5	%rms
Adjacent Channel Power	P_{adj}	Δf = 600 kHz MOD Pattern: PN9	–	–68	–60	dBc

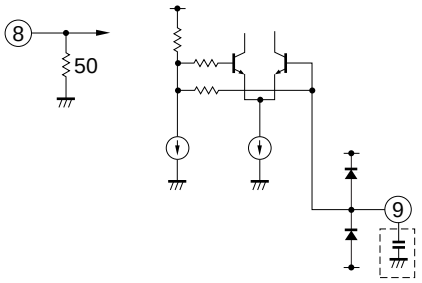
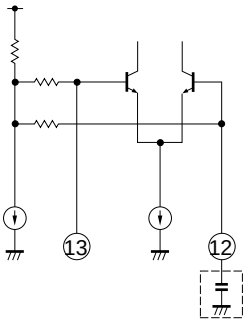
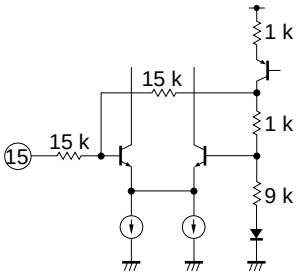
4. STANDARD CHARACTERISTICS FOR REFERENCE

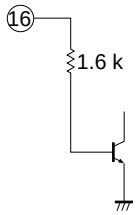
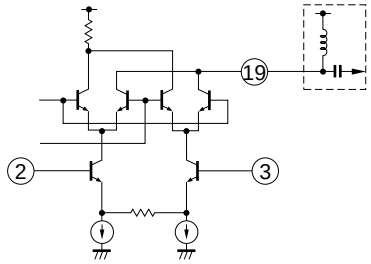
(T_A = +25 °C, V_{CC} = 3.0 V, unless otherwise specified V_{AGC} = 3.0 V, Vps = 3.0 V, R_{AGC} = 10 kΩ, Rps = 1 kΩ, I/Q (DC) = Ib/Qb (DC) = V_{CC}/2 = 1.5 V, $f_{I/Qin}$ = 24 kHz, $V_{I/Qin}$ = 500 mVp-p (Single ended) or 250 mVp-p (Differential Input), π/4DQPSK modulation, Data rate: 384 kbps, Filter roll off: α = 0.5, MOD pattern: all zero [0000], f_{Lo1in} = 250 MHz, P_{Lo1in} = –10 dBm, f_{Lo2in} = 1 650 MHz, P_{Lo2in} = –10 dBm, f_{RFout} = 1 900 MHz + $f_{I/Qin}$)

Parameter	Symbol	Test Conditions	Reference	Unit
UP-CONVERTER + QUADRATURE MODULATOR TOTAL				
Lo1 × n Spurious Level	$P_{SUP(Lo1)}$	Lo1 × 7, Lo1 × 7 (Image) Lo1 × 8, Lo1 × 8 (Image)	–60	dBc
Total Output Power	$P_{RFout\ 2}$	V_{AGC} = 0.5 V	–50	dBm
I/Q Input Inpedance	$Z_{I/Qin}$	$f_{I/Qin}$ = 24 kHz, I to Ib, Q to Qb	200	kΩ
I/Q Bias Current	$I_{I/Q}$	I, Ib, Q, Qb to GND (each)	5	μA
Lo1 Input VSWR	Z_{Lo1in}	f_{Lo1} = 220 M to 270 MHz	1.2:1	

5. PIN EXPLANATIONS

Pin NO.	Symbol	Supply Voltage (V)	Pin Voltage Typ. (V) @V_{CC} = 3 V	Function and Description	Internal Equivalent Circuit
1	V_{CC}(MOD.)	2.7 to 5.5	–	Supply voltage pin for the modulator. Internal regulator can be kept stable condition of supply bias against the variable temperature or V_{CC}.	
2	Filter1	–	1.9	Filter pin can control spurious (Lo1 × n) by insertion BPF between Filter2 pin.	
3	Filter2	–	1.9	Filter pin can control spurious (Lo1 × n) by insertion BPF between Filter1 pin.	
4	I	V_{CC}/2	–	Input for I signal. This input impedance is 200 kΩ. In case of that I/Q input signals are single ended, amplitude of the signal is 500 mVp-p max. See **Chapter 6**.	
5	Ib	V_{CC}/2	–	Input for I signal. This input impedance is 200 kΩ. In case of that I/Q input signals are single ended, V_{CC}/2 biased DC signal should be input. In case of the I/Q input signals are differential, amplitude of the signal is 250 mVp-p max. See **Chapter 6**.	
6	Q	V_{CC}/2	–	Input for Q signal. This input impedance is 200 kΩ. In case of that I/Q input signals are single ended, amplitude of the signal is 500 mVp-p max. See **Chapter 6**.	
7	Qb	V_{CC}/2	–	Input for I signal. This input impedance is 200 kΩ. In case of that I/Q input signals are single ended, V_{CC}/2 biased DC signal should be input. In case of the I/Q input signals are differential, amplitude of the signal is 250 mVp-p max. See **Chapter 6**.	

Pin NO.	Symbol	Supply Voltage (V)	Pin Voltage Typ. (V) @V_{CC} = 3 V	Function and Description	Internal Equivalent Circuit
8	Lo1 in	–	0	Lo input for the phase shifter. This input impedance is internally matched to 50 Ω.	
9	Lo1 inb	–	2.4	Bypass of the Lo1 input. This pin is grounded through external capacitor.	
10 11	GND (MOD.)	–	0	Ground pin for modulator block. Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
12	Lo2 inb	–	1.9	Bypass of the Lo2 input. This pin is grounded through external capacitor.	
13	Lo2 in	–	1.9	Lo input for the up-converter. This pin is high impedance input, and should be matched external circuit.	
14 17 18	GND (Up-con.)	–	0	Ground pin for up-Converter. Connect to the ground with minimum impedance. Track length should be kept as short as possible.	
15	V_{AGC}	0 to V_{CC}	–	Control voltage input pin for AGC amplitude. RF output level can be governed by supply voltage to this pin. AGC performance can be adjustable R_{AGC} value.	

Pin NO.	Symbol	Supply Voltage (V)	Pin Voltage Typ. (V) @V_{CC} = 3 V	Function and Description	Internal Equivalent Circuit
16	V_{PS}	0 to V_{CC}	–	Power save control pin for phase shifter and up-converter can controlled the On/Sleep state with bias as follows: V_{PS}(V) / STATE 2 to V_{CC} / ON (Active Mode) 0 to 0.5 / OFF (Sleep Mode)	
19	RF_{out}	V_{CC}	–	RF output from up-converter. This pin is open collector output and should be matched external circuit.	
20	V_{CC} (Up-con.)	2.7 to 5.5	–	Supply voltage pin for the up-converter. An internal regulator helps keep the device stable against temperature or V_{CC} variation.	———

: Externally

6. RELATIONS BETWEEN AMPLITUDE AND Vcc/2 BIAS OF I/Q INPUT SIGNALS

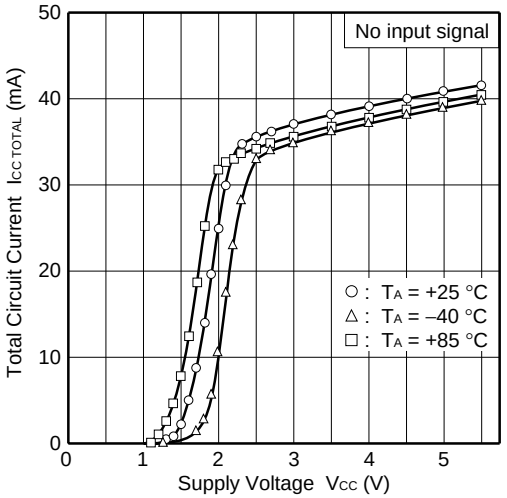
Supply voltage V_{CC}(V)	I/Q DC Voltage(V) $V_{CC}/2$ = I = Ib = Q = Qb	I/Q Input signal (mVp-p)	
		Single ended input I = Q	Differential input I = Ib = Q = Qb
2.7 to 3.0 to 5.5	1.35 to 1.5 to 2.75	≤ 500	≤ 250

7. STANDARD TYPICAL CHARACTERISTICS

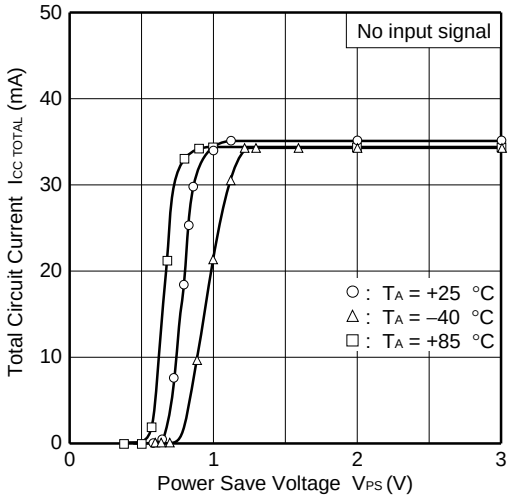
T_A = +25 °C, V_{CC} = Vps = 3 V, V_{AGC} = 3 V, R_{AGC} = 10 kΩ, Rps = 1 kΩ, I/Q (DC) = Ib/Qb (DC) = V_{CC}/2 = 1.5 V,
$f_{I/Qin}$ = 24 kHz, $V_{I/Qin}$ = 500 mVp-p (Single ended), Data rate: 384 kbps, Filter roll off: α = 0.5,
MOD pattern: all zero [0000], f_{Lo1in} = 250 MHz, P_{Lo1in} = –10 dBm, f_{Lo2in} = 1 650 MHz, P_{Lo2in} = –10 dBm,
f_{RFout} = 1 900 MHz + $f_{I/Qin}$ unless otherwise specified

7.1 DC Performance

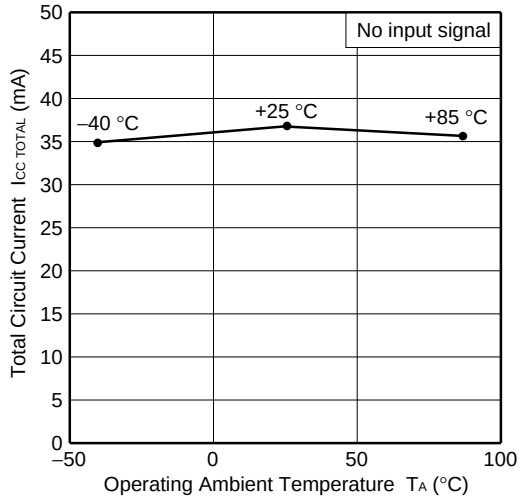
TOTAL CIRCUIT CURRENT vs. SUPPLY VOLTAGE



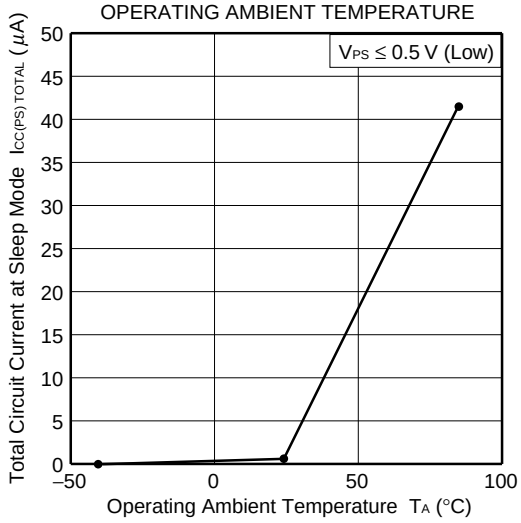
TOTAL CIRCUIT CURRENT vs. POWER SAVE VOLTAGE



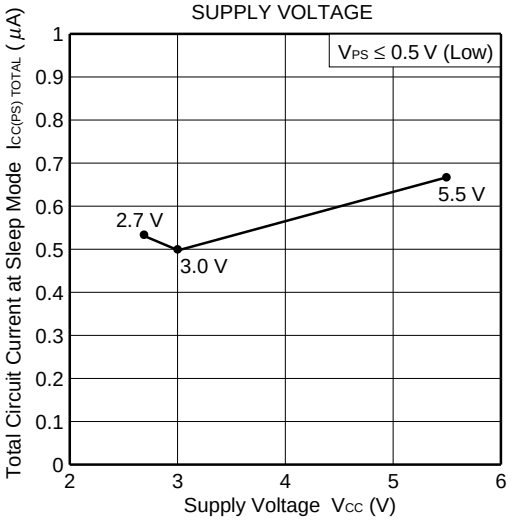
TOTAL CIRCUIT CURRENT vs.
OPERATING AMBIENT TEMPERATURE



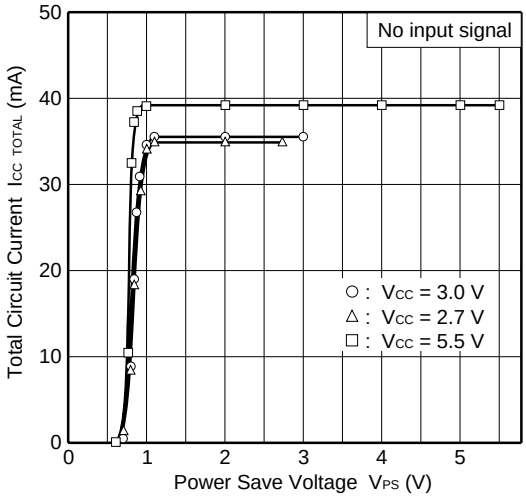
TOTAL CIRCUIT CURRENT AT SLEEP MODE vs.
OPERATING AMBIENT TEMPERATURE



TOTAL CIRCUIT CURRENT AT SLEEP MODE vs.
SUPPLY VOLTAGE

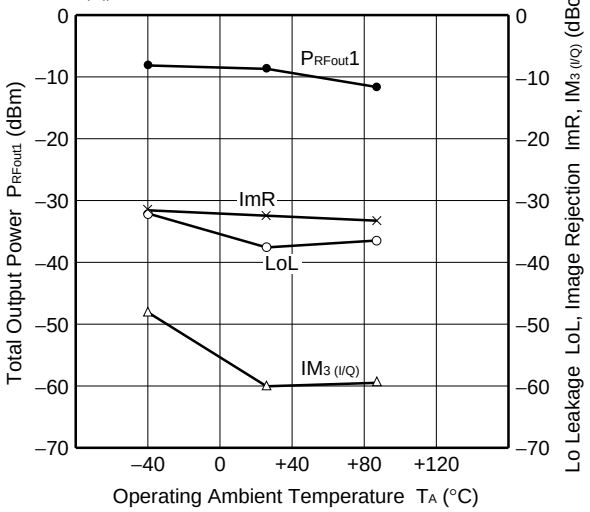


TOTAL CIRCUIT CURRENT vs.
POWER SAVE VOLTAGE

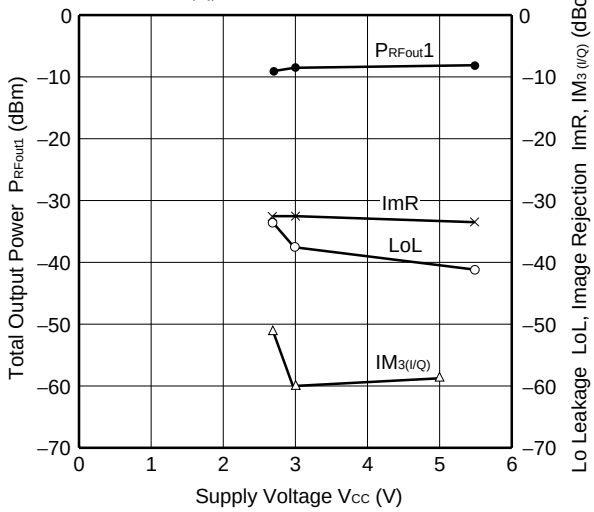


7.2 Output Performance

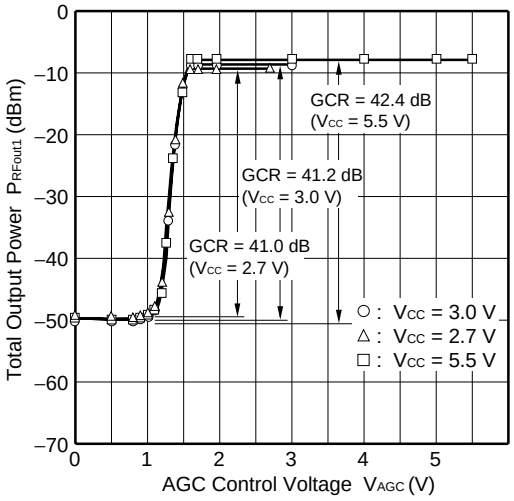
TOTAL OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION, $IM_{3\,(I/Q)}$ vs. OPERATING AMBIENT TEMPERATURE



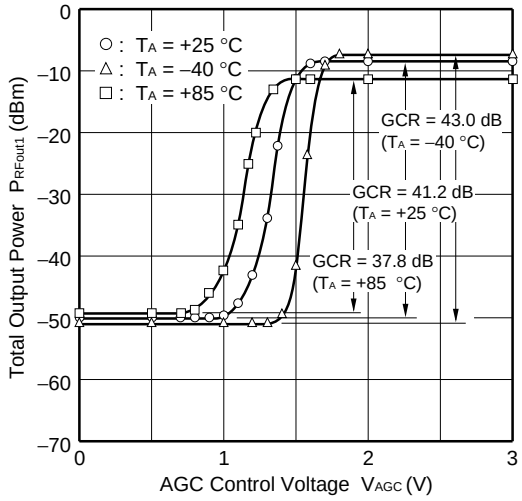
TOTAL OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION, $IM_{3\,(I/Q)}$ vs. SUPPLY VOLTAGE



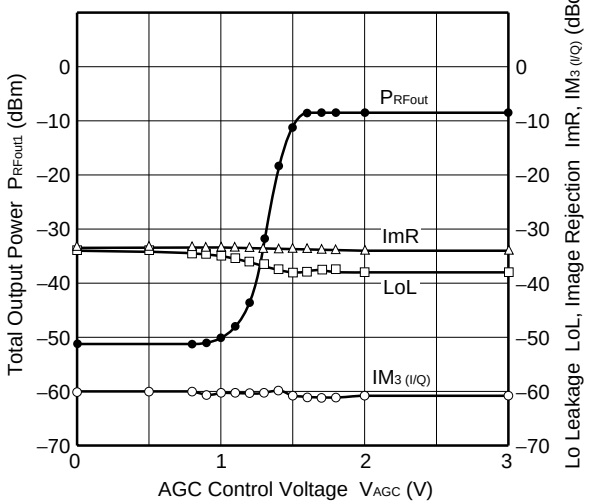
TOTAL OUTPUT POWER vs. AGC CONTROL VOLTAGE



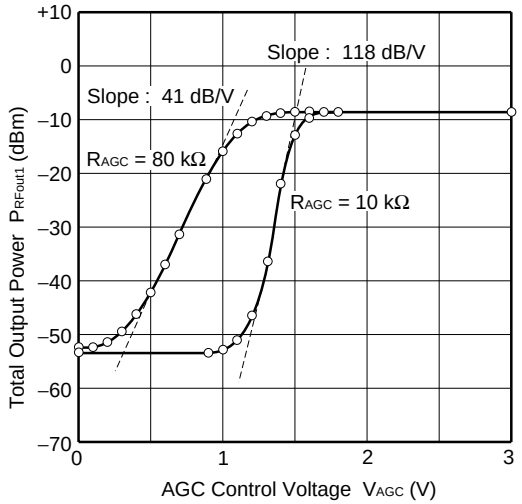
TOTAL OUTPUT POWER vs. AGC CONTROL VOLTAGE



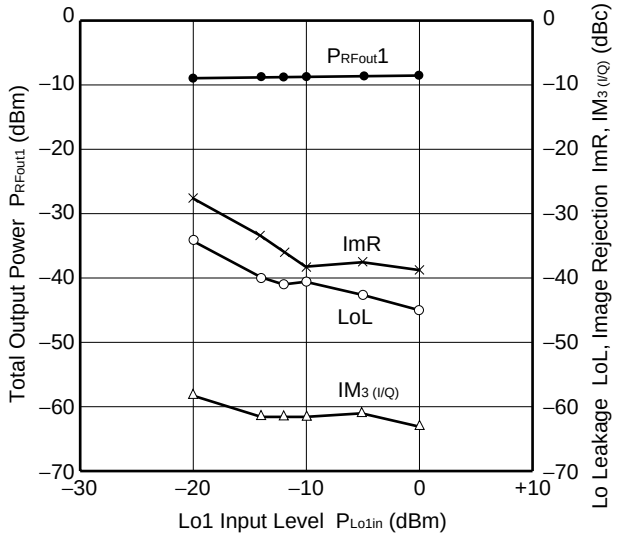
TOTAL OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION, $IM_{3\,(I/Q)}$ vs. AGC CONTROL VOLTAGE



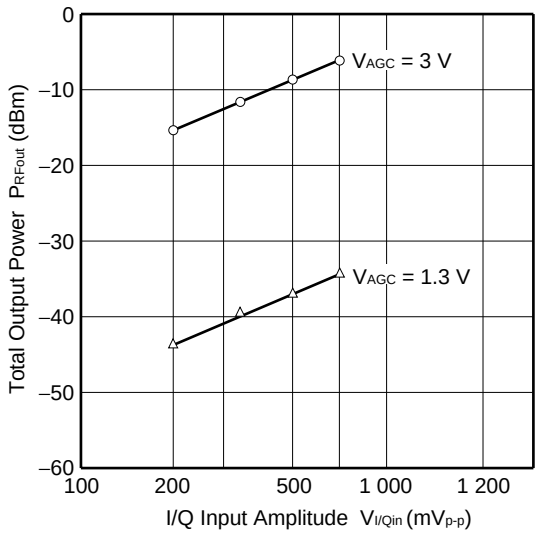
TOTAL OUTPUT POWER vs. AGC CONTROL VOLTAGE



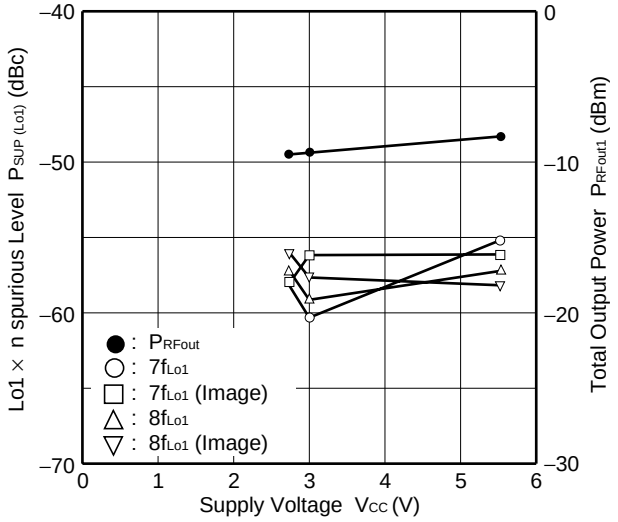
TOTAL OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION, $IM_{3\,(I/Q)}$ vs. LO1 INPUT LEVEL



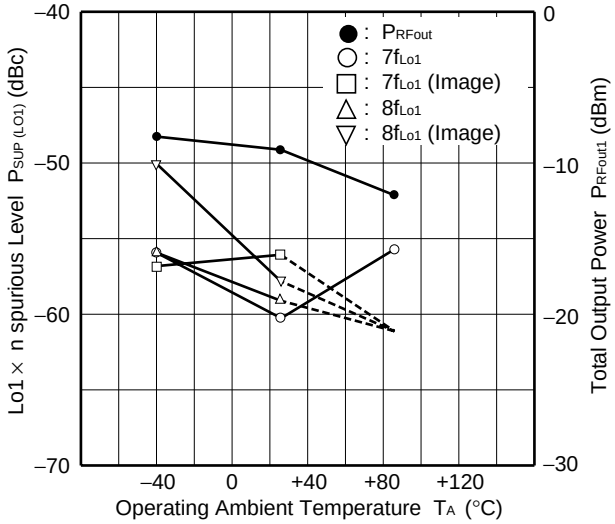
TOTAL OUTPUT POWER vs. I/Q INPUT AMPLITUDE



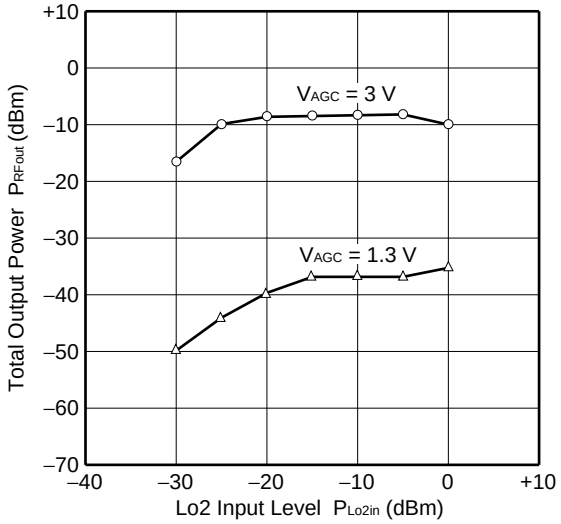
LO1 × N SPURIOUS LEVEL, TOTAL OUTPUT POWER vs. SUPPLY VOLTAGE



LO1 × N SPURIOUS LEVEL, TOTAL OUTPUT POWER vs. OPERATING AMBIENT TEMPERATURE

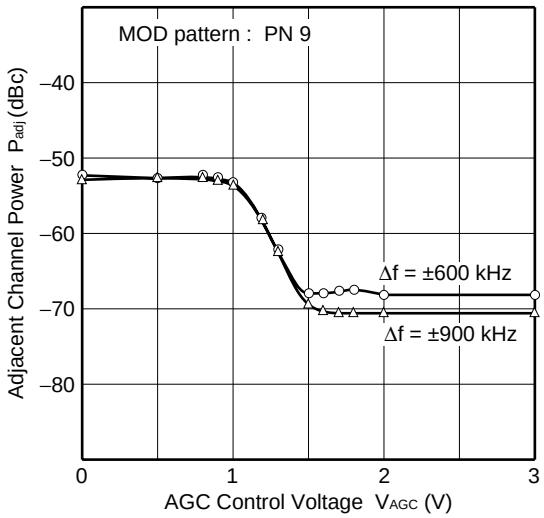


TOTAL OUTPUT POWER vs. LO2 INPUT LEVEL

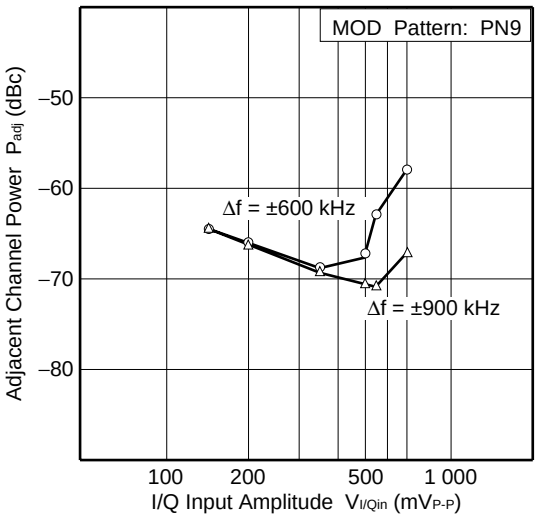


7.3 Adjacent Channel Interference Power

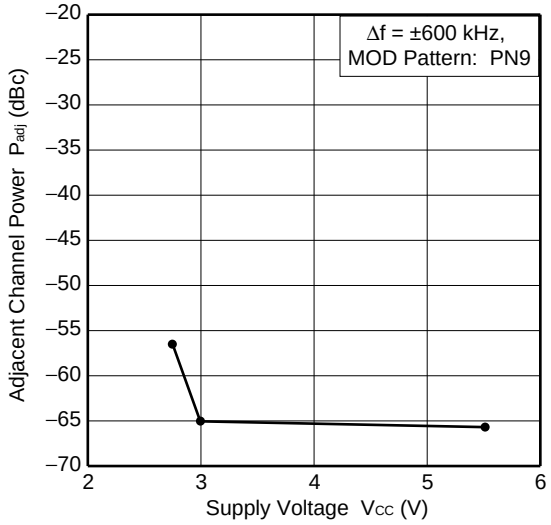
ADJACENT CHANNEL POWER vs. AGC CONTROL VOLTAGE



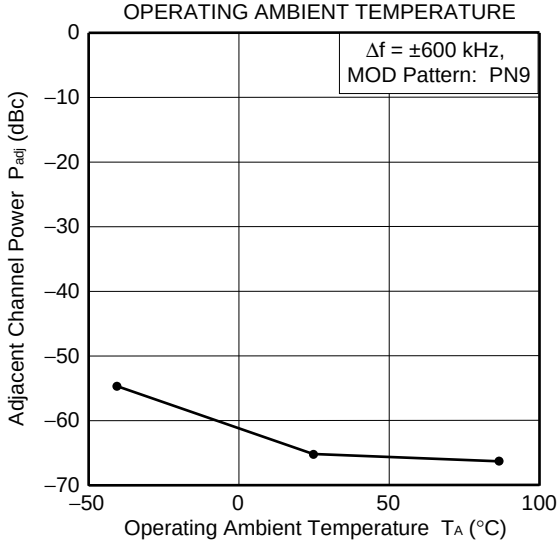
ADJACENT CHANNEL POWER vs. I/Q INPUT AMPLITUDE



ADJACENT CHANNEL POWER vs. SUPPLY VOLTAGE

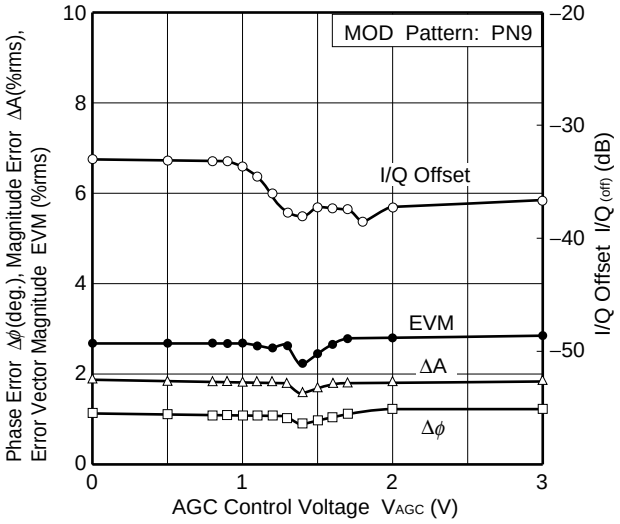


ADJACENT CHANNEL POWER vs. OPERATING AMBIENT TEMPERATURE

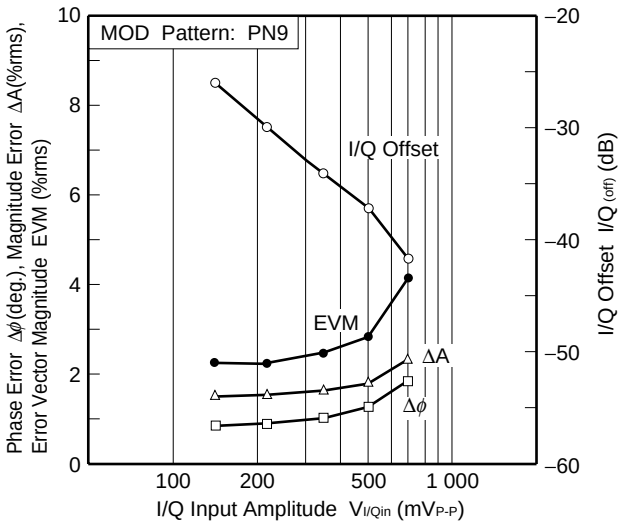


7.4 Error and Accuracy

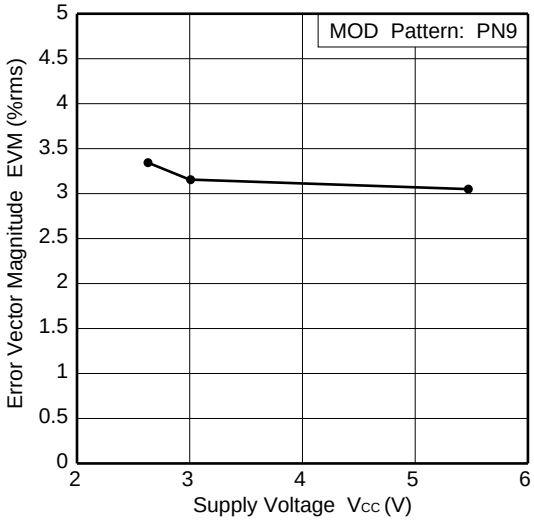
PHASE ERROR, MAGNITUDE ERROR, ERROR VECTOR MAGNITUDE, I/Q OFFSET vs. AGC CONTROL VOLTAGE



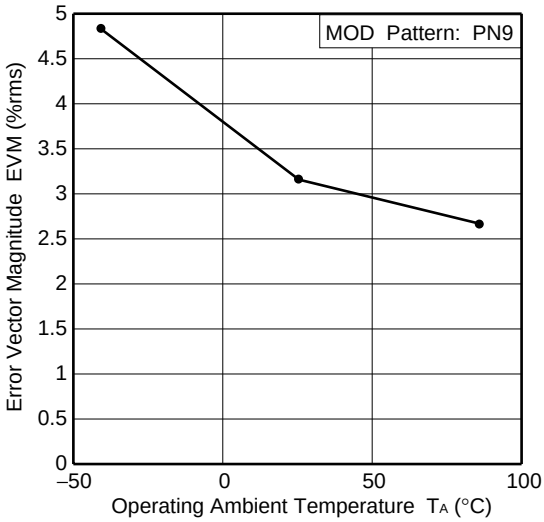
PHASE ERROR, MAGNITUDE ERROR, ERROR VECTOR MAGNITUDE, I/Q OFFSET vs. I/Q INPUT AMPLITUDE



ERROR VECTOR MAGNITUDE vs. SUPPLY VOLTAGE

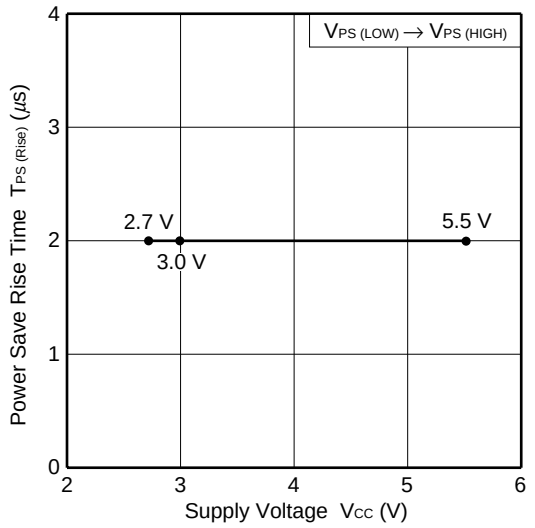


ERROR VECTOR MAGNITUDE vs. OPERATING AMBIENT TEMPERATURE

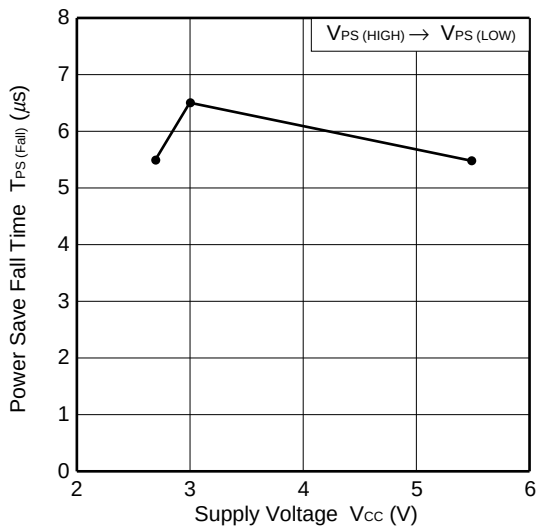


7.5 Power Save Response Time

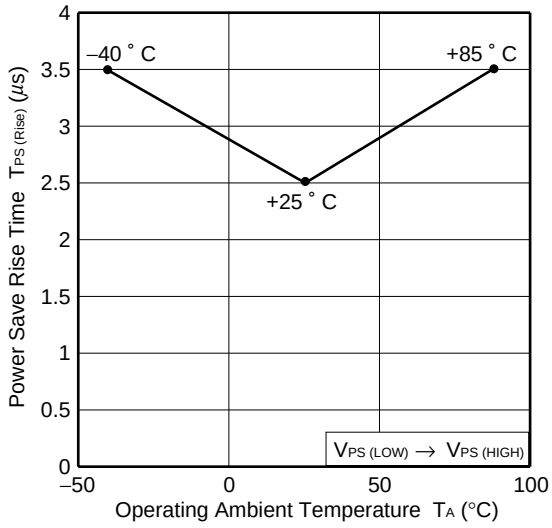
POWER SAVE RISE TIME vs. SUPPLY VOLTAGE



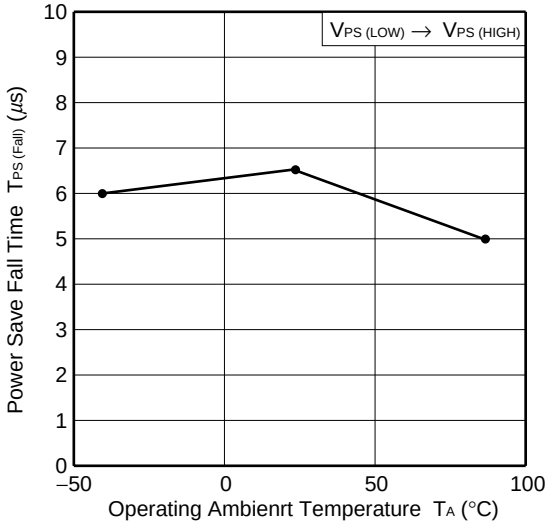
POWER SAVE FALL TIME vs. SUPPLY VOLTAGE



POWER SAVE RISE TIME vs.
OPERATING AMBIENT TEMPERATURE



POWER SAVE FALL TIME vs.
OPERATING AMBIENT TEMPERATURE



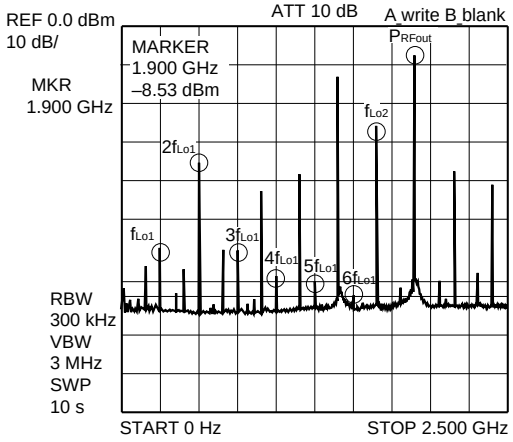
OUTPUT RESPONSE (1)
(V_{CC} = 2.7 V)

OUTPUT RESPONSE (2)
(V_{CC} = 3.0 V)

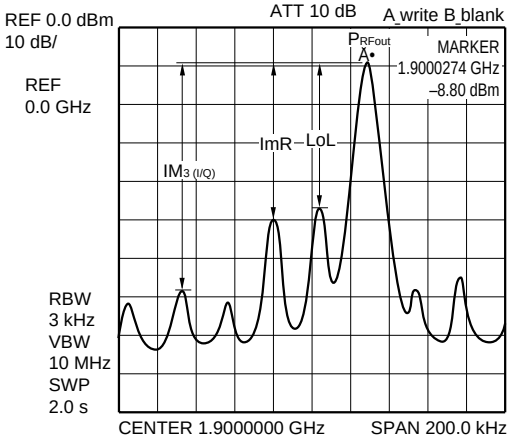
OUTPUT RESPONSE (3)
(V_{CC} = 5.5 V)

7.6 Spectrum

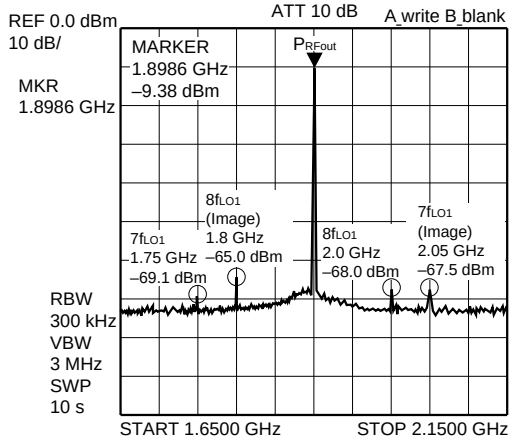
TYPICAL SINE WAVE MODULATION
OUTPUT SPECTRUM



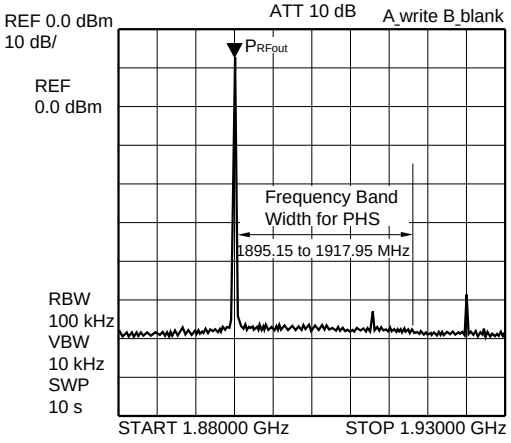
TYPICAL SINE WAVE MODULATION
OUTPUT SPECTRUM



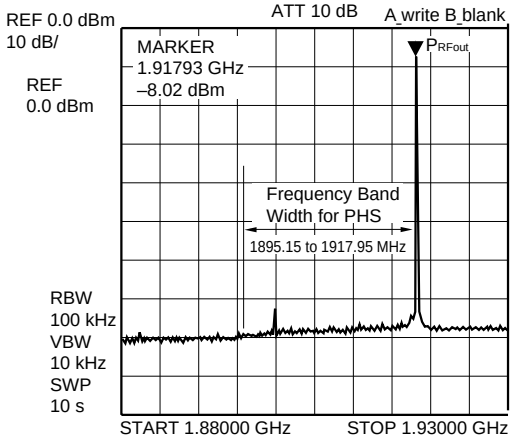
TYPICAL SINE WAVE MODULATION
OUTPUT SPECTRUM (IN BAND) (1)



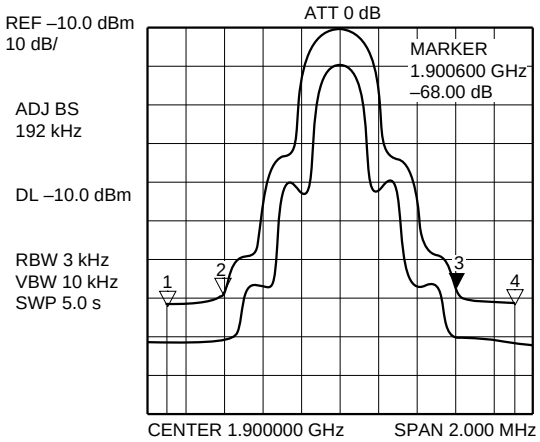
TYPICAL SINE WAVE MODULATION
OUTPUT SPECTRUM (IN BAND) (2)
(f_{LO1} = 233.15 MHz,f_{LO2} = 1662 MHz)



TYPICAL SINE WAVE MODULATION
OUTPUT SPECTRUM (IN BAND) (3)
(f_{LO1} = 233.15 MHz, f_{LO2} = 1684.8 MHz)



TYPICAL π/4 DQPSK MODULATION
OUTPUT SPECTRUM

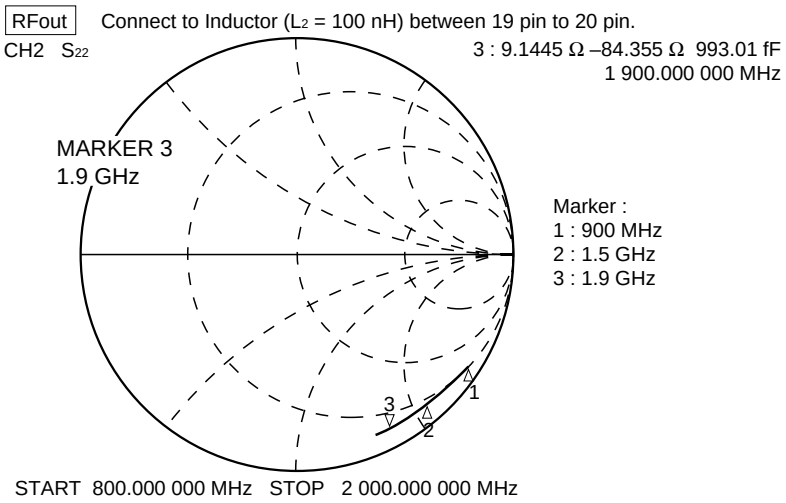


*** Multi Marker List ***
No.1 : 1.899100 GHz –71.00 dB
No.2 : 1.899400 GHz –68.00 dB
No.3 : 1.900600 GHz –68.00 dB
No.4 : 1.900900 GHz –71.25 dB

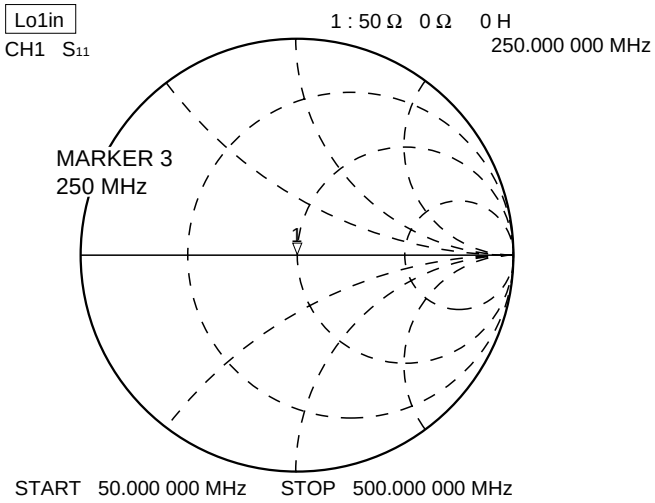
7.7 Input/output Impedance

RF OUTPUT (19 pin) IMPEDANCE

$V_{CC} = V_{PS}$ = 3.0 V

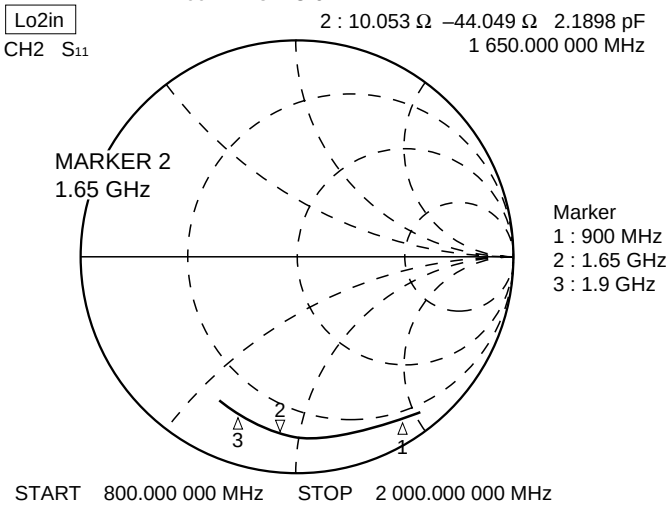


Lo1 INPUT (8 pin) IMPEDANCE $V_{CC} = V_{PS}$ = 3.0 V

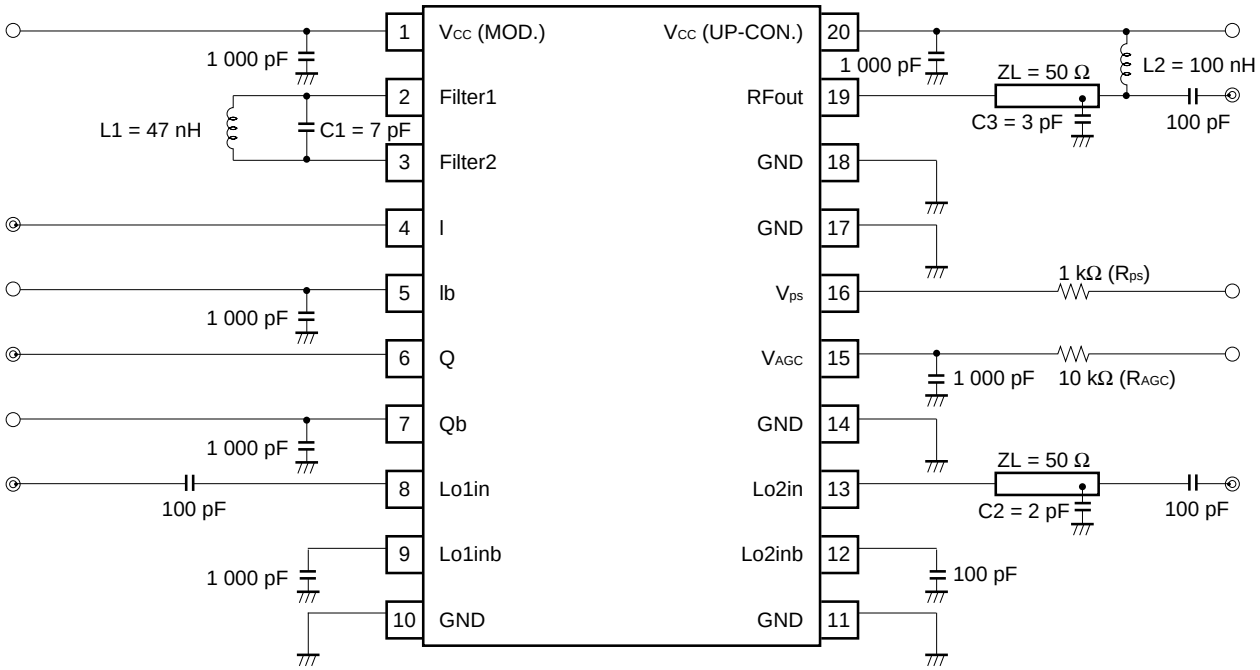


Lo2 INPUT (13 pin) IMPEDANCE

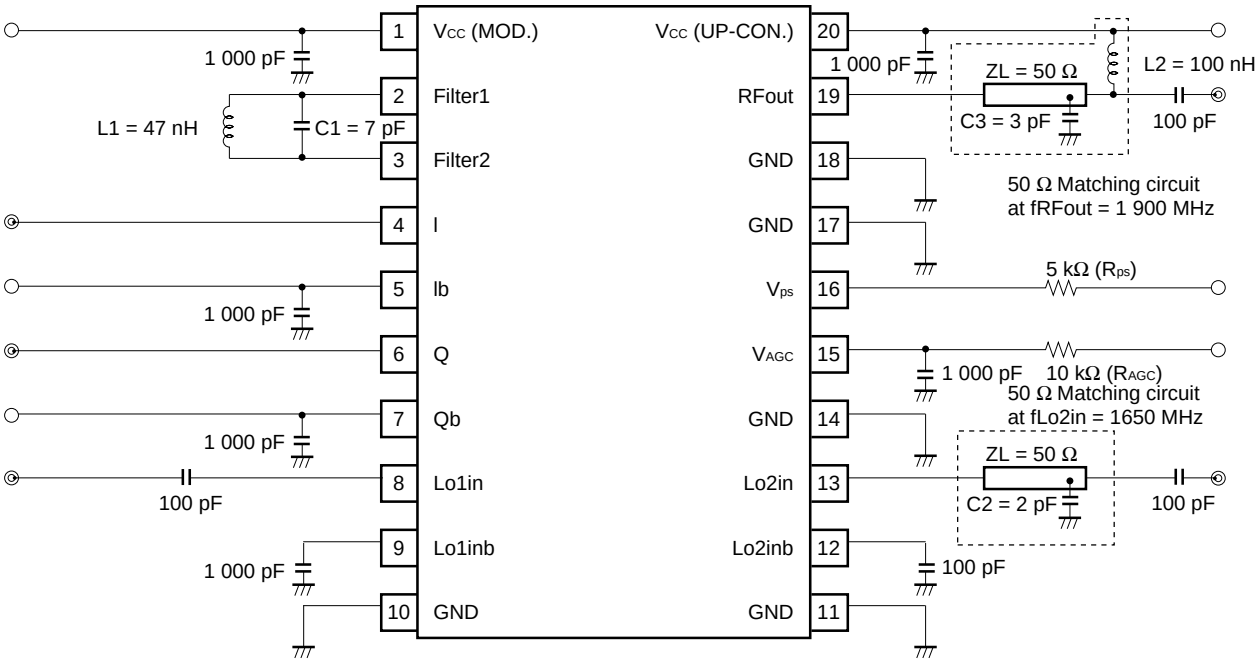
$V_{CC} = V_{PS}$ = 3.0 V



8. TEST CIRCUIT (SINGLE ENDED INPUT)

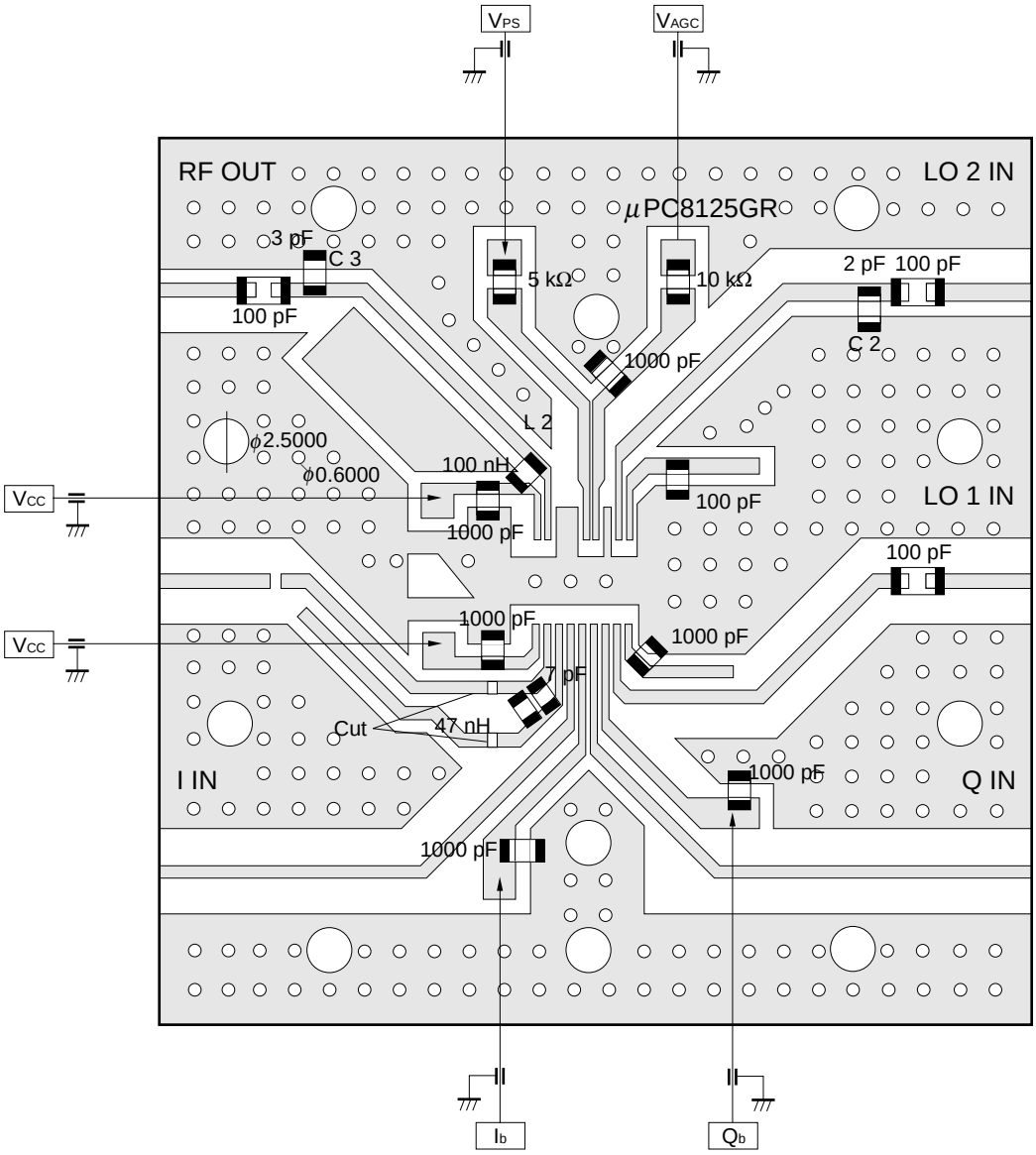


9. APPLICATION CIRCUIT EXAMPLE (IN THE CASE OF SINGLE ENDED INPUT)



Note For the details of application circuit and its explanations, please refer to application note '**Usage of μPC8101, 8104, 8105, 8125, 8129**' (Document No. **P13251E**).

10. ASSEMBLED TEST BOARD



Notes 1. Double-sided patterning with 35 μm thick copper on polyhimid board sizing 50 × 50 × 0.4 mm.

2. GND pattern on backside.

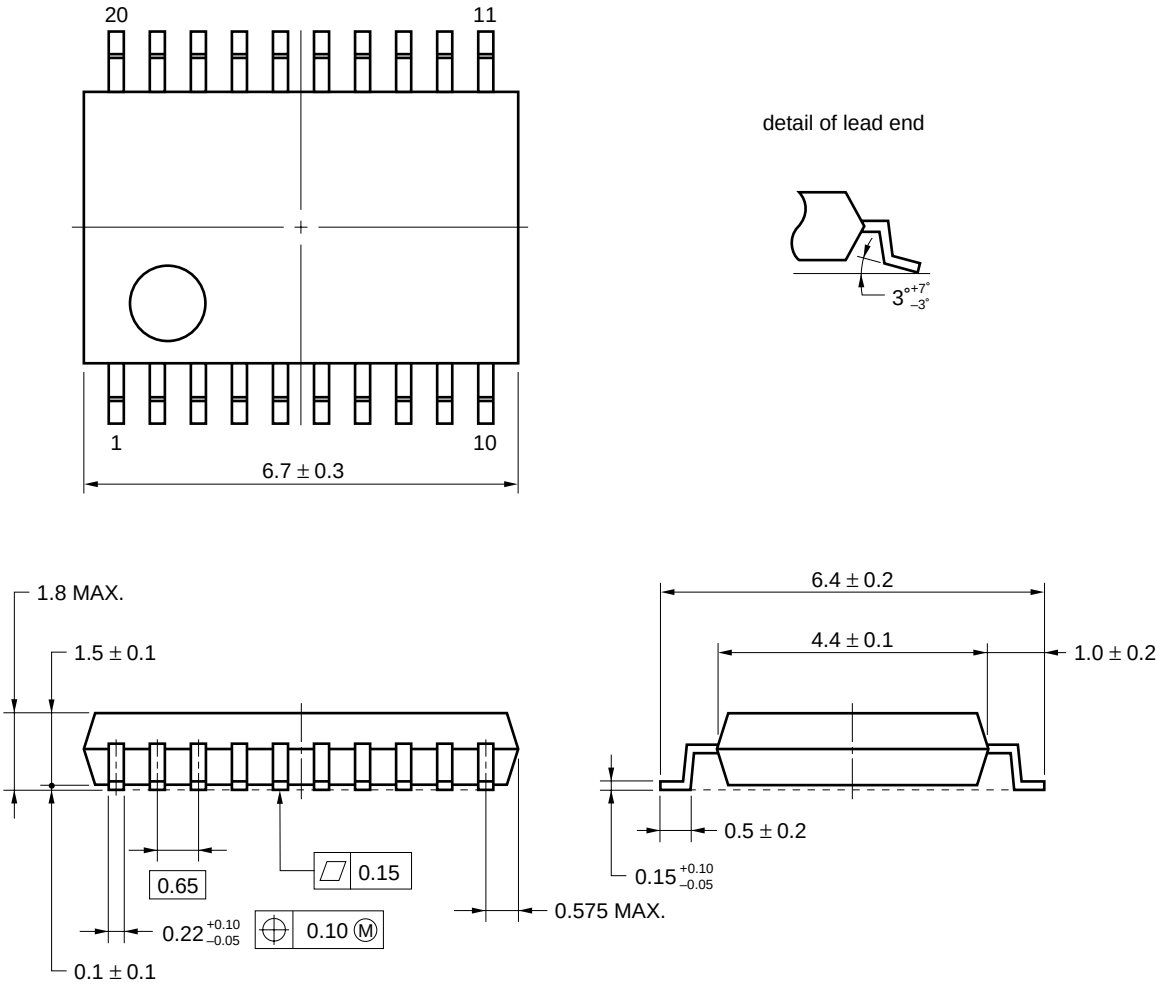
3. Solder coating over patterns.

4. ○, ○ indicate through-holes.

Remark The test circuits and board pattern on data sheet are for performance evaluation use only. (They are not recommended circuits.) In the case of actual design-in, matching circuit should be determined using S-parameter of desired frequency in accordance to actual mounting pattern.

★ 11. PACKAGE DIMENSIONS

20 PIN PLASTIC SSOP (225 mil) (UNIT: mm)



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

12. NOTE ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (example: 1 000 pF) to the V_{CC} pin.

13. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 2, Exposure limit: None[Note]	IR35-00-2
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 2, Exposure limit: None[Note]	VP15-00-2
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit: None[Note]	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit: None[Note]	–

Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]

[MEMO]

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