DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8129GR

UP CONVERTER WITH AGC FUNCTION + QUADRATURE MODULATOR IC FOR DIGITAL MOBILE COMMUNICATION SYSTEMS

DESCRIPTION

The μPC8129GR is a silicon monolithic integrated circuit designed as indirect quadrature modulator for digital mobile communication systems. This modulator consists of 0.8 GHz to 1.9 GHz up-converter and 100 MHz to 400 MHz quadrature modulator which are packaged in 20 pin SSOP. The device has power save function and can operate 2.7 to 5.5 V supply voltage, therefore, it can contribute to make RF block small, high performance and low power consumption.

FEATURES

- High linearity up converter is incorporated; P_{RFout} = –5 dBm TYP./@f_{RFout} = 900 MHz
- Wide operating frequency range. Up converter ; f_{RFout} = 800 MHz to 1900 MHz
  Modulator ; f_{LO1in} = 200 MHz to 800 MHz
  f_{MODout} = 100 MHz to 400 MHz, $f_{I/Q}$ = DC to 10 MHz
- External IF filter can be applied between modulator output and up converter input terminal.
- Low phase difference due to digital phase shifter is adopted.
- Supply voltage: V_{CC} = 2.7 to 5.5 V
- Equipped with power save function.
- 20 pin SSOP suitable for high density surface mounting.

APPLICATIONS

- Digital cellular phones (ex. GSM etc…)
- Digital cordless phones

ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPC8129GR-E1	20 pin plastic SSOP (225 mil)	Embossed tape 12 mm wide. QTY 2.5 kp/Reel. Pins 1 through 10 are in pull-out direction.

* To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: μPC8129GR)

Caution electro-static sensitive device

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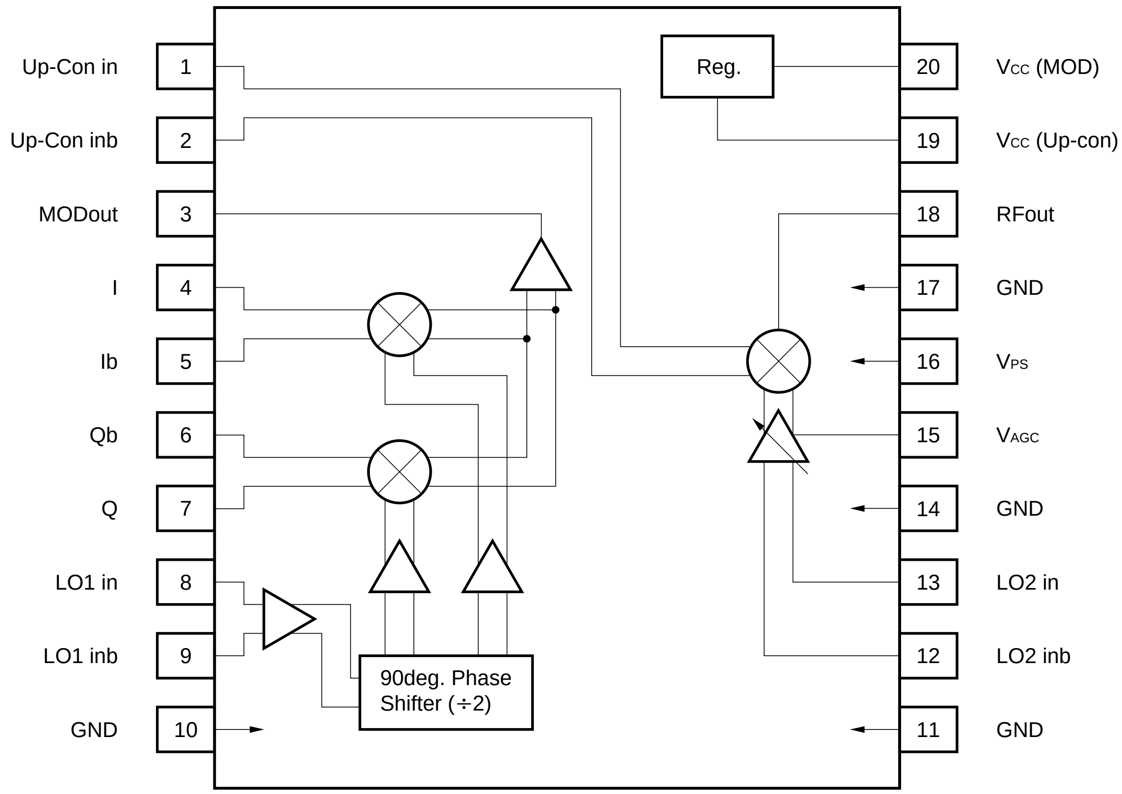
The mark ★ shows major revised points.

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS

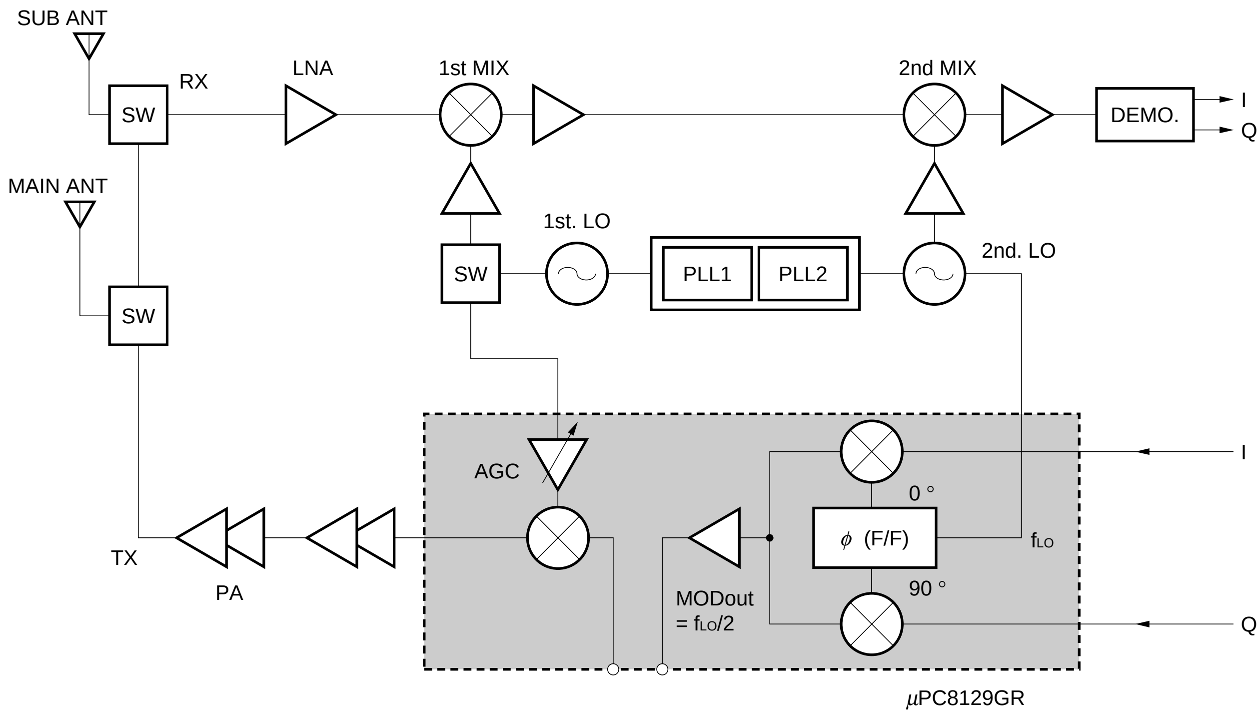


★ QUADRATURE MODULATOR SERIES PRODUCT

Part Number	Functions	I_{CC} (mA)	f_{LO1in} (MHz)	f_{MODout} (MHz)	RF Mixer f_{RFout} (MHz)	Phase Shifter	Package	Application
μPC8101GR	150 MHz Quad.Mod	15/@2.7 V	100 to 300	50 to 150	External	F/F	20-pin SSOP (225 mil)	CT-2 etc.
μPC8104GR	RF Up-Converter + IF Quad.Mod	28/@3.0 V	100 to 400		900 to 1 900	Doubler + F/F		Digital Comm.
μPC8105GR	400 MHz Quad.Mod	16/@3.0 V	100 to 400		External		16-pin SSOP (225 mil)	
μPC8110GR	1 GHz Direct Quad.Mod	24/@3.0 V	800 to 1 000		External		20-pin SSOP (225 mil)	PDC800 MHz, etc.
μPC8125GR	RF Up-Converter + IF Quad.Mod + AGC	36/@3.0 V	220 to 270		1 800 to 2 000			PHS
μPC8126GR	900 MHz Direct Quad.Mod with Offset-Mixer	35/@3.0 V	915 to 960		915 to 960			PDC800 MHz
μPC8126K			889 to 960		889 to 960		28-pin QFN	
μPC8129GR	×2LO IF Quad. Mod+RF Up-Converter	28/@3.0 V	200 to 800	100 to 400	800 to 1 900	F/F	20-pin SSOP (225 mil)	GSM, DCS1800, etc.
μPC8139GR-7JH	Transceiver IC (1.9 GHz Indirect Quad. Mod + RX-IF + IF VCO)	TX: 32.5 RX: 4.8 /@3.0 V	220 to 270		1 800 to 2 000	CR	30-pin TSSOP (225 mil)	PHS
μPC8158K	RF Up-Converter + IF Quad.Mod + AGC	28/@3.0 V	100 to 300		800 to 1 500		28-pin QFN	PDC800 M/1.5 G

APPLICATION EXAMPLE

[GSM]



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	CONDITION
Supply Voltage	V_{CC}	6.0	V	T_A = +25 °C
Power Save Voltage	V_{PS}	6.0	V	
AGC Control Voltage	V_{AGC}	6.0	V	
IQ DC Offset Voltage	IQ (DC)	4.0	V	
Power Dissipation	P_D	430	mW	T_A = +85 °C Note
Operating Ambient Temperature	T_A	–40 to +85	°C	
Storage Temperature	T_{stg}	–55 to +150	°C	

Note Mounted on double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{CC}	2.7	3.0	5.5	V	
Operating Ambient Temperature	T_A	–40	+25	+85	°C	
Up Converter RF Frequency	f_{RFout}	800		1900	MHz	
Up Converter Input Freq.	$f_{UPCONin}$	100		400	MHz	
Modulator Output Frequency	f_{MODout}					
LO1 Input Frequency	f_{LO1in}	200		800	MHz	
LO1 Input Level	P_{LO1in}	–15	–10	–5	dBm	
LO2 Input Frequency	f_{LO2in}	800		1800	MHz	
LO2 Input Level	P_{LO2in}	–15	–10	–5	dBm	
I/Q Input Frequency	$f_{I/Qin}$	DC		10	MHz	
I/Q Input Amplitude	$V_{I/Qin}$			600	mV_{P-P}	Single ended Input

ELECTRICAL CHARACTERISTICS (1)

Conditions (unless otherwise specified):

T_A = +25 °C, V_{CC} = 3 V, V_{PS} = 3 V, R_{PS} = 1 kΩ, V_{AGC} = 3 V, R_{AGC} = 10 kΩ

I/Q DC = 1.5 V (Vbias(I) = Vbias(Ib) = Vbias (Q) = Vbias (Qb) = 1.5 V)

$f_{I/Qin}$ = 67.7 kHz, $V_{I/Qin}$ = 500 mV_{P-P} (single ended input, Ib = Qb = 0 mV_{P-P})

Modulation Pattern: <0000>

f_{LO1in} = 500 MHz, P_{LO1in} = –10 dBm

f_{LO2in} = 1150 MHz, P_{LO2in} = –10 dBm

$f_{UPCONin}$ = f_{MODout} = f_{LO1in}/2 + $f_{I/Qin}$ = 250 MHz + $f_{I/Qin}$

f_{RFout} = 900 MHz – $f_{I/Qin}$

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
UP CONVERTER + QUADRATURE MODULATOR TOTAL						
Total Circuit Current	$I_{CC(TOTAL)}$	20	28	37	mA	No input signal
Total Circuit Current at Power Save Mode	$I_{CC(PS)TOTAL1}$		0.6	10	μA	V_{PS} ≤ 0.5 V
Total Output Power	P_{RFout}	–8	–5	–2	dBm	
Local Oscillator Carrier Leakage	LoL		–40	–26.5	dBc	f_{LoL} = f_{LO2} – f_{LO1}/2
Image Rejection (Side Band Leak)	ImR		–30	–26.5	dBc	
AGC Gain Control Rang	GCR	28	40		dB	V_{AGC} = 2.5 V to 0 V
Power Save Rise Time	T_{PS}(rise)		2.0	5.0	μs	V_{PS}(Low) → V_{PS}(High)
Power Save Fall Time	T_{PS}(fall)		2.0	5.0	μs	V_{PS}(High) → V_{PS}(Low)
UP CONVERTER BLOCK						
Circuit Current at Power Save Mode	$I_{CC(PS)}$ (Up con.)			5.0	μA	V_{PS} ≤ 0.5 V
QUADRATURE MODULATOR BLOCK						
Circuit Current at Power Save Mode	$I_{CC(PS)}$ (MOD)			5.0	μA	V_{PS} ≤ 0.5 V

STANDARD CHARACTERISTICS FOR REFERENCE (1)

Conditions (unless otherwise specified):

T_A = +25 °C, V_{CC} = 3 V, V_{PS} = 3 V, R_{PS} = 1 kΩ, V_{AGC} = 3 V, R_{AGC} = 10 kΩ

I/Q DC = 1.5 V (Vbias(I) = Vbias(Ib) = Vbias (Q) = Vbias (Qb) = 1.5 V)

$f_{I/Qin}$ = 67.7 kHz, $P_{I/Qin}$ = 500 mV_{P-P} (single ended input, Ib = Qb = 0 mV_{P-P})

Modulation Pattern: <0000>

f_{LO1in} = 500 MHz, P_{LO1in} = –10 dBm

f_{LO2in} = 1150 MHz, P_{LO2in} = –10 dBm

$f_{UPCONin}$ = f_{MODout} = f_{LO1in}/2 + $f_{I/Qin}$ = 250 MHz + $f_{I/Qin}$

f_{RFout} = 900 MHz – $f_{I/Qin}$

PARAMETER	SYMBOL	REFERENCE	UNIT	TEST CONDITIONS
UP CONVERTER + QUADRATURE MODULATOR TOTAL				
Total Circuit Current at Power-Save Mode	$I_{CC(PS)TOTAL2}$	60	μA	V_{PS} ≤ 0.5 V, V_{AGC} = 0 V
Phase Error	$\Delta\phi$	1.8	deg. (rms)	MOD Pattern: PN9
UP CONVERTER BLOCK				
UP Con. Circuit Current	$I_{CC(UpCon)}$	14	mA	No input signal
UP Con. Circuit Current at Power-Save Mode	$I_{CC(PS)UpCon}$	60	μA	V_{PS} ≤ 0.5 V, V_{AGC} = 0 V
Conversion Gain	CG	12	dB	$P_{UPCONin}$ = –20 dBm
Maximum Output Power	$P_{RF(sat)}$	–1.5	dBm	$P_{UPCONin}$ = –4 dBm
Output 3rd Order Intercept Point	OIP_3	+6	dBm	$f_{UPCONin}$ = 250.0 MHz/250.2 MHz
QUADRATURE MODULATOR BLOCK				
MOD. Circuit Current	$I_{CC(MOD)}$	14	mA	No input signal
Output Power	P_{MODout}	–16.5	dBm	
LO1 Carrier Leakage	LoL	–40	dBc	f_{LoL} = f_{LO1}/2
Image Rejection (Side Band Leak)	ImR	–30	dBc	
I/Q 3rd Order Intermodulation Distortion	$IM_{3I/Q}$	–50	dBc	
I/Q Input Impedance	$Z_{I/Q}$	200	kΩ	I to Ib, Q to Qb
IQ Bias Current	$I_{I/Q}$	5	μA	I, Ib, Q, Qb to GND (each)
LO1 Input VSWR	$VSWR_{(Lo1)}$	1.2 : 1	–	
Output Noise Floor		–133	dBc/Hz	Δf = ±20 MHz

STANDARD CHARACTERISTICS FOR REFERENCE (2)

Conditions (unless otherwise specified):

T_A = +25 °C, V_{CC} = 3 V, V_{PS} = 3 V, R_{PS} = 1 kΩ, V_{AGC} = 3 V, R_{AGC} = 10 kΩ

I/Q DC = 1.5 V (Vbias(I) = Vbias(Ib) = Vbias (Q) = Vbias (Qb) = 1.5 V)

$f_{I/Qin}$ = 67.7 kHz, $P_{I/Qin}$ = 500 mV_{P-P} (single ended input, Ib = Qb = 0 mV_{P-P})

Modulation Pattern: <0000>

f_{LO1in} = 500 MHz, P_{LO1in} = –10 dBm

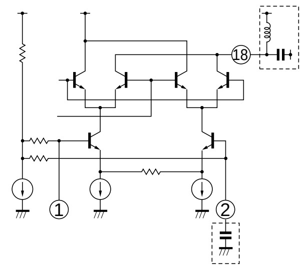
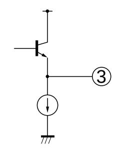
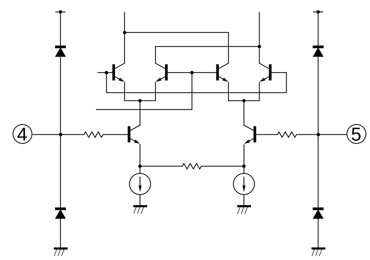
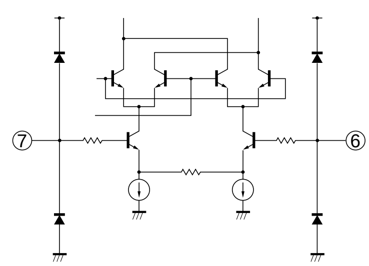
f_{LO2in} = 1650 MHz, P_{LO2in} = –10 dBm

$f_{UPCONin}$ = f_{MODout} = f_{LO1in}/2 + $f_{I/Qin}$ = 250 MHz + $f_{I/Qin}$

f_{RFout} = 1900 MHz + $f_{I/Qin}$

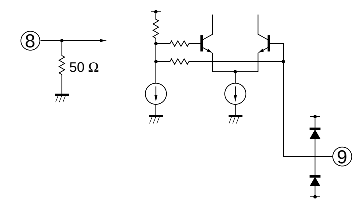
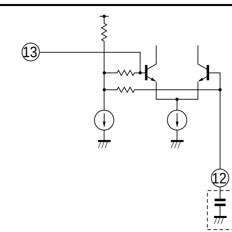
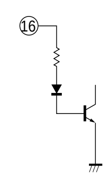
PARAMETER	SYMBOL	REFERENCE	UNIT	TEST CONDITIONS
UP CONVERTER + QUADRATURE MODULATOR TOTAL				
Total Output Power	P_{RFout}	–12	dBm	
Local Oscillator Carrier Leakage	LoL	–40	dBc	f_{LoL} = f_{LO2} + f_{LO1}/2
Image Rejection (Side Band Leak)	ImR	–30	dBc	
AGC Gain Control Rang	GCR	45	dB	V_{AGC} = 2.5 V to 0 V
Phase Error	$\Delta\phi$	1.8	deg. (rms)	MOD Pattern: PN9
UP CONVERTER BLOCK				
Conversion Gain	CG	5	dB	$P_{UPCONin}$ = –20 dBm
Maximum Output Power	$P_{RF(sat)}$	–7	dBm	$P_{UPCONin}$ = –4 dBm
Output Intercept Point	OIP_3	–1	dBm	$f_{UPCONin}$ = 250.0 MHz/250.2 MHz

PIN EXPLANATION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Supply Voltage (V)</th><th>Pin Voltage Typ. (V) @V_{CC} = 3 V</th><th>Description</th><th>Equivalent Circuit</th></tr>
<tr><td>18</td><td>RFout</td><td>V_{CC}</td><td>–</td><td>RF output from Up-Converter.
This pin is open collector output.</td><td rowspan="3"></td></tr>
<tr><td>1</td><td>UpCon in</td><td>–</td><td>2.2</td><td>IF input for Up-converter.
This pin is high impedance input.</td></tr>
<tr><td>2</td><td>UpCon inb</td><td>–</td><td>2.2</td><td>Bypass of IF input.
Grounded through external capacitor.</td></tr>
<tr><td>3</td><td>MODout</td><td>–</td><td>1.9</td><td>Output from modulator.
This is emitter follower output.</td><td></td></tr>
<tr><td>4</td><td>I</td><td>V_{CC}/2</td><td>–</td><td>Input for I signal. This input impedance is about 200 kΩ.
Relations between amplitude and V_{CC}/2 bias of input signal are following.
<table><tr><th>V_{CC}/2 (V)</th><th>Signal Level (mV_{P-P})</th></tr><tr><td>≥ 1.35</td><td>≤ 400</td></tr><tr><td>≥ 1.5</td><td>≤ 600</td></tr><tr><td>≥ 1.75</td><td>≤ 1000</td></tr></table> Note</td><td rowspan="2"></td></tr>
<tr><td>5</td><td>Ib</td><td>V_{CC}/2</td><td>–</td><td>Input for I signal. This input impedance is about 200 kΩ.
V_{CC}/2 biased DC signal should be input.</td></tr>
<tr><td>6</td><td>Qb</td><td>V_{CC}/2</td><td>–</td><td>Input for Q signal. This input impedance is about 200 kΩ
V_{CC}/2 biased DC signal should be input.</td><td rowspan="2"></td></tr>
<tr><td>7</td><td>Q</td><td>V_{CC}/2</td><td>–</td><td>Input for Q signal. This input impedance is about 200 kΩ.
Relations between amplitude and V_{CC}/2 bias of input signal are following.
<table><tr><th>V_{CC}/2 (V)</th><th>Signal Level (mV_{P-P})</th></tr><tr><td>≥ 1.35</td><td>≤ 400</td></tr><tr><td>≥ 1.5</td><td>≤ 600</td></tr><tr><td>≥ 1.75</td><td>≤ 1000</td></tr></table> Note</td></tr>
</table>

Note In the case of that I/Q input signals are single ended.
Of course, I/Q signal inputs can be used either single endedly or differentially with proper terminations.

PIN EXPLANATION

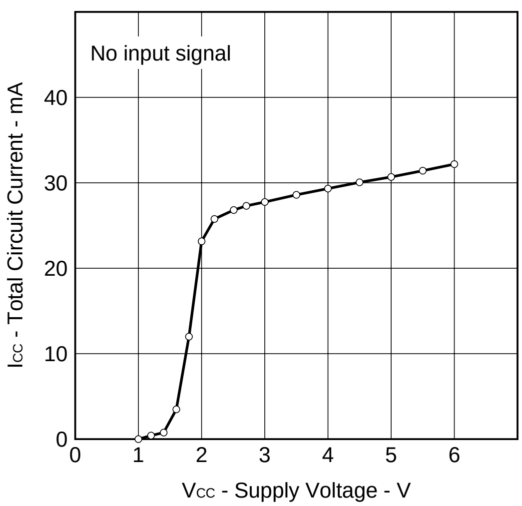
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Supply Voltage (V)</th><th>Pin Voltage Typ. (V) @V_{CC} = 3 V</th><th>Description</th><th>Equivalent Circuit</th></tr>
<tr><td>8</td><td>LO1in</td><td>–</td><td>0</td><td>Lo1 input for phase shifter.
This input impedance is 50 Ω matched internally.</td><td rowspan="2">
</td></tr>
<tr><td>9</td><td>LO1in b</td><td>–</td><td>2.3</td><td>Bypass of Lo1 input.
This pin is grounded through internal capacitor.</td></tr>
<tr><td>10
11</td><td>GND for Modulator</td><td>0</td><td>–</td><td>Connect to the ground with minimum inductance.
Track length should be kept as short as possible.</td><td>———</td></tr>
<tr><td>12</td><td>LO2in b</td><td>–</td><td>1.9</td><td>Bypass of Lo2 input.
Grounded through external capacitor.</td><td rowspan="2">
</td></tr>
<tr><td>13</td><td>LO2in</td><td>–</td><td>1.9</td><td>Lo2 input of Up-converter.
This pin is high impedance input.</td></tr>
<tr><td>14
17</td><td>GND for Up-con.</td><td>0</td><td>–</td><td>Connect to the ground with minimum inductance.
Track length should be kept as short as possible.</td><td>———</td></tr>
<tr><td>15</td><td>V_{AGC}</td><td>0 to V_{CC}</td><td>–</td><td>Input for AGC amplifier.
Total Output Power can be controlled by changing input voltage.
And as external series resistance (R_{AGC}) connecting, a slope of AGC curve can be changed by the resistance (R_{AGC}).</td><td>———</td></tr>
<tr><td>16</td><td>Power Save</td><td>0 to V_{CC}</td><td>–</td><td>Power save control pin can be controlled ON/OFF state with bias as follows;
<table><tr><th>V_{PS} (V)</th><th>STATE</th></tr><tr><td>2 to V_{CC}</td><td>ON (Active Mode)</td></tr><tr><td>0 to 0.5</td><td>OFF (Sleep Mode)</td></tr></table></td><td>
</td></tr>
<tr><td>19</td><td>V_{CC} for Up-converter</td><td>2.7 to 5.5</td><td>–</td><td>Supply voltage pin for Up-converter.</td><td>———</td></tr>
<tr><td>20</td><td>V_{CC} for Modulator</td><td>2.7 to 5.5</td><td>–</td><td>Supply voltage pin for modulator.
Internal regulator can be kept stable condition of supply bias against the variable temperature or V_{CC}.</td><td>———</td></tr>
</table>

: Externally

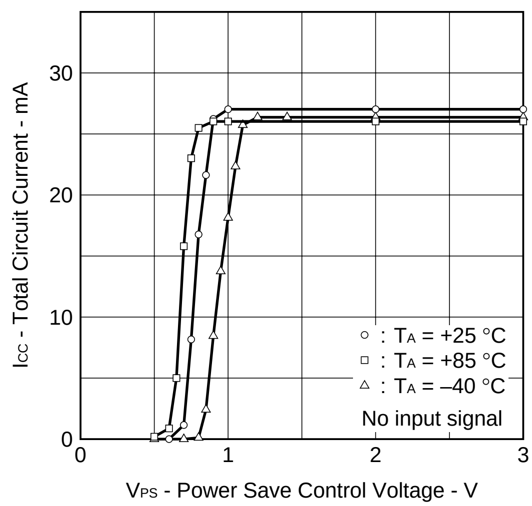
STANDARD TYPICAL CHARACTERISTICS <Modulator + Up-Converter Total at 900 MHz>

Test Circuit 1, T_A = +25 °C, V_{CC} = 3 V, V_{PS} = 3 V, R_{PS} = 1 kΩ, V_{AGC} = 3 V, R_{AGC} = 10 kΩ
I/Q DC = 1.5 V (Vbias(I) = Vbias(Ib) = Vbias(Q) = Vbias(Qb) = 1.5 V)
$f_{I/Qin}$ = 67.7 kHz, $V_{I/Qin}$ = 500 mV_{P-P} (single ended input, Ib = Qb = 0 mV_{P-P})
Modulation Pattern: All Zero <0000>, f_{LO1in} = 500 MHz, P_{LO1in} = –10 dBm
f_{LO2in} = 1150 MHz, P_{LO2in} = –10 dBm, $f_{UPCONin}$ = f_{MODout} = f_{LO1in}/2 + $f_{I/Qin}$ = 250 MHz + $f_{I/Qin}$
f_{RFout} = 900 MHz – $f_{I/Qin}$, Unless Otherwise Specified

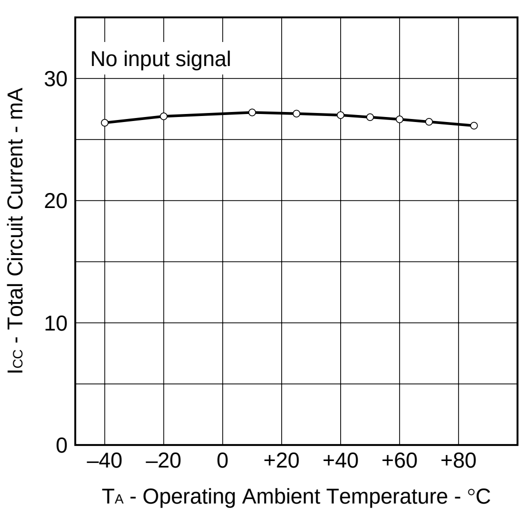
I_{CC} (TOTAL) vs V_{CC}



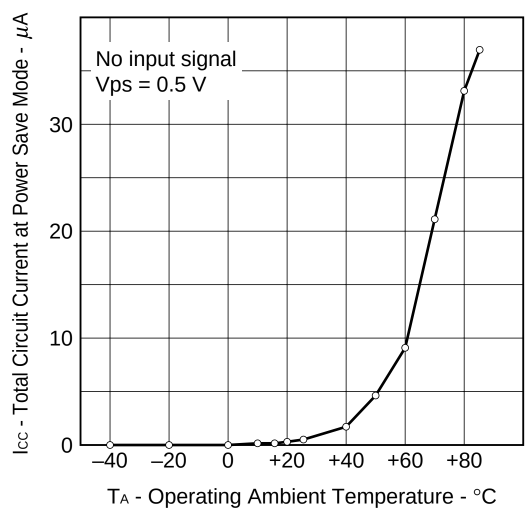
I_{CC} (TOTAL) vs V_{PS}



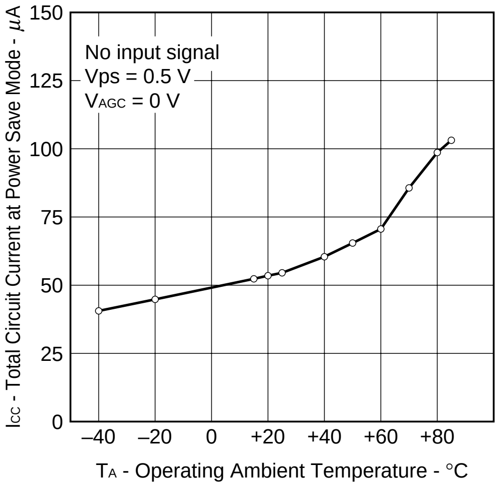
I_{CC} (TOTAL) vs T_A



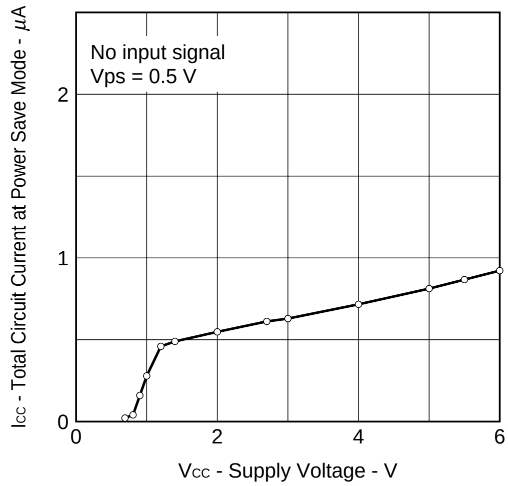
I_{CC} (PS) TOTAL vs T_A



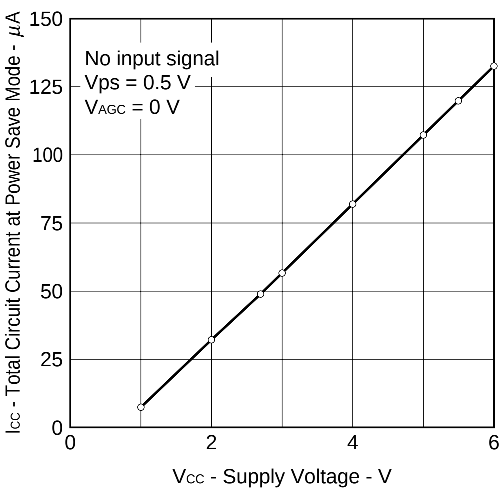
ICC (PS) TOTAL2 vs TA



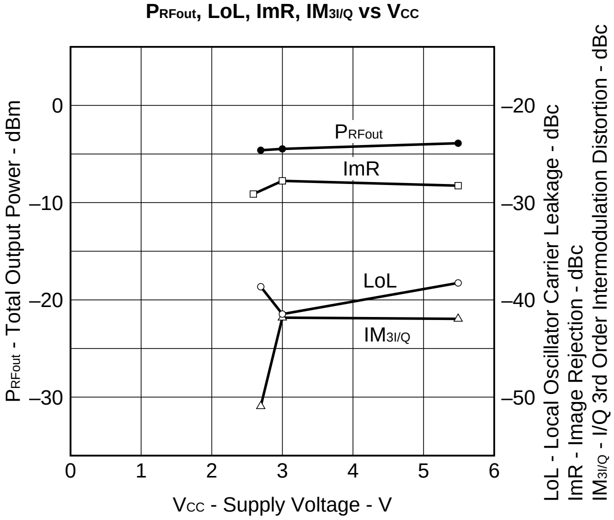
ICC (PS) TOTAL1 vs VCC



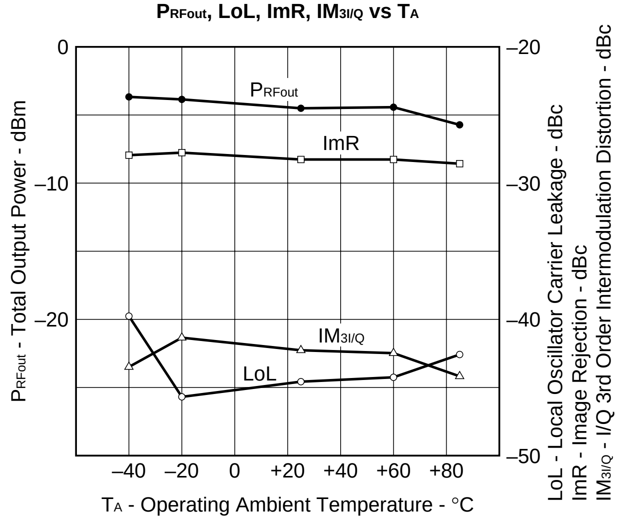
ICC (PS) TOTAL2 vs VCC



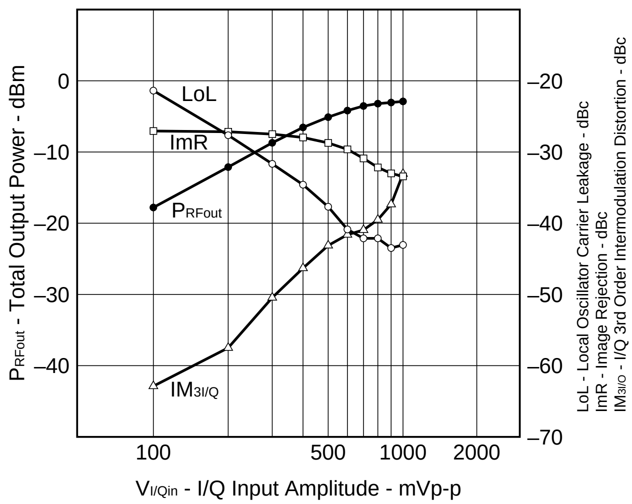
PRFout, LoL, ImR, IM3I/Q vs VCC



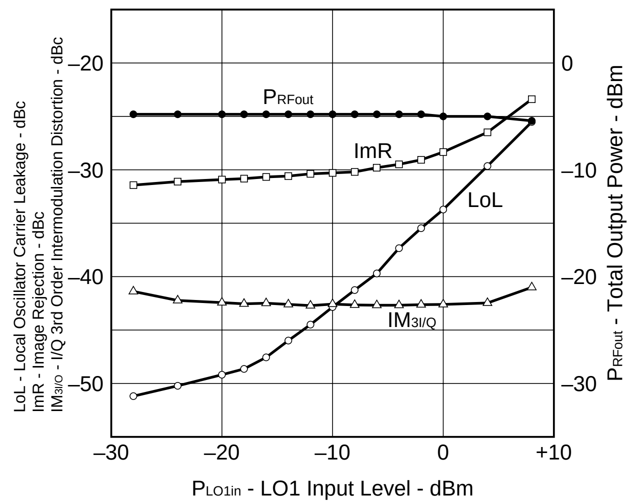
PRFout, LoL, ImR, IM3I/Q vs TA



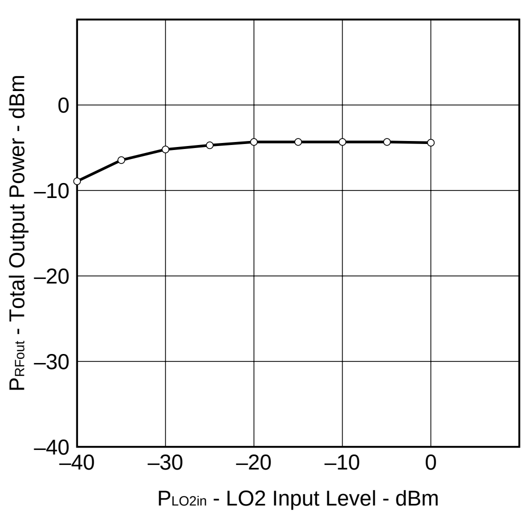
P_{RFout}, LoL, ImR, $IM_{3I/Q}$ vs $V_{I/Qin}$



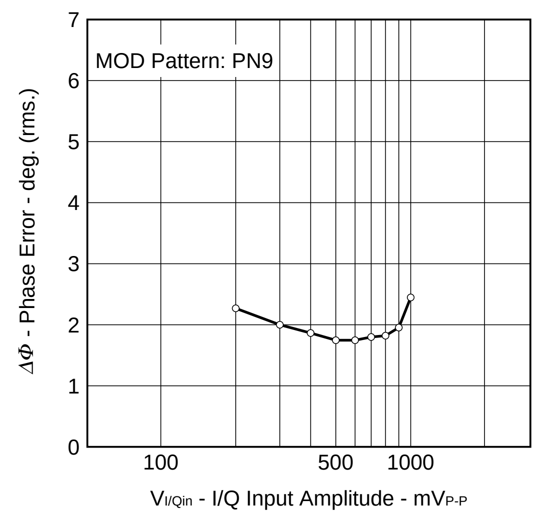
P_{RFout}, LoL, ImR, $IM_{3I/Q}$ vs P_{LO1in}



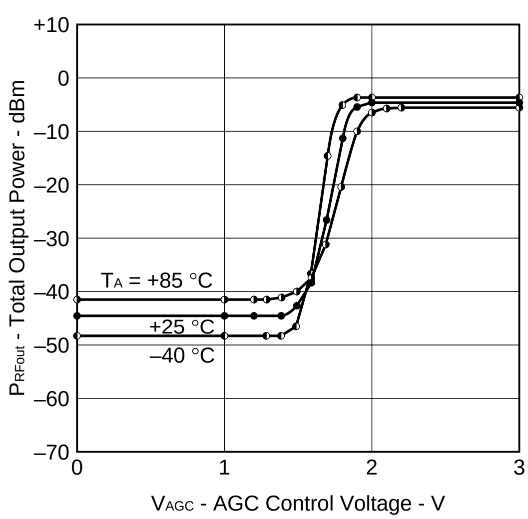
P_{RFout} vs P_{LO2in}



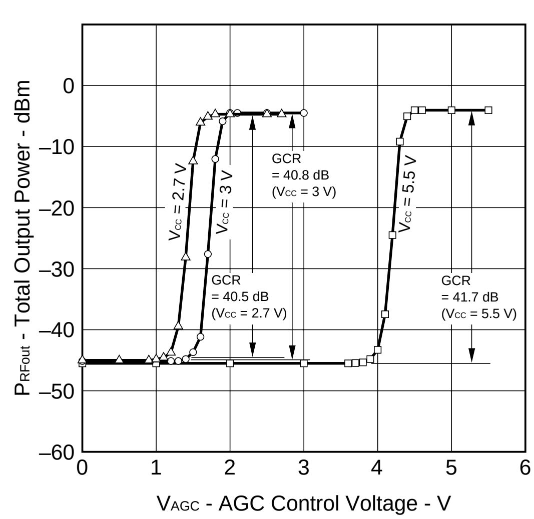
$\Delta\Phi$ vs $V_{I/Qin}$



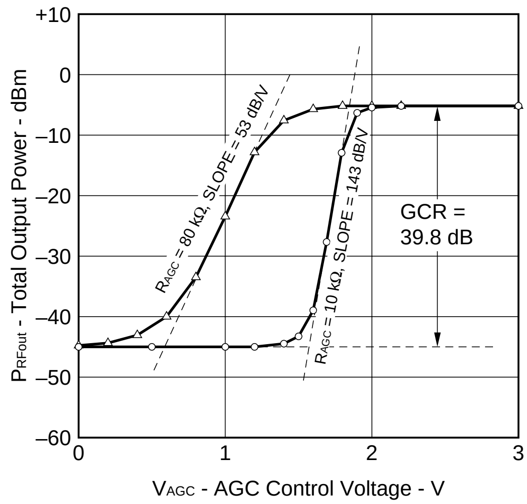
P_{RFout} vs V_{AGC}



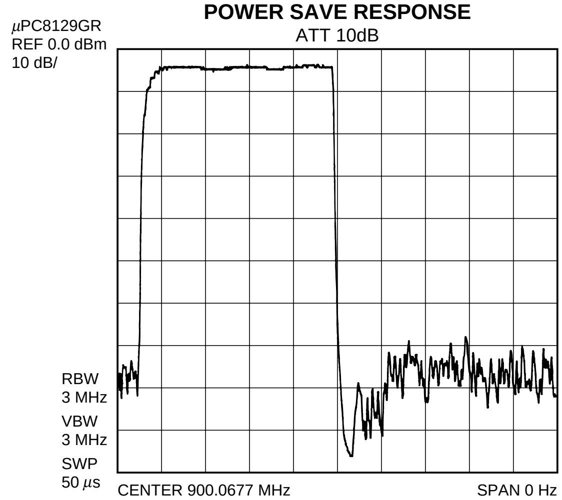
P_{RFout} vs V_{AGC}



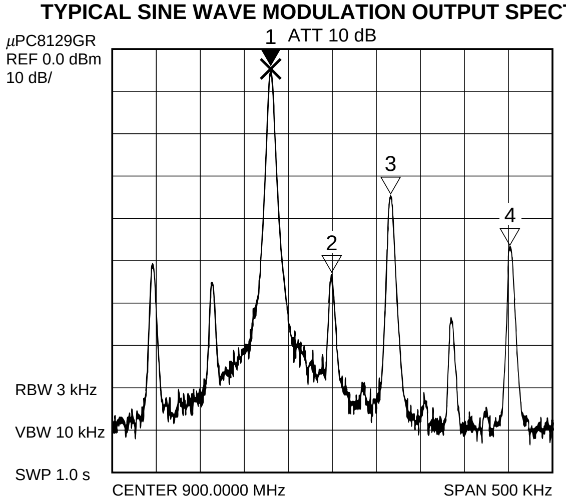
P_{RFout} VS V_{AGC}



POWER SAVE RESPONSE



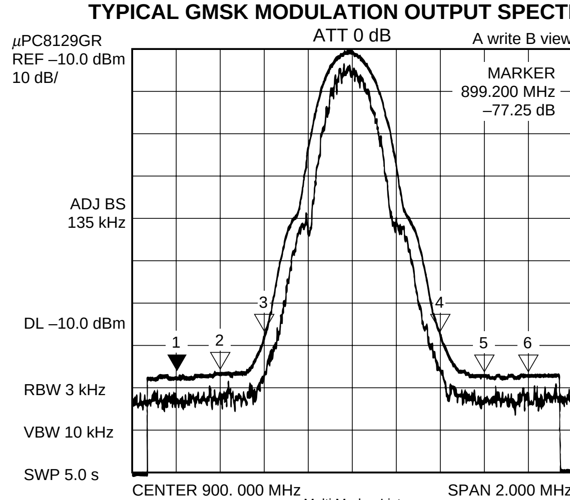
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



*** Multi Marker List ***

No.1:	899.9323 MHz	–4.80 dBm
No.2:	900.0000 MHz	–48.02 dBc
No.3:	900.0677 MHz	–29.88 dBc
No.4:	900.2031 MHz	–42.41 dBc

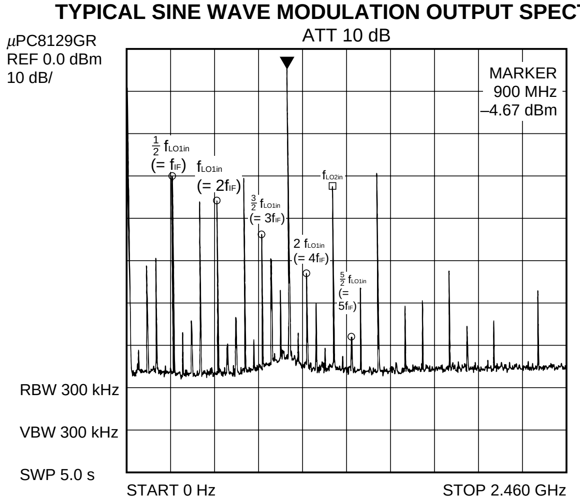
TYPICAL GMSK MODULATION OUTPUT SPECTRUM



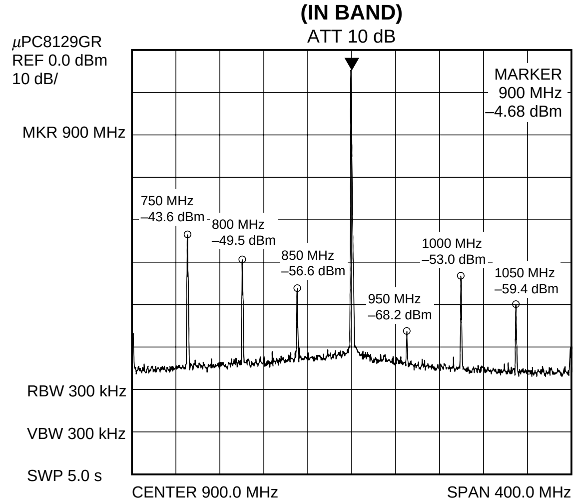
*** Multi Marker List ***

No.1:	899.200 MHz	–77.25 dB
No.2:	899.400 MHz	–76.50 dB
No.3:	899.600 MHz	–68.00 dB
No.4:	900.400 MHz	–68.25 dB
No.5:	900.600 MHz	–77.50 dB
No.6:	900.800 MHz	–77.50 dB
Δ:		

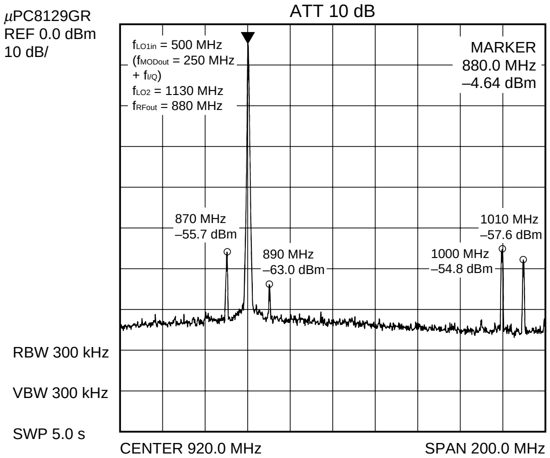
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



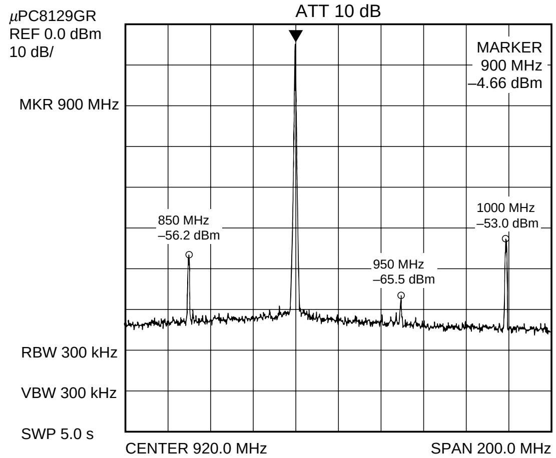
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND)



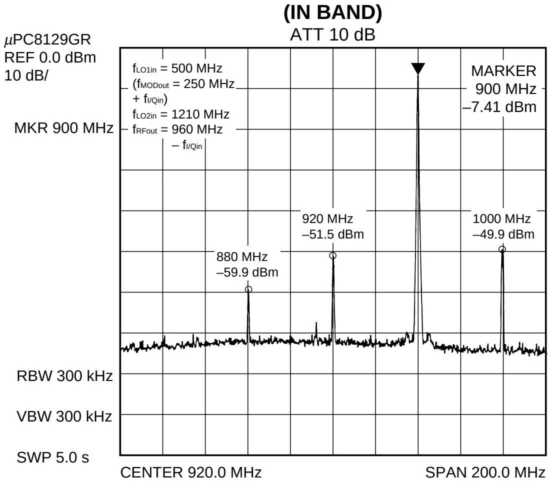
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND)



TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND)



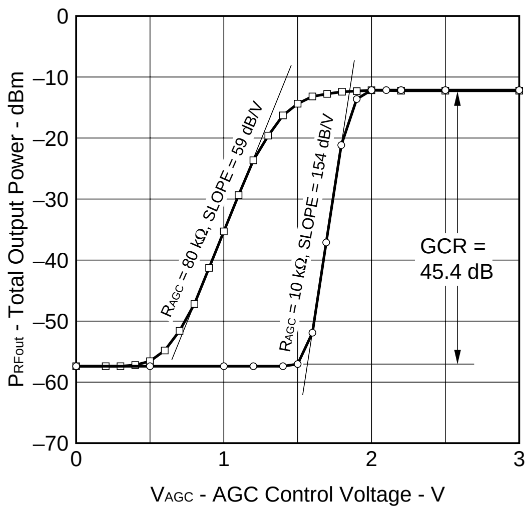
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND)



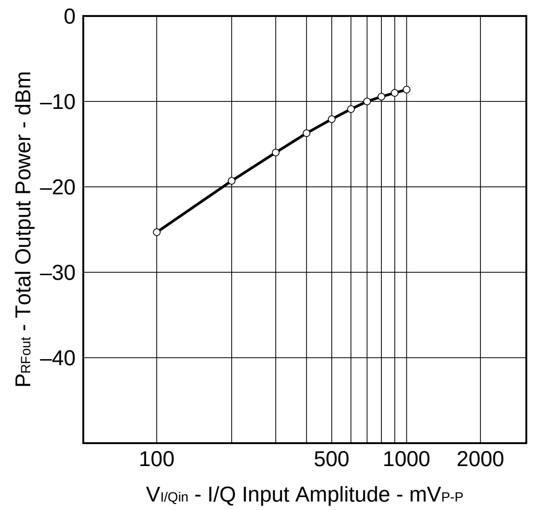
STANDARD TYPICAL CHARACTERISTICS <Modulator + Up-Converter Total at 1900 MHz>

Test Circuit 2, T_A = +25 °C, V_{CC} = 3 V, V_{PS} = 3 V, R_{PS} = 1 kΩ, V_{AGC} = 3 V, R_{AGC} = 10 kΩ
I/Q DC = 1.5 V (Vbias(I) = Vbias(Ib) = Vbias(Q) = Vbias(Qb) = 1.5 V)
$f_{I/Qin}$ = 67.7 kHz, $V_{I/Qin}$ = 500 mV_{P-P} (single ended input, Ib = Qb = 0 mV_{P-P})
Modulation Pattern: All Zero <0000>, f_{LO1in} = 500 MHz, P_{LO1in} = –10 dBm
f_{LO2in} = 500 MHz, P_{LO2in} = –10 dBm, $f_{UPCONin}$ = f_{MODout} = f_{LO1in}/2 + $f_{I/Qin}$ = 250 MHz + $f_{I/Qin}$
f_{RFout} = 1900 MHz + $f_{I/Qin}$, Unless Otherwise Specified

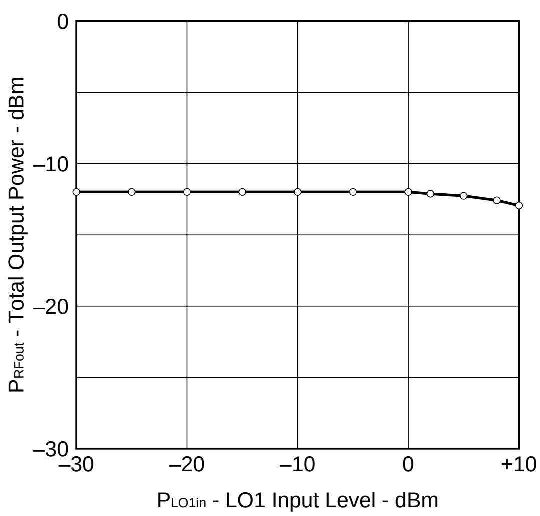
P_{RFout} vs V_{AGC}



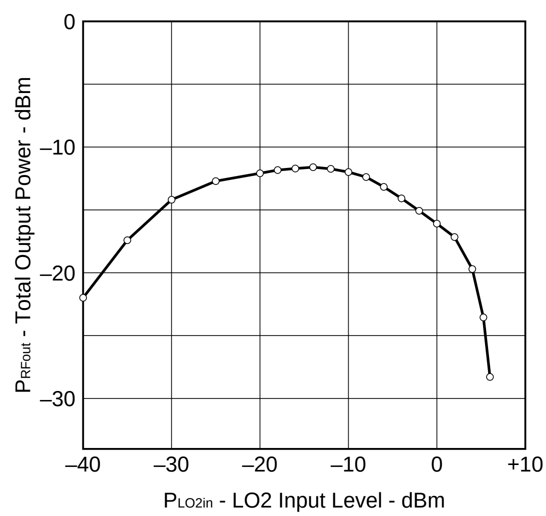
P_{RFout} vs $V_{I/Qin}$



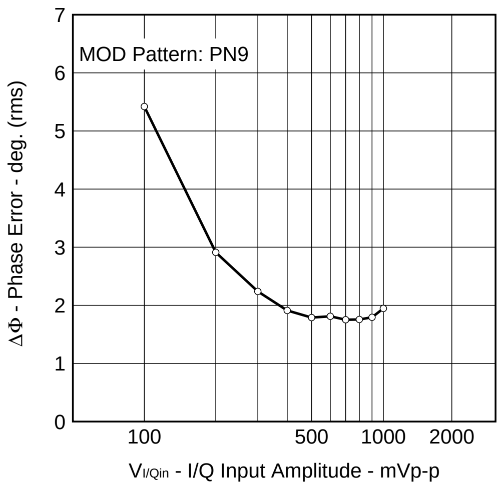
P_{RFout} vs P_{LO1in}



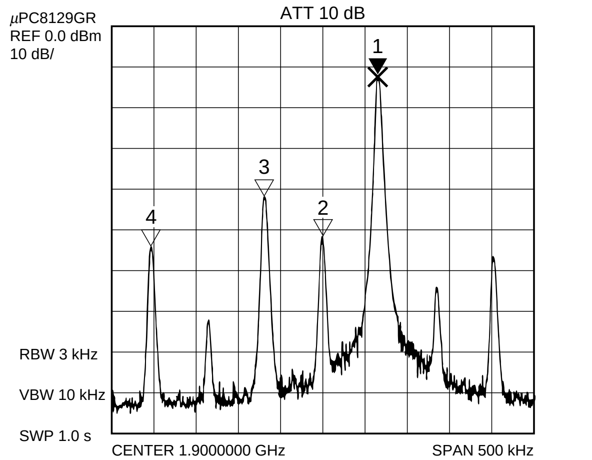
P_{RFout} vs P_{LO2in}



$\Delta\Phi$ vs $V_{I/Qin}$



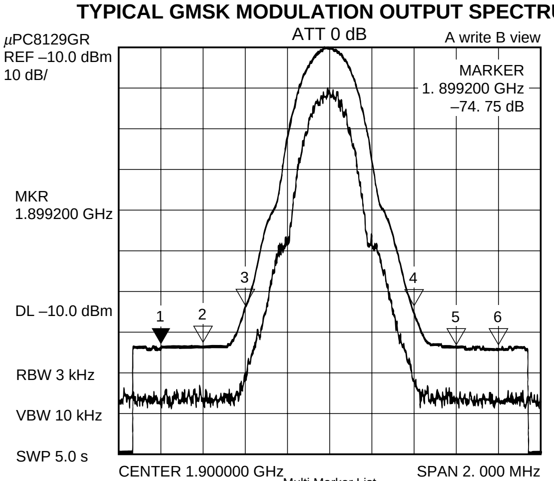
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



*** Multi Marker List ***

No.1:	1.9000677 GHz	–12.13 dBm
No.2:	1.9000000 GHz	–39.30 dBc
No.3:	1.8999323 GHz	–28.98 dBc
No.4:	1.8997969 GHz	–41.30 dBc

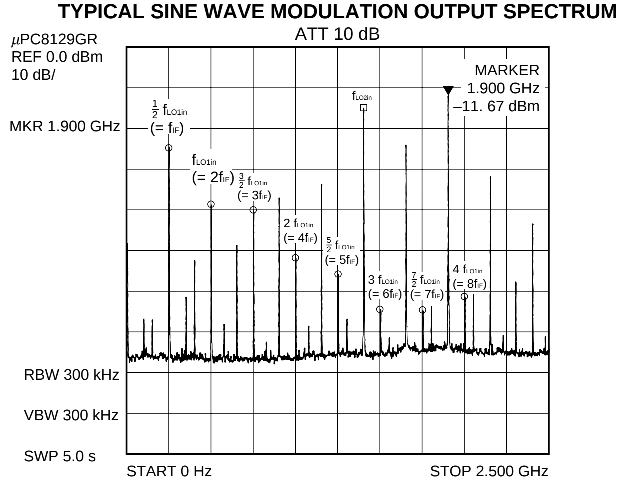
TYPICAL GMSK MODULATION OUTPUT SPECTRUM



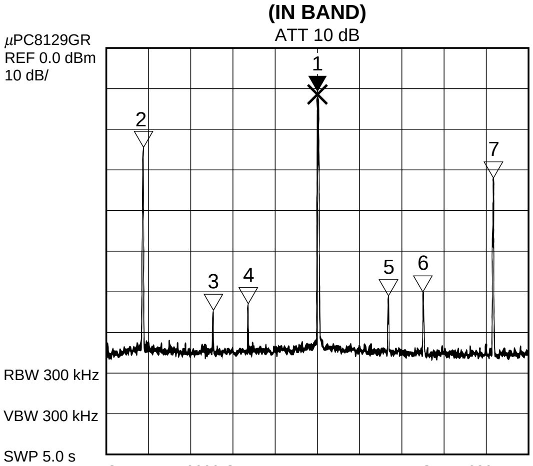
*** Multi Marker List ***

No.1:	1.899200 GHz	–74.75 dB
No.2:	1.899400 GHz	–74.50 dB
No.3:	1.899600 GHz	–64.75 dB
No.4:	1.900400 GHz	–66.50 dB
No.5:	1.900600 GHz	–74.25 dB
No.6:	1.900800 GHz	–74.75 dB
Δ:		

TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



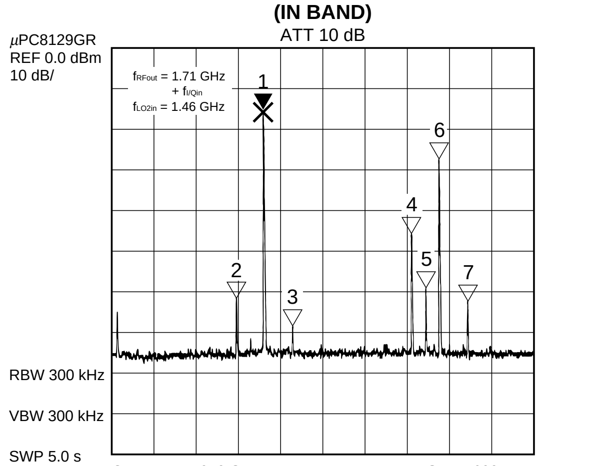
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND)



*** Multi Marker List ***

No.1:	1.900 GHz	–11.71 dBm
No.2:	1.650 GHz	–24.07 dBm
No.3:	1.750 GHz	–64.52 dBm
No.4:	1.800 GHz	–63.37 dBm
No.5:	2.000 GHz	–61.09 dBm
No.6:	2.050 GHz	–59.39 dBm
No.7:	2.150 GHz	–31.62 dBm

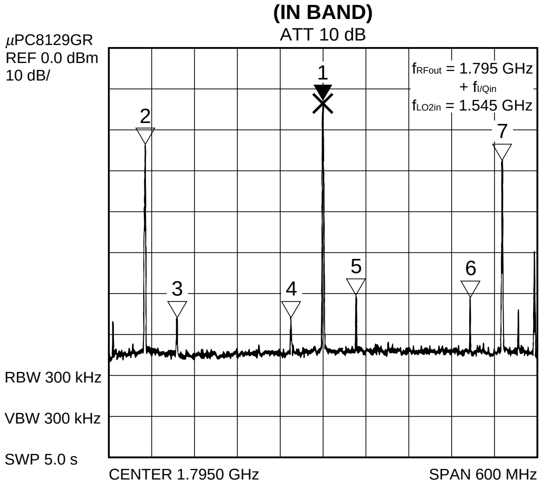
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND)



*** Multi Marker List ***

No.1:	1.710 GHz	–15.16 dBm
No.2:	1.670 GHz	–61.50 dBm
No.3:	1.750 GHz	–67.84 dBm
No.4:	1.920 GHz	–46.33 dBm
No.5:	1.940 GHz	–58.68 dBm
No.6:	1.960 GHz	–27.94 dBm
No.7:	2.000 GHz	–62.11 dBm

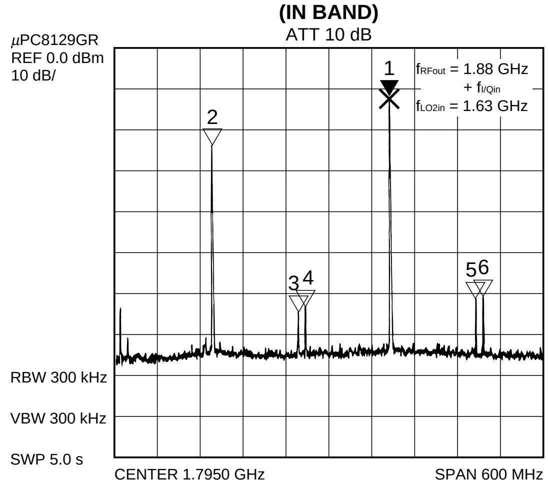
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND)



*** Multi Marker List ***

No.1:	1.795 GHz	–14.21 dBm
No.2:	1.545 GHz	–24.47 dBm
No.3:	1.590 GHz	–65.96 dBm
No.4:	1.750 GHz	–66.40 dBm
No.5:	1.840 GHz	–60.91 dBm
No.6:	2.000 GHz	–61.79 dBm
No.7:	2.045 GHz	–28.73 dBm

TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM (IN BAND)

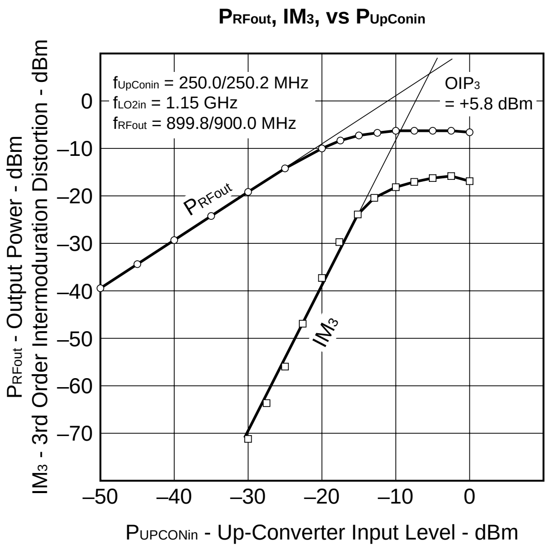


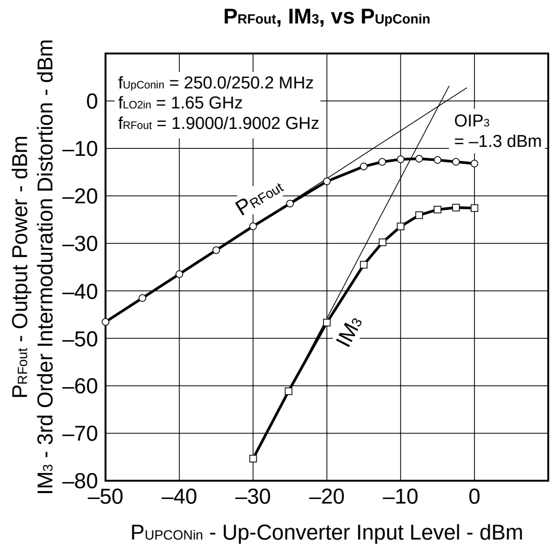
*** Multi Marker List ***

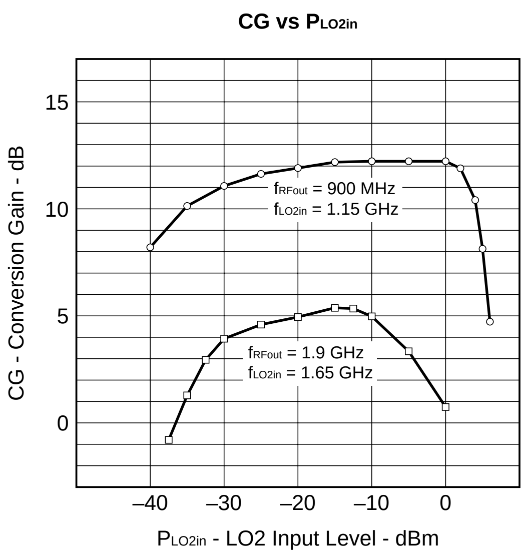
No.1:	1.880 GHz	–12.32 dBm
No.2:	1.630 GHz	–23.47 dBm
No.3:	1.750 GHz	–64.08 dBm
No.4:	1.760 GHz	–63.19 dBm
No.5:	2.000 GHz	–61.05 dBm
No.6:	2.010 GHz	–60.25 dBm

STANDARD TYPICAL CHARACTERISTICS <Up-Converter Block>

T_A = +25 °C, V_{CC} = 3.0 V, V_{PS} = 3.0 V, $f_{UPCONin}$ = 250 MHz, $P_{UPCONin}$ = –20 dBm
Test Circuit 1 (f_{RFout} = 900 MHz, f_{LO2in} = 1150 MHz) or
Test Circuit 2 (f_{RFout} = 1900 MHz, f_{LO2in} = 1650 MHz), Unless Otherwise Specified



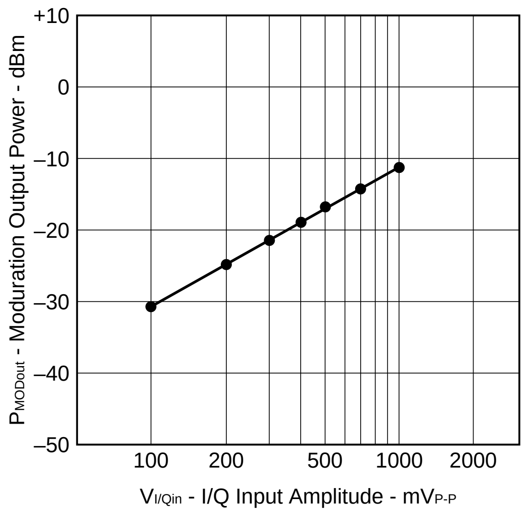




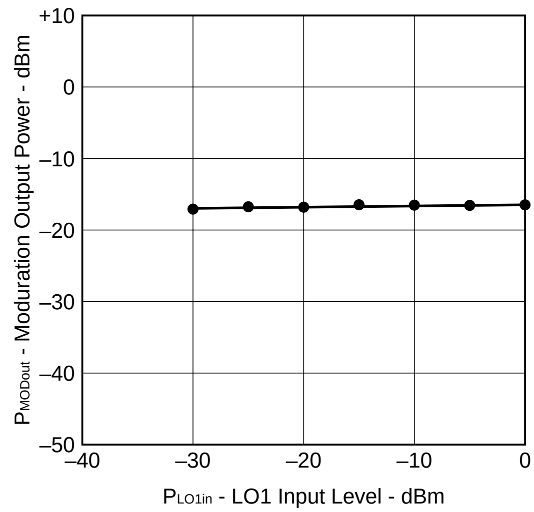
STANDARD TYPICAL CHARACTERISTICS <Modulator Block>

Test Circuit 1 or 2, T_A = +25 °C, V_{CC} = 3 V, V_{PS} = 3 V
I/Q DC = 1.5 V (Vbias(I) = Vbias(Ib) = Vbias(Q) = Vbias(Qb) = 1.5 V)
$f_{I/Qin}$ = 67.7 kHz, $V_{I/Qin}$ = 500 mV_{P-P} (single ended input, Ib = Qb = 0 mV_{P-P})
Modulation Pattern: All Zero <0000>, f_{LO1in} = 500 MHz, P_{LO1in} = –10 dBm
f_{MODout} = f_{LO1in}/2 + $f_{I/Qin}$ = 250 MHz + $f_{I/Qin}$, Unless Otherwise Specified

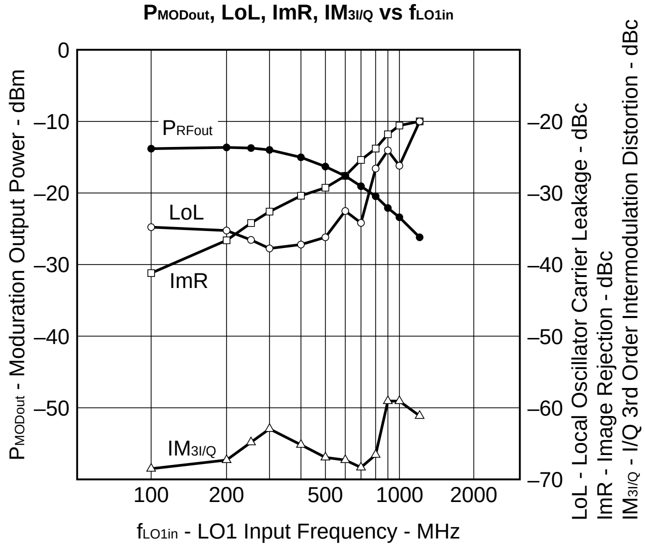
P_{MODout} vs $V_{I/Qin}$



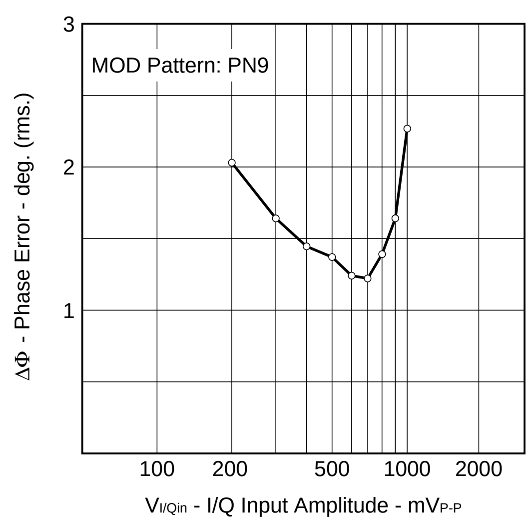
P_{MODout} vs P_{LO1in}

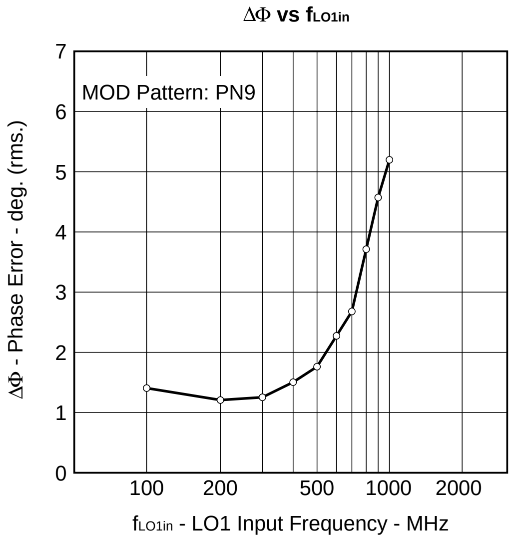


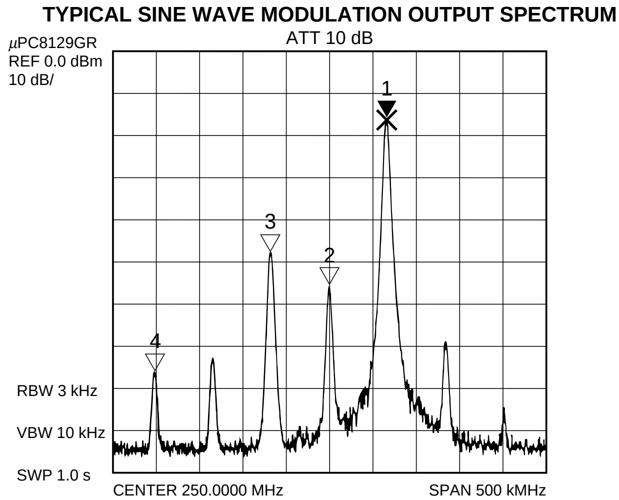
P_{MODout}, LoL, ImR, $IM_{3I/Q}$ vs f_{LO1in}



ΔΦ vs $V_{I/Qin}$



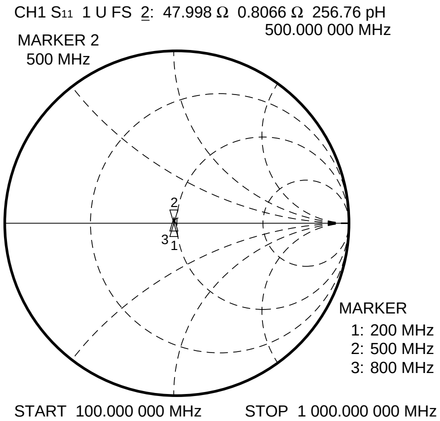




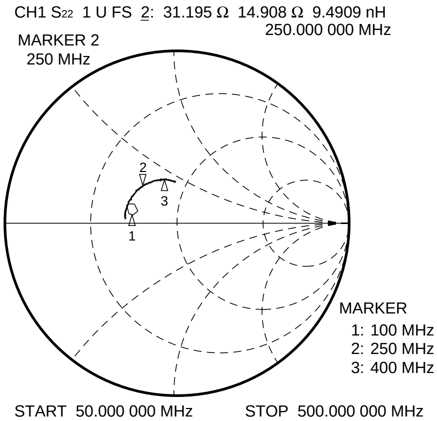
*** Multi Marker List ***

No.1:	250.0677 MHz	–16.37 dBm
No.2:	250.0000 MHz	–39.49 dBc
No.3:	249.9323 MHz	–31.07 dBc
No.4:	249.7969 MHz	–58.80 dBc

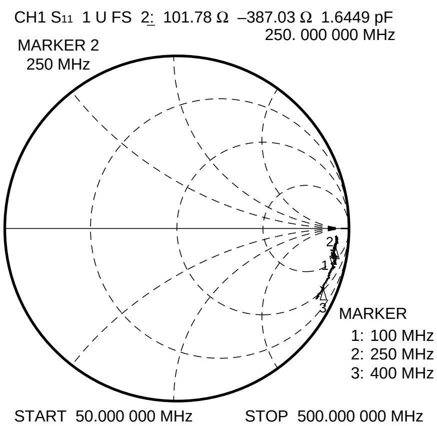
LO1 INPUT (Pin8) IMPEDANCE
V_{CC} = V_{PS} = 3 V



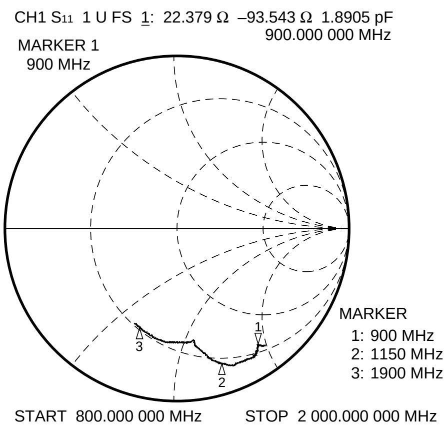
MOD OUTPUT (Pin3) IMPEDANCE
V_{CC} = V_{PS} = 3 V



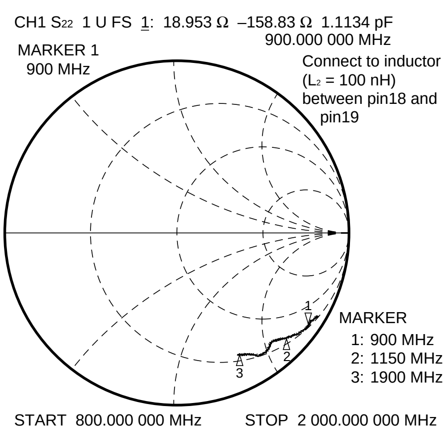
Up-Con. INPUT (Pin1) IMPEDANCE
V_{CC} = V_{PS} = 3 V



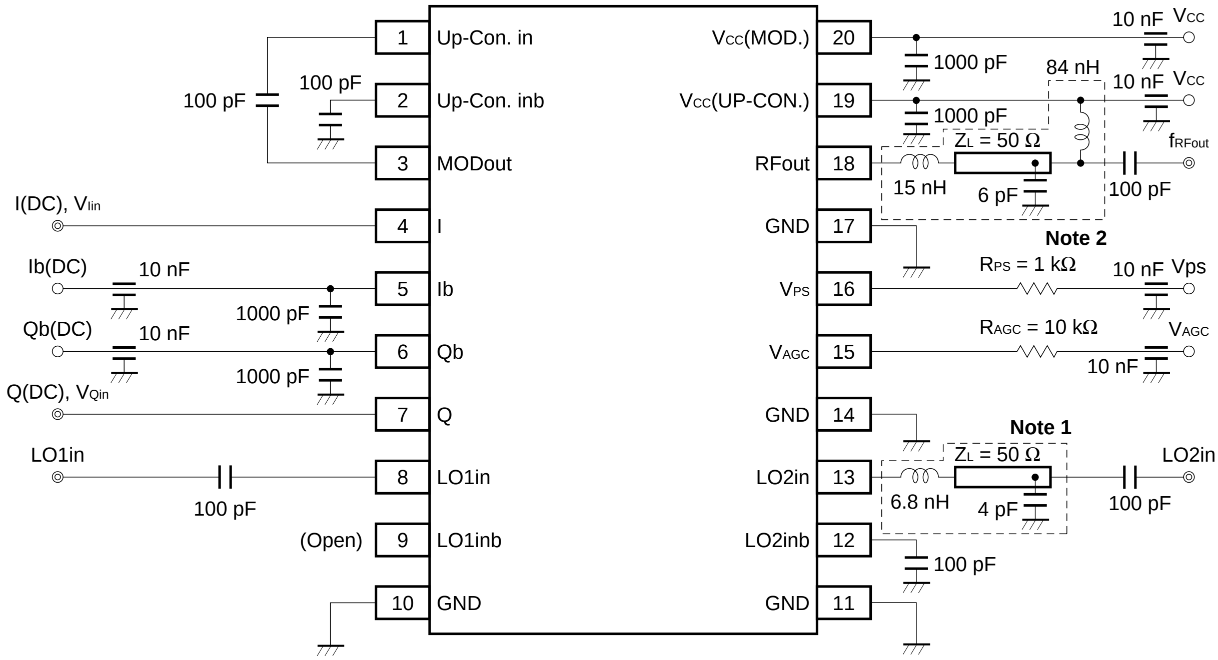
LO2 INPUT (Pin13) IMPEDANCE
V_{CC} = V_{PS} = 3 V



RF OUTPUT (Pin18) IMPEDANCE
V_{CC} = V_{PS} = 3 V



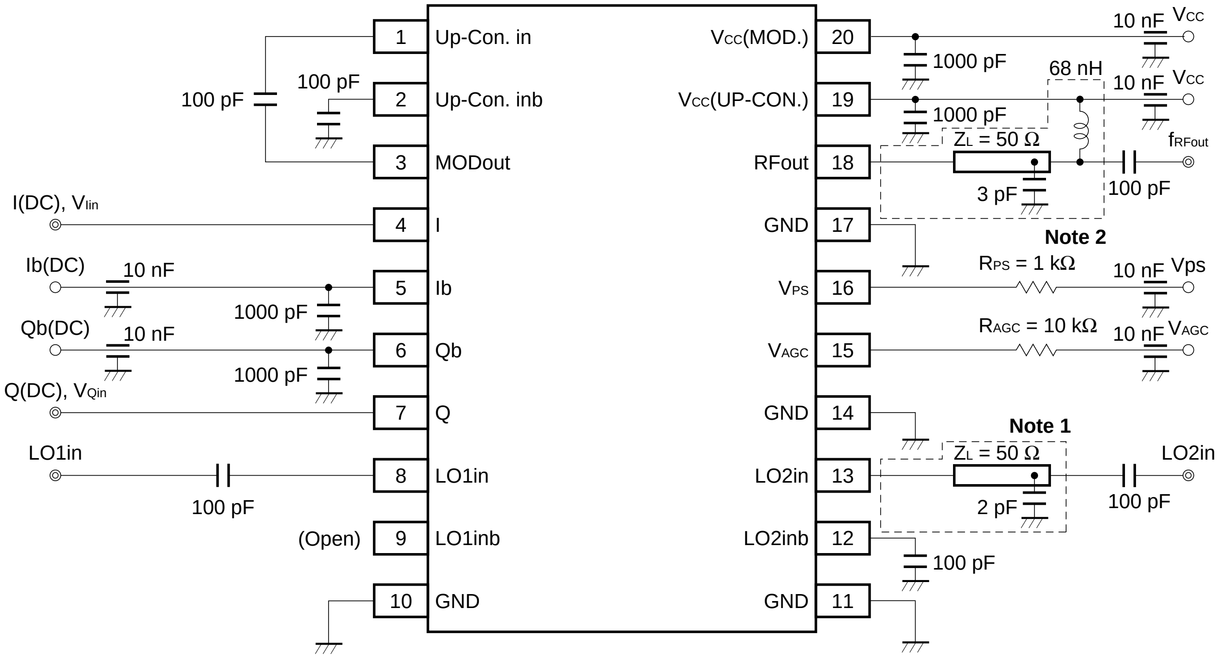
TEST CIRCUIT 1 (In the case of f_{RFout} = 900 MHz Band)



Notes 1. 50 Ω matching circuit at f_{LO2in} = 1150 MHz.
In the case of using NEC's evaluation board.

2. 50 Ω matching circuit at f_{RFout} = 900 MHz.
In the case of using NEC's evaluation board.

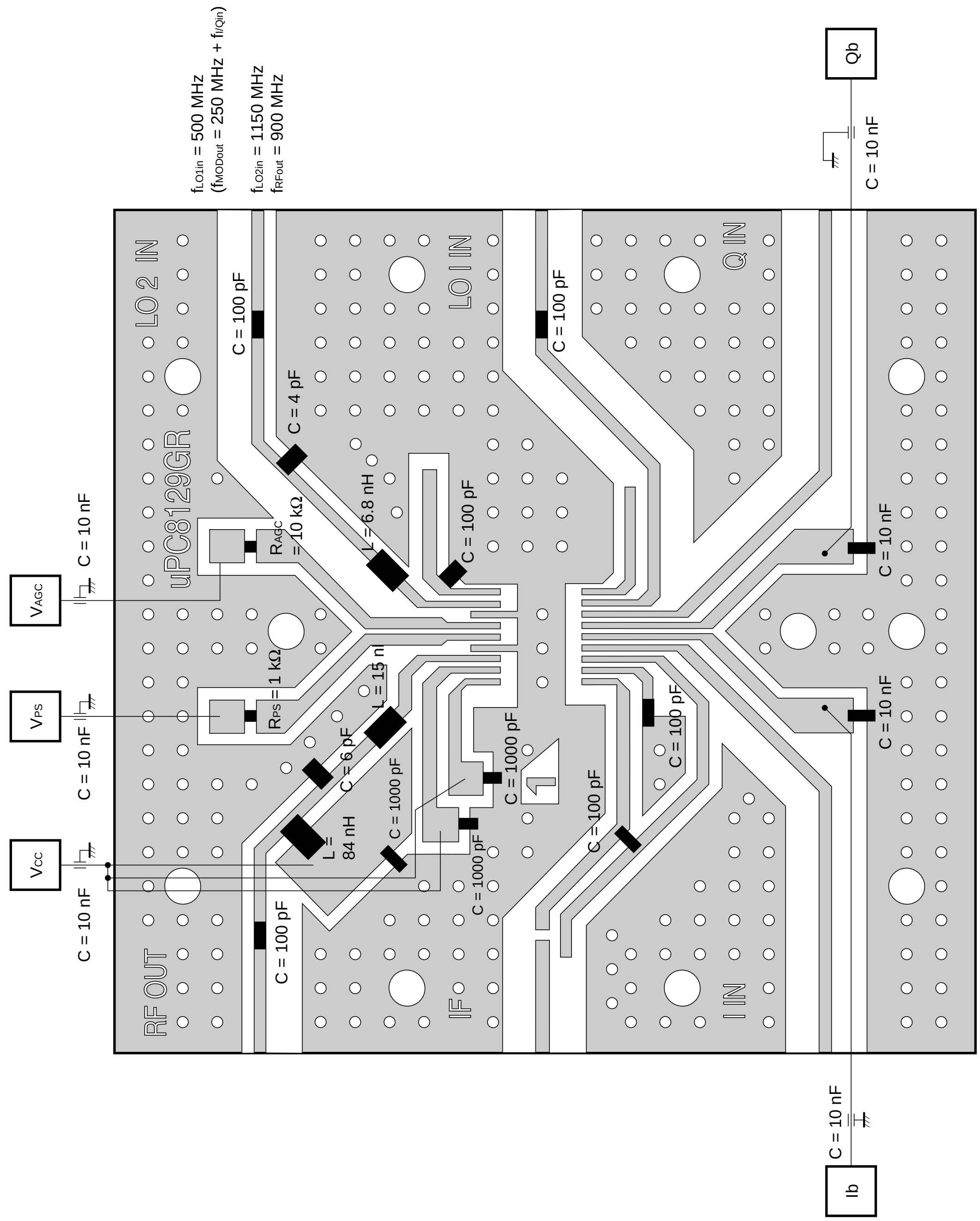
TEST CIRCUIT 2 (In the case of f_{RFout} = 1900 MHz Band)



Notes 1. 50 Ω matching circuit at f_{LO2in} = 1650 MHz.
In the case of using NEC's evaluation board.

2. 50 Ω matching circuit at f_{RFout} = 1900 MHz.
In the case of using NEC's evaluation board.

EXAMPLE OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD



Notes 1. Double-sided patterning with 35 μm thick copper on 50 × 50 × 0.4 mm polyimide board.

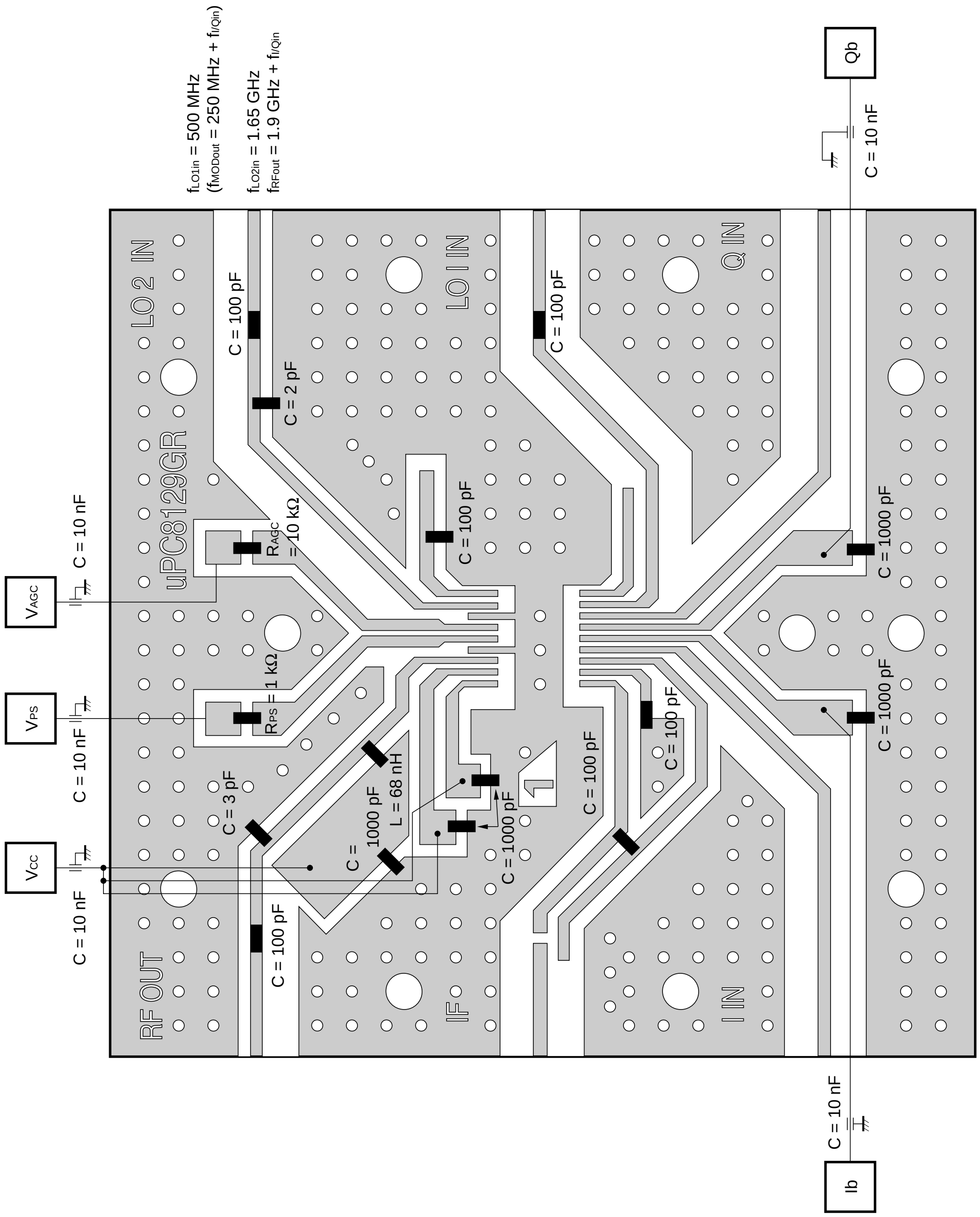
2. GND pattern on backside.

3. Solder coating over patterns.

4. ∘, ○ indicate through-holes.

NOTICE **The test circuits and board pattern on data sheet are for performance evaluation use only. In the case of actual design-in, matching circuit should be determined using S-parameter of desired frequency in accordance to actual mounting pattern.**

EXAMPLE OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD



Notes 1. Double-sided patterning with 35 μm thick copper on polyimide board.

2. GND pattern on backside.

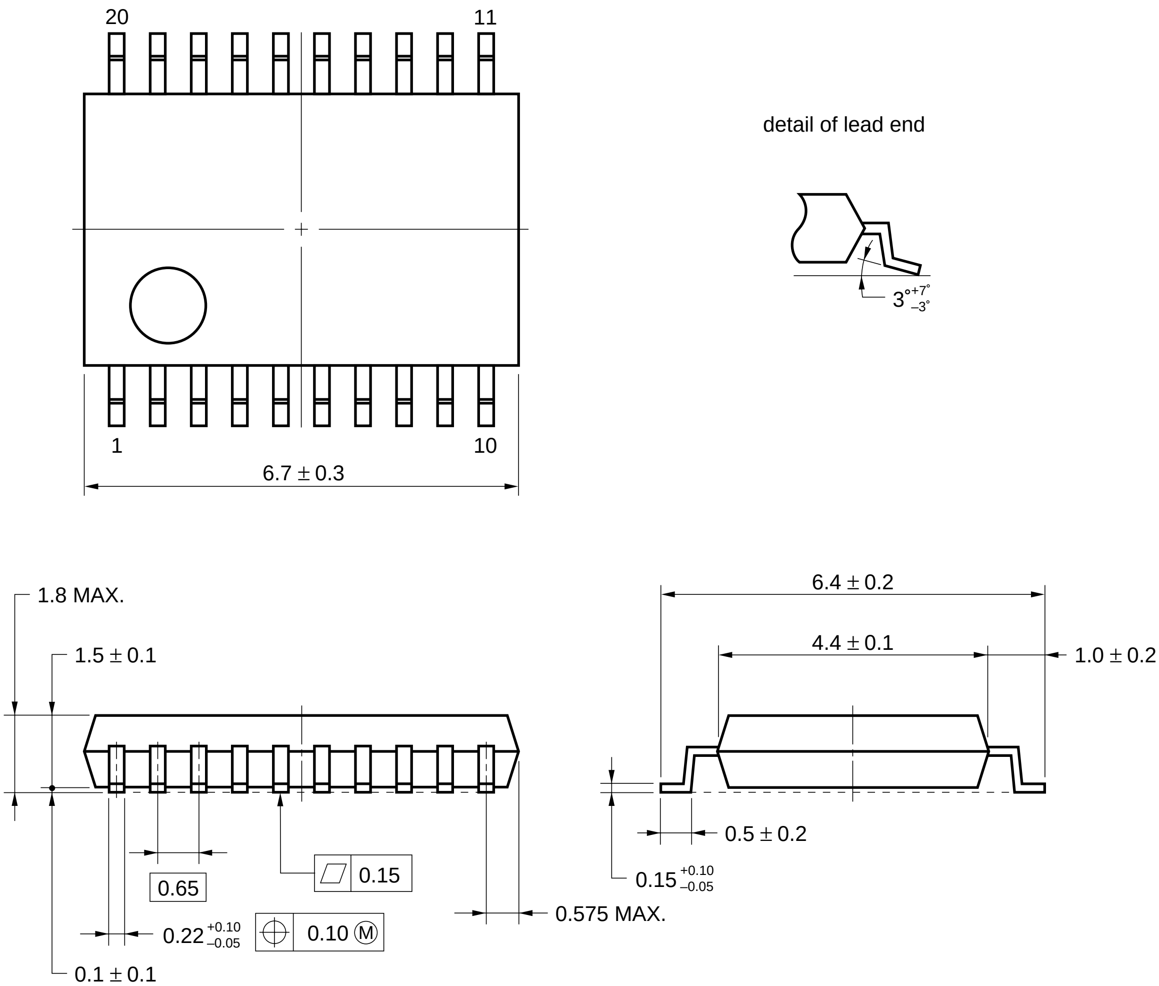
3. Solder coating over patterns.

4. ∘, ○ indicate through-holes.

NOTICE **The test circuits and board pattern on data sheet are for performance evaluation use only. In the case of actual design-in, matching circuit should be determined using S-parameter of desired frequency in accordance to actual mounting pattern.**

PACKAGE DIMENSIONS

★ **20 PIN PLASTIC SSOP (225 mil) (UNIT: mm)**



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (e.x. 1000 pF) to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with sales representatives.

μPC8129GR

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 2, Exposure limit[Note]: None	IR35-00-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 2, Exposure limit[Note]: None	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit[Note]: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 3 seconds/pin or below, Exposure limit[Note]: None	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Apply only a single process at once, except for "Partial heating method".
For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).