

HIGH VOLTAGE CMOS DRIVER FOR PDP, EL, VFD**DESCRIPTION**

μ PD16310 is high voltage driver for PDP, EL or VFD graphic panel structured by CMOS process. Logic power supply is 5.0 V connecting direct to control logic. Maximum output voltage is 80 V and maximum current is 50 mA.

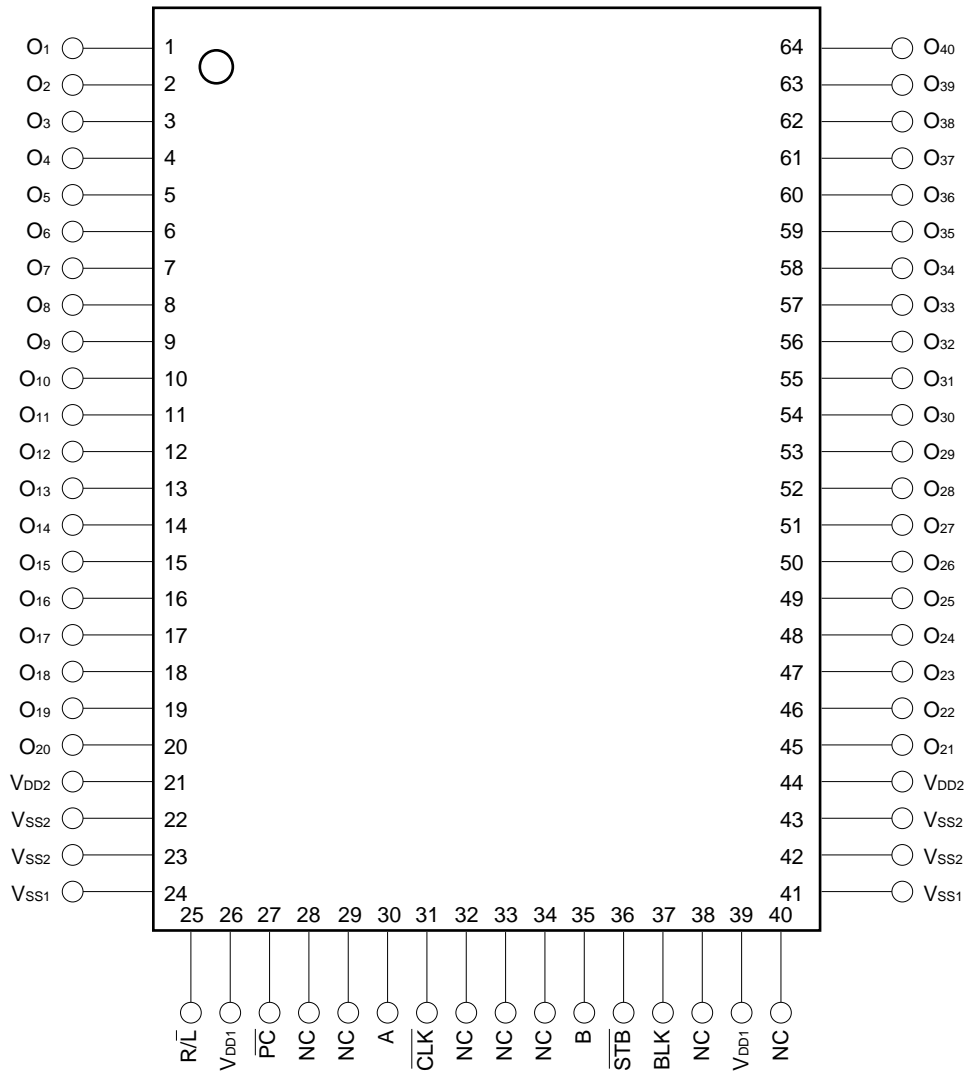
FEATURES

- 80 V Output Voltage Swing Capability
- 50 mA Output Sink and Source Current Capability
- 40 bit Shift-register and Latch
- High Speed Serial DATA Transferring ($f_{max.} = 20 \text{ MHz MIN.}$)
- Low Standby Current 100 μA

ORDERING INFORMATION

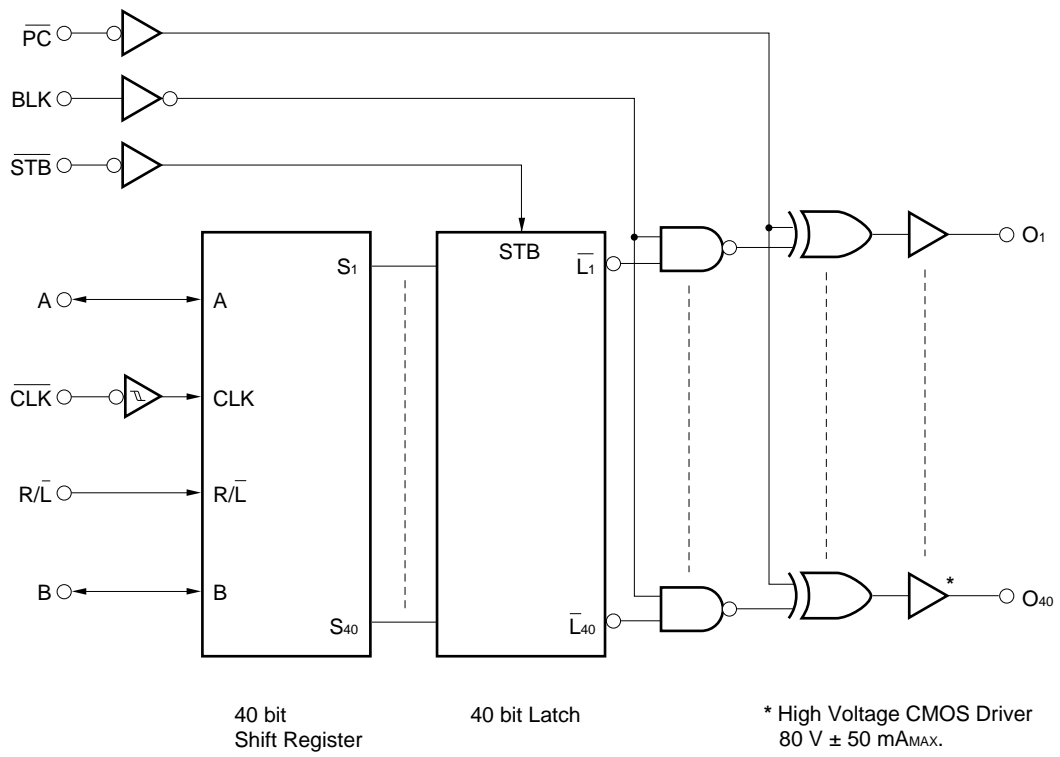
Part Number	Package
μ PD16310GF-3L9	80-pin plastic QFP (3 direction lead)

PIN CONNECTION DIAGRAM (Top View)



Note The 33 pin (NC) should be open.
 All the power supply terminals should be used.
 V_{SS1} and V_{SS2} should be respectively connected with themselves outside.
 To prevent latch up breakdown, the power should be turned ON in order V_{DD1}, logic input, V_{DD2}.
 It should be turned OFF in the opposite order.
 This relationship should be followed during transition period as well.

BLOCK DIAGRAM



PN CONFIGURATION

PIN No.	SYMBOL	PIN NAME	FUNCTION
27	\overline{PC}	Polarity Change Input	All driver outputs' level are inverted while \overline{PC} is L.
37	BLK	Blank Input	All driver outputs are H or L while BLK is H.
36	\overline{STB}	Latch Strobe Input	Latch's status is data through while \overline{STB} is L.
30	A	Right Data Input/Output	R \overline{L} = H : A = IN, B = OUT R \overline{L} = L : A = OUT, B = IN
35	B	Left Data Input/Output	
31	CLK	Clock Input	Data of shift-register is shifted while CLK is going H to L. (Negative edge is active.)
25	R \overline{L}	Shift Direction Control Input	H: Right Shift Mode A → O ₁ ... O ₄₀ → B L: left Shift Mode B → O ₄₀ ... O ₁ → A
1 - 20 45 - 64	O ₁ - O ₄₀	Driver Outputs	High voltage output 80 V, 50 mA
26, 39	V _{DD1}	Logic Power Supply	5.0 V ± 10 %
21, 44	V _{DD2}	Driver Power Supply	10 to 70 V
24, 41	V _{SS1}	Ground (for Logic)	Connect to the system ground.
22, 23, 42, 43	V _{SS2}	Ground (for Driver)	Connect to the system ground.
28, 29, 32 - 34 38, 40	NC	No Connect	No. 33 pin should be open.

TRUTH TABLE 1 (Shift-Register part)

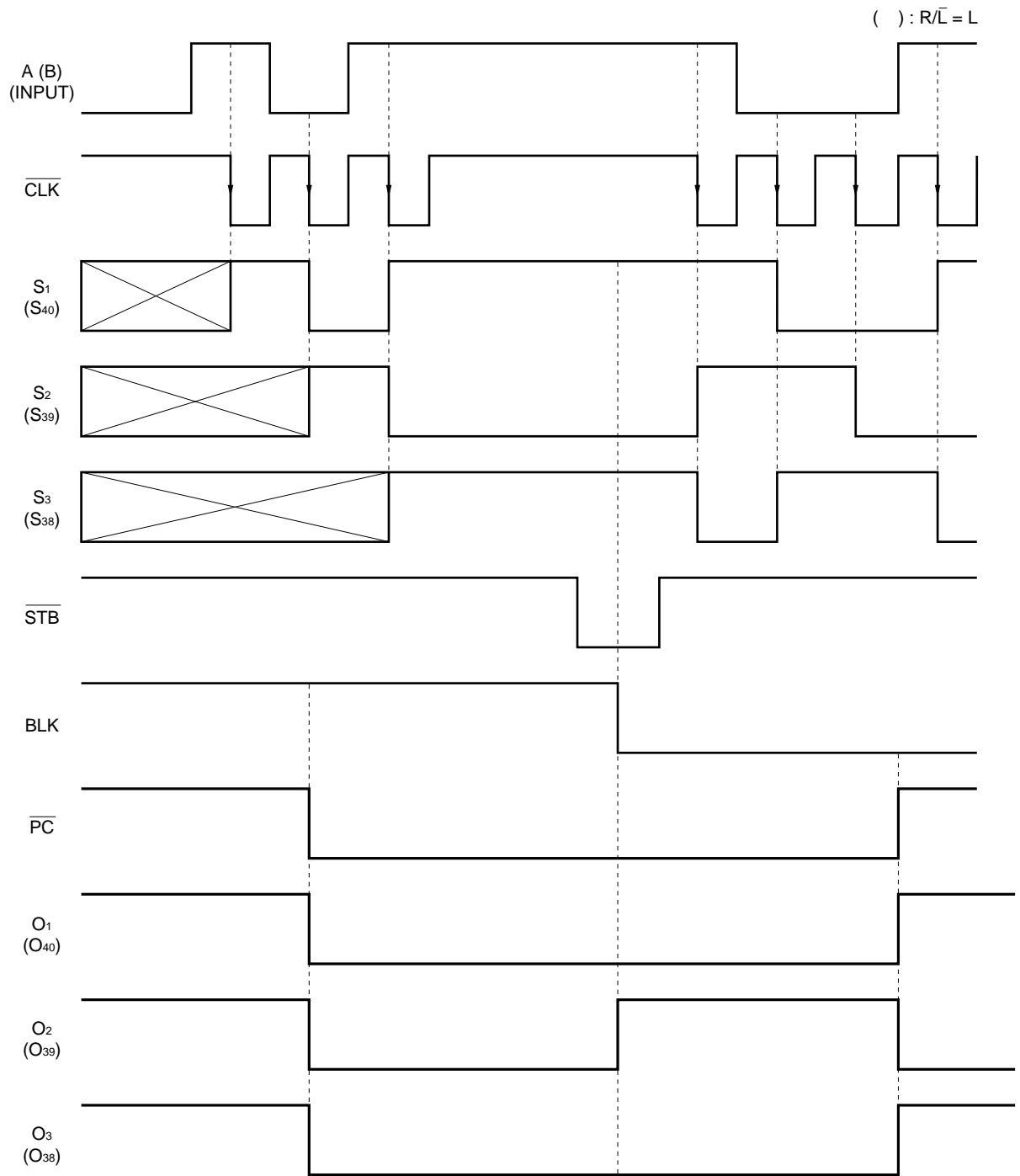
INPUT		IN/OUT		SHIFT-REGISTER
R \overline{L}	CLK	A	B	
H	↓	IN	OUT	DATA is shifted.
H	H or L	IN	OUT	No Change.
L	↓	OUT	IN	DATA is shifted.
L	H or L	OUT	IN	No Change.

TRUTH TABLE 2 (Latch, Driver part)

INPUT				DRIVER OUTPUT
A (B)	\overline{STB}	BLK	\overline{PC}	
X	X	H	H	ALL H
X	X	H	L	ALL L
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
X	H	L	H	Latch's data output
X	H	L	L	Latch's data output (inverting)

X = H or L, H = High Level, L = Low Level

TIMING CHART



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, V_{SS1} = V_{SS2} = 0 V)

PARAMETER	SYMBOL	RATINGS	UNIT
Logic Power Supply	V _{DD1}	-0.5 to +7.0	V
Input Voltage	V _I	-0.5 to V _{DD1} + 0.5	V
Logic Output Voltage	V _{O1}	-0.5 to V _{DD1} + 0.5	V
Driver Power Supply	V _{DD2}	-0.5 to 80	V
Driver Output Voltage	V _{O2}	-0.5 to V _{DD2} + 0.5	V
Drive Maximum Current	I _{O2}	±50	mA
Power Dissipation	P _D	1 000	mW
Operating Temperature	T _{opt}	-40 to +85	°C
Storage Temperature	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C, V_{SS1} = V_{SS2} = 0 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic Power Supply	V _{DD1}	4.5	5.0	5.5	V
High Level Input Voltage	V _{IH}	0.7 · V _{DD1}		V _{DD1}	V
Low Level Input Voltage	V _{IL}	0		0.2 · V _{DD1}	V
Driver Power Supply	V _{DD2}	10		70	V
Driver Output Current	I _{OL2}			+40	mA
	I _{OH2}			-40	mA

DC CHARACTERISTICS (T_a = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High Level Output Voltage	V _{OH1}	0.9 · V _{DD1}			V	Logic, I _{OH1} = -1.0 mA
Low Level Output Voltage	V _{OL1}			0.1 · V _{DD1}	V	Logic, I _{OL1} = 1.0 mA
High Level Output Voltage	V _{OH21}	69			V	O ₁ - O ₄₀ , I _{OH2} = -1.0 mA
	V _{OH22}	65			V	O ₁ - O ₄₀ , I _{OH2} = -10 mA
Low Level Output Voltage	V _{OL21}			1.0	V	O ₁ - O ₄₀ , I _{OL2} = 5.0 mA
	V _{OL22}			10	V	O ₁ - O ₄₀ , I _{OL2} = 40 mA
High Level Input Current	I _{IH}			1.0	μA	V _I = V _{DD1}
Low Level Input Current	I _{IL}			-1.0	μA	V _I = 0 V
High Level Input Voltage	V _{IH}	0.7 · V _{DD1}			V	
Low Level Input Voltage	V _{IL}			0.2 · V _{DD1}	V	
Standby Current	I _{DD1}			10	μA	for V _{DD1} , T _a = 25 °C
	I _{DD1}			100	μA	for V _{DD1} , T _a = -40 to +85 °C
	I _{DD2}			100	μA	for V _{DD2} , T _a = 25 °C
	I _{DD2}			1 000	μA	for V _{DD2} , T _a = -40 to +85 °C

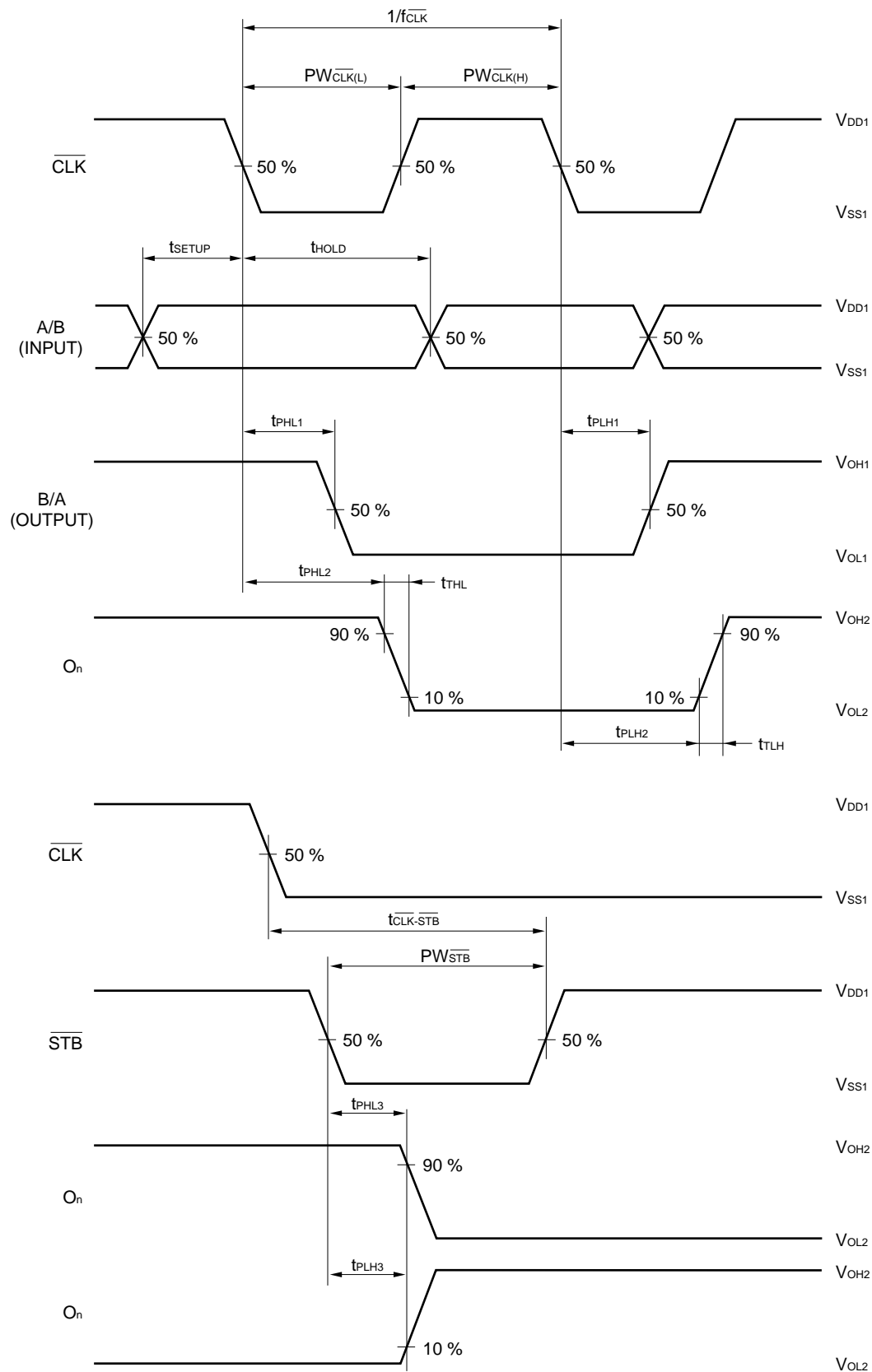
AC CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$, $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 70\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$, Logic $C_L = 15\text{ pF}$, Driver $C_L = 50\text{ pF}$)

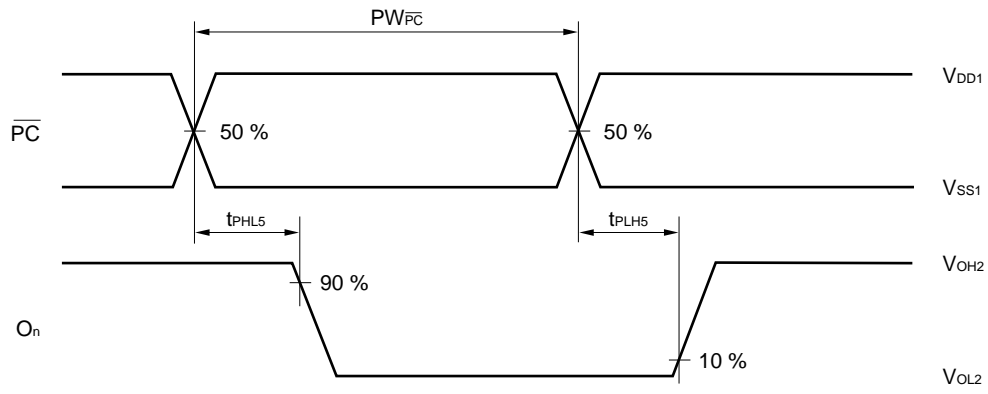
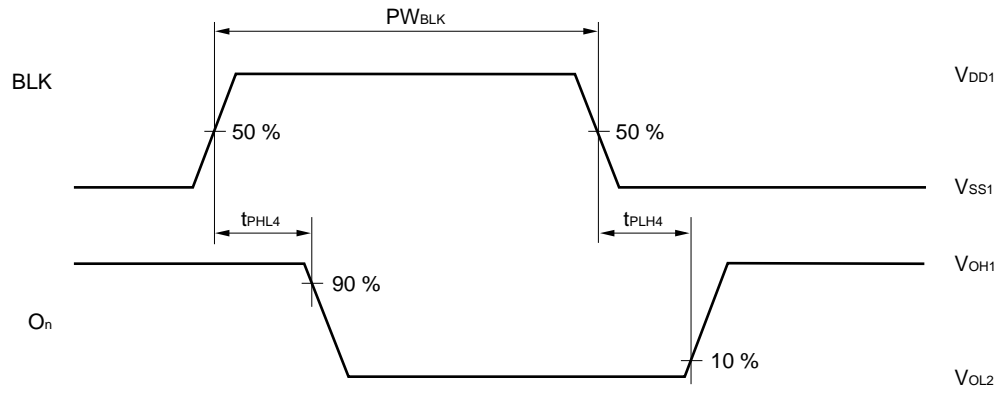
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Delay Time	t_{PHL1}			50	ns	$\overline{\text{CLK}} \rightarrow \text{A/B}$
	t_{PLH1}			50	ns	
	t_{PHL2}			160	ns	$\overline{\text{CLK}} \rightarrow \text{O}_1 - \text{O}_{40}$
	t_{PLH2}			160	ns	
	t_{PHL3}			150	ns	$\overline{\text{STB}} \rightarrow \text{O}_1 - \text{O}_{40}$
	t_{PLH3}			150	ns	
	t_{PHL4}			145	ns	$\text{BLK} \rightarrow \text{O}_1 - \text{O}_{40}$
	t_{PLH4}			145	ns	
	t_{PHL5}			140	ns	$\overline{\text{PC}} \rightarrow \text{O}_1 - \text{O}_{40}$
t_{PLH5}			140	ns		
Rise Time	t_{TLH}			70	ns	$\text{O}_1 - \text{O}_{40}$
Fall Time	t_{THL}			70	ns	$\text{O}_1 - \text{O}_{40}$
Maximum Frequency	$f_{\text{max.}}$	20	30		MHz	Duty = 50 %, for CLK
Input Capacitance	C_i		10	20	pF	

AC TIMING REQUIREMENT ($T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, $V_{DD1} = 4.5\text{ to }5.5\text{ V}$, $V_{DD2} = 10\text{ to }70\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Clock Pulse Width	$PW_{\overline{\text{CLK}}}$	20			ns	
Strobe Pulse Width	$PW_{\overline{\text{STB}}}$	20			ns	
Blank Pulse Width	PW_{BLK}	200			ns	
Polarity Change Pulse Width	$PW_{\overline{\text{PC}}}$	200			ns	
Data Setup Time	t_{SETUP}	10			ns	
Data Hold Time	t_{HOLD}	10			ns	
Setup Time	$t_{\text{CLK-STB}}$	50			ns	for $\overline{\text{CLK}} \downarrow$ to $\overline{\text{STB}} \uparrow$

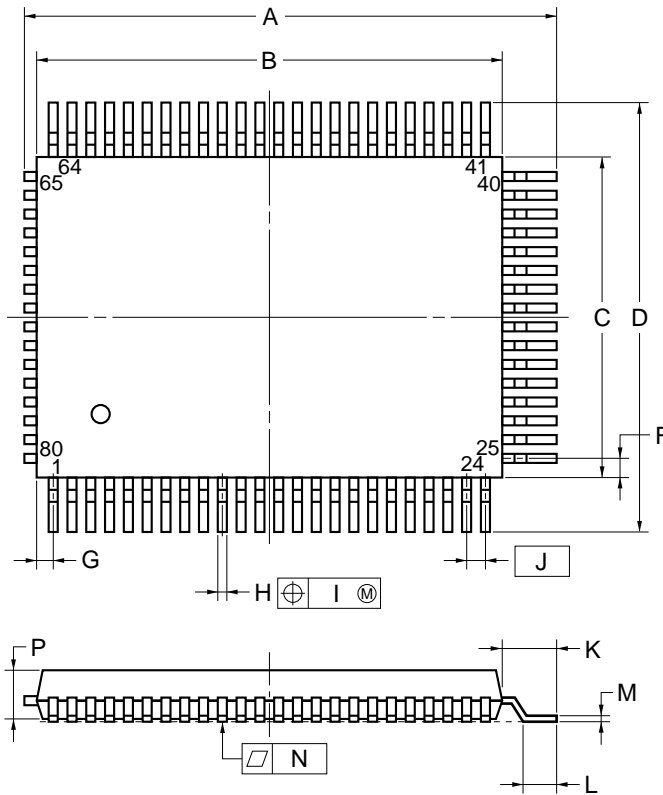
AC CHARACTERISTICS WAVEFORM



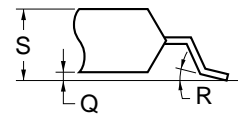


PACKAGE DIMENSIONS

80 PIN PLASTIC QFP (THREE DIRECTIONS) (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.3±0.4	0.878±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P80GF-80-3L9-2

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

μPD16310GF-3L9

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	IR30-00-1
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: None	VP15-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

* Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note Do not apply more than a single process at once, except for "Partial heating method."

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Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.