DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD178P018

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD178P018 is a device in which the on-chip mask ROM of the μPD178018 is replaced with a one-time PROM or EPROM.

Because this device can be programmed by users, it is ideally suited for system evaluation, small-lot and multiple-device production, and early development and time-to-market.

The μPD178P018 is a PROM version corresponding to the μPD178004, 178006, and 178016.

Caution The μPD178P018KK-T does not maintain planned reliability when used in your system's mass-produced products. Please use only experimentally or for evaluation purposes during trial manufacture.

For more information on functions, refer to the following User's Manuals. Be sure to read them when designing.

μPD178018 Subseries User's Manual: U11410E
78K/0 Series User's Manual Instruction: U12326E (In Preparation)

FEATURES

- Pin-compatible with mask ROM version (except for V_{PP} pin)
- Internal PROM: 60 Kbytes
  - μPD178P018GC : One-time programmable (ideally suited for small-lot production)
  - μPD178P018KK-T : Reprogrammable (ideally suited for system evaluation)
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 2048 bytes
- Buffer RAM: 32 bytes
- Can be operated in the same power supply voltage as the mask ROM version (During PLL operation: V_{DD} = 4.5 to 5.5 V)

The electrical specifications (power supply current, etc.) and PLL analog specifications of the μPD178P018 differ from that of mask ROM versions. So, these differences should be considered and verified before application sets are mass-produced.

In this document, the term PROM is used in parts common to one-time PROM versions and EPROM versions.

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APPLICATIONS

Car stereo, home stereo systems

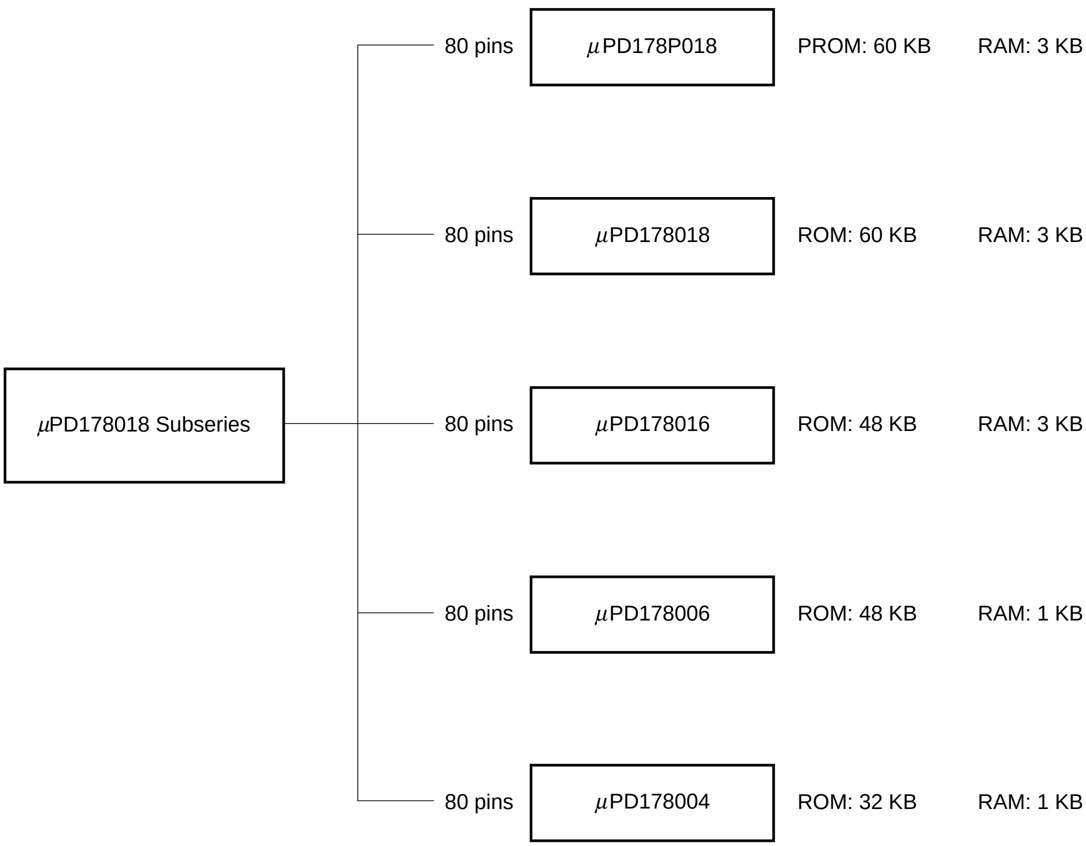
ORDERING INFORMATION

Part Number	Package	Internal ROM	Quality Grade
μPD178P018GC-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)	One-Time PROM	Standard
μPD178P018KK-T[Note]	80-pin ceramic WQFN (14 × 14 mm, 0.65-mm pitch)	EPROM	Not applicable

Note Under planning

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

μPD178018 SUBSERIES EXPANSION



FUNCTION DESCRIPTION

(1/2)

Item		Function
Internal memory		• PROM : 60 Kbytes • RAM High-speed RAM : 1024 bytes Expansion RAM : 2048 bytes Buffer RAM : 32 bytes
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		With variable instruction execution time function 0.44 μs/0.88 μs/1.78 μs/3.56 μs/7.11 μs/14.22 μs (with 4.5-MHz crystal resonator)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD Adjust, etc.
I/O port		Total : 62 pins • CMOS input : 1 pin • CMOS I/O : 54 pins • N-ch open-drain I/O : 4 pins • N-ch open-drain output : 3 pins
A/D converter		8-bit resolution × 6 channels
Serial interface		• 3-wire/SBI/2-wire/I²C bus[Note] mode selectable : 1 channel • 3-wire serial I/O mode (with automatic transmit/receive function of up to 32 bytes) : 1 channel
Timer		• Basic timer (timer carry FF (10 Hz)) : 1 channel • 8-bit timer/event counter : 2 channels • 8-bit timer (D/A converter: PWM output) : 1 channel • Watchdog timer : 1 channel
Buzzer (BEEP) output		1.5 kHz, 3 kHz, 6 kHz
Vectored interrupt	Maskable interrupt	Internal: 8, external: 7
	Non-maskable interrupt	Internal: 1
	Software interrupt	Internal: 1
Test input		Internal: 1
PLL frequency synthesizer	Division mode	Two types • Direct division mode (VCOL pin) • Pulse swallow mode (VCOH and VCOL pins)
	Reference frequency	11 types selectable by program (1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50 kHz)
	Charge pump	Error out output: 2
	Phase comparator	Unlock detectable by program

Frequency counter		• Frequency measurement
		  • AMIFC pin: for 450-kHz count
		  • FMIFC pin: for 450-kHz/10.7-MHz count

D/A converter (PWM output)		8-/9-bit resolution × 3 channels (shared by 8-bit timer)
Standby function		• HALT mode • STOP mode

Note When using the I²C bus mode (including when this mode is implemented by program without using the peripheral hardware), consult your local NEC sales representative when you place an order for mask.

(2/2)

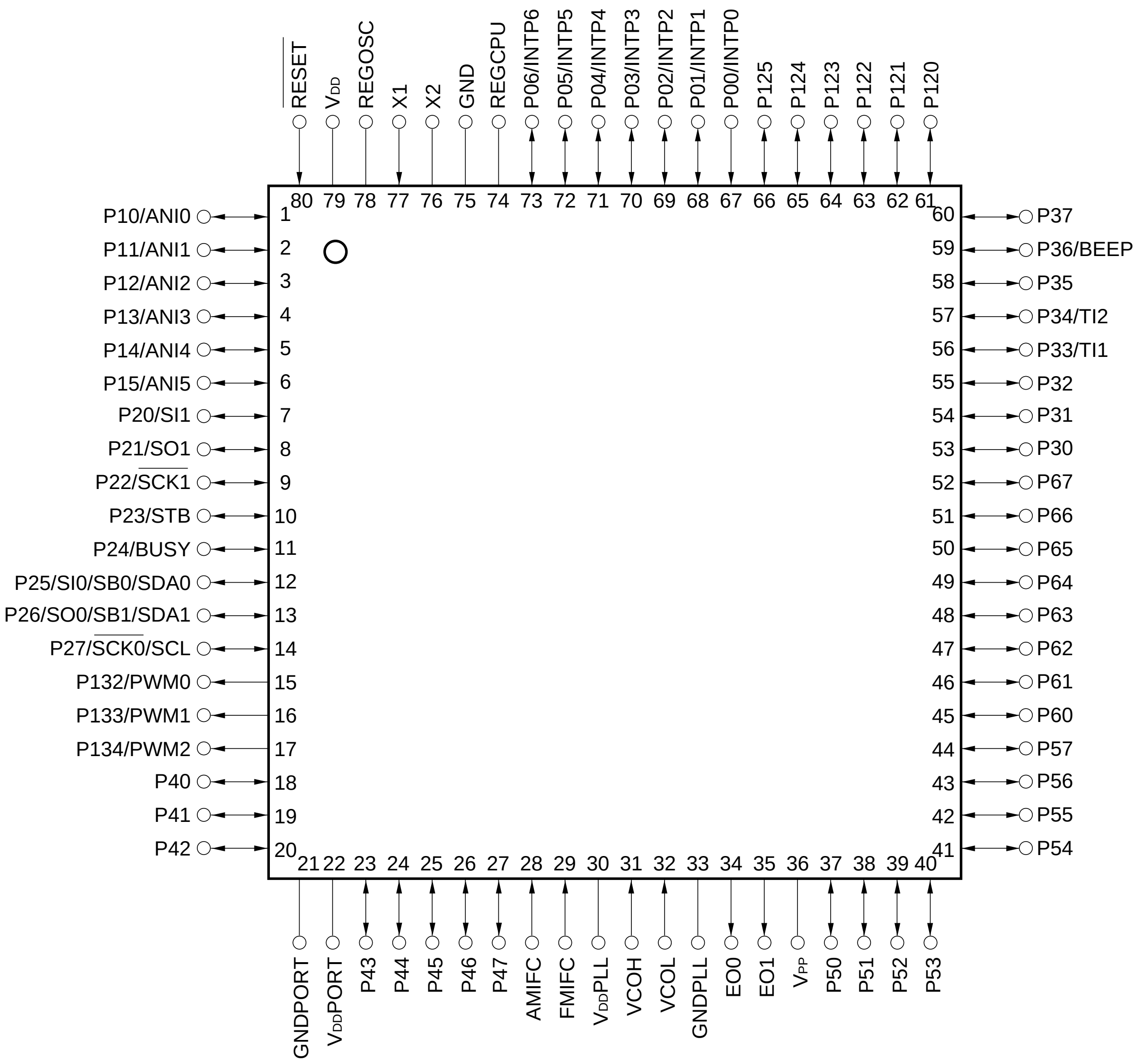
Item	Function
Reset	• Reset via the $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Reset by power-ON clear circuit (3-value detection) • Detection of less than 4.5 V[Note] (CPU clock: f_X) • Detection of less than 3.5 V[Note] (CPU clock: $f_X/2$ or less and on power application) • Detection of less than 2.5 V[Note] (in STOP mode)
Power supply voltage	• V_{DD} = 4.5 to 5.5 V (with PLL operating) • V_{DD} = 3.5 to 5.5 V (with CPU operating, CPU clock: $f_X/2$ or less) • V_{DD} = 4.5 to 5.5 V (with CPU operating, CPU clock: f_X)
Package	• 80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch) • 80-pin ceramic WQFN (14 × 14 mm, 0.65-mm pitch)

Note These voltage values are maximum values. The reset is actually executed at a voltage lower than these values.

PIN CONFIGURATIONS (TOP VIEW)

(1) Normal operating mode

- **80-PIN PLASTIC QFP (14 × 14 mm, 0.65-mm pitch)**
  μPD178P018GC-3B9
- **80-PIN CERAMIC WQFN (14 × 14 mm, 0.65-mm pitch)**
  μPD178P018KK-T



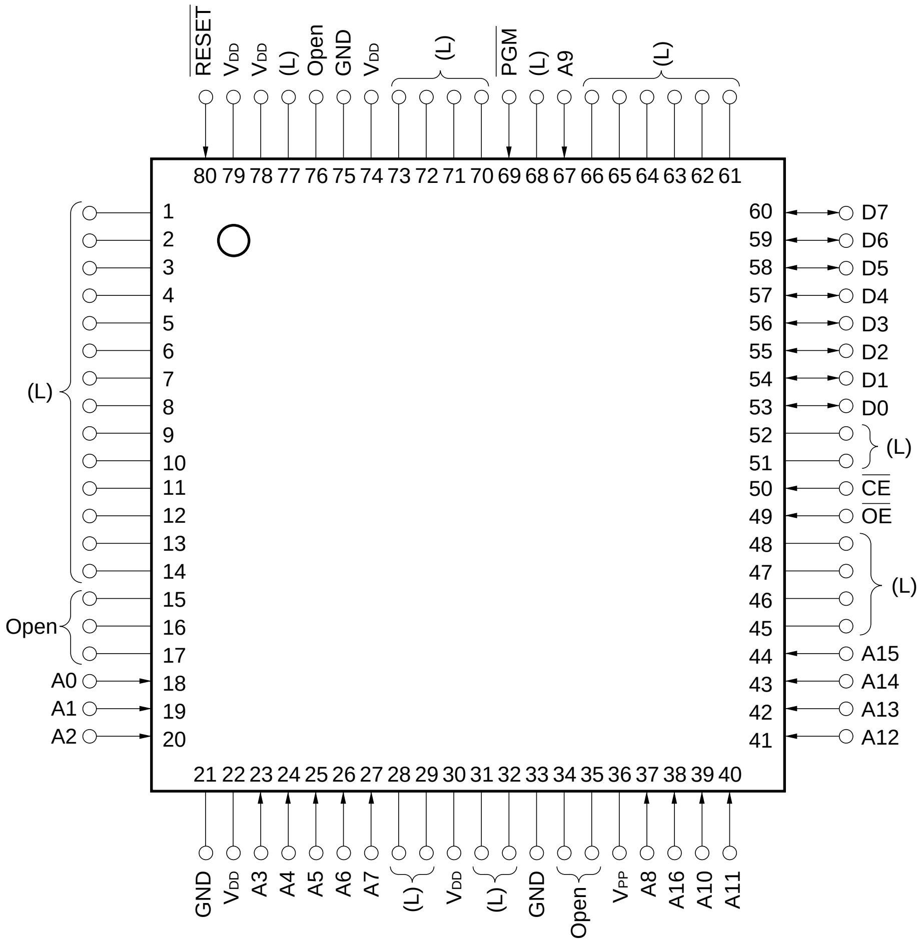
Cautions 1. Connect the V_{PP} pin to GND directly.
2. Connect the V_{DD}PORT and V_{DD}PLL pins to V_{DD}.
3. Connect the GNDPORT and GNDPLL pins to GND.
4. Connect each of the REGOSC and REGCPU pins to GND via a 0.1-μF capacitor.

AMIFC	: AM Intermediate Frequency Counter Input
ANI0 to ANI5	: A/D Converter Input
BEEP	: Buzzer Output
BUSY	: Busy Output
EO0, EO1	: Error Out Output
FMIFC	: FM Intermediate Frequency Counter Input
GND	: Ground
GNDPLL	: PLL Ground
GNDPORT	: Port Ground
INTP0 to INTP6	: Interrupt Inputs
P00 to P06	: Port 0
P10 to P15	: Port 1
P20 to P27	: Port 2
P30 to P37	: Port 3
P40 to P47	: Port 4
P50 to P57	: Port 5
P60 to P67	: Port 6
P120 to P125	: Port 12
P132 to P134	: Port 13

PWM0 to PWM2	: PWM Output
REGCPU	: Regulator for CPU Power Supply
REGOSC	: Regulator for Oscillator
$\overline{\text{RESET}}$	: Reset Input
SB0, SB1	: Serial Data Bus Input/Output
$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$	: Serial Clock Input/Output
SCL	: Serial Clock Input/Output
SDA0, SDA1	: Serial Data Input/Output
SI0, SI1	: Serial Data Input
SO0, SO1	: Serial Data Output
STB	: Strobe Output
TI1, TI2	: Timer Clock Input
VCOL, VCOH	: Local Oscillation Input
V_{DD}	: Power Supply
V_{DD}PLL	: PLL Power Supply
V_{DD}PORT	: Port Power Supply
V_{PP}	: Programming Power Supply
X1, X2	: Crystal Resonator Connection

(2) **PROM programming mode**

- **80-PIN PLASTIC QFP (14 × 14 mm)**
  μPD178P018GC-3B9
- **80-PIN CERAMIC WQFN**
  μPD178P018KK-T[Note]

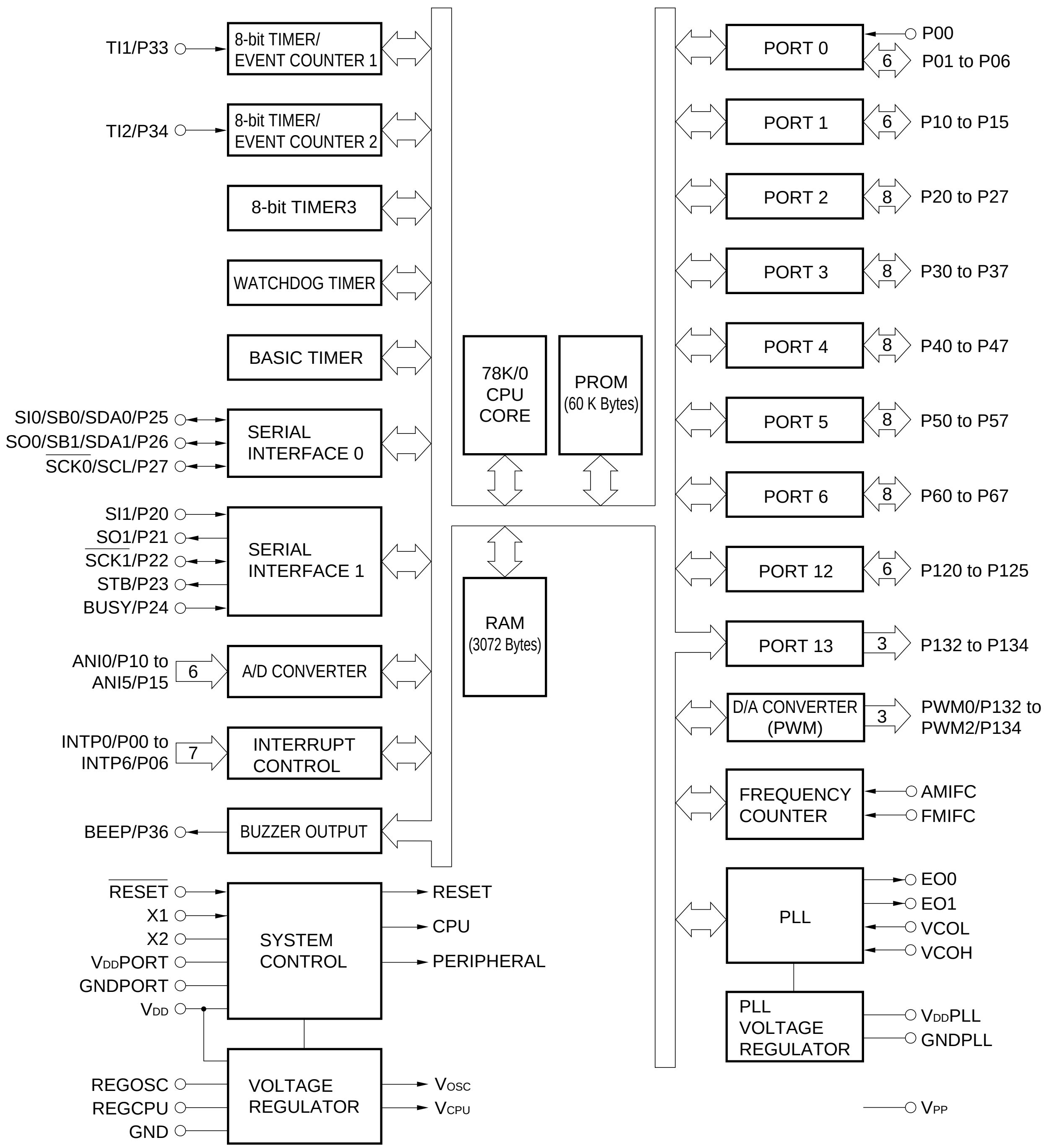


Note Under planning

Cautions **1. (L) : Individually connect to GND via a pull-down resistor.**
2. GND : Connect to GND.
3. RESET : Set to the low level.
4. Open : Leave open.

A0 to A16	:	Address Bus	GND	:	Ground	RESET	:	Reset
CE	:	Chip Enable	OE	:	Output Enable	V_{DD}	:	Power Supply
D0 to D7	:	Data Bus	PGM	:	Program	V_{PP}	:	Programming Power Supply

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTION LIST

1.1 Pins in Normal Operating Mode

(1) Port pins

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0. 7-bit input/output port.	Input only	Input	INTP0
P01 to P06	I/O		Input/output mode can be specified bit-wise.	Input	INTP1 to INTP6
P10 to P15	I/O	Port 1. 6-bit input/output port. Input/output mode can be specified bit-wise.		Input	ANI0 to ANI5
P20	I/O	Port 2. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{SCK0}$/SCL
P30 to P32	I/O	Port 3. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P33					TI1
P34					TI2
P35					—
P36					BEEP
P37					—
P40 to P47	I/O	Port 4. 8-bit input/output port. Input/output mode can be specified in 8-bit units. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	—
P50 to P57	I/O	Port 5. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P60 to P63	I/O	Port 6. 8-bit input/output port. Input/output mode can be specified bit-wise.	Middle voltage N-ch open-drain input/output port. LEDs can be driven directly.	Input	—
P64 to P67					
P120 to P125	I/O	Port 12. 6-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P132 to P134	Output	Port 13. 3-bit output port. N-ch open-drain output port.		—	PWM0 to PWM2

(2) Non-port pins (1 of 2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP6	Input	External maskable interrupt inputs with specifiable valid edges (rising edge, falling edge, both rising and falling edges).	Input	P00 to P06
SI0	Input	Serial interface serial data input	Input	P25/SB0/SDA0
SI1				P20
SO0	Output	Serial interface serial data output	Input	P26/SB1/SDA1
SO1				P21
SB0	I/O	Serial interface serial data input/output	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{\text{SCK0}}$	I/O	Serial interface serial clock input/output	Input	P27/SCL
$\overline{\text{SCK1}}$				P22
SCL				P27/$\overline{\text{SCK0}}$
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit busy input	Input	P24
TI1	Input	External count clock input to 8-bit timer (TM1)	Input	P33
TI2		External count clock input to 8-bit timer (TM2)		P34
BEEP	Output	Buzzer output	Input	P36
ANI0 to ANI5	Input	A/D converter analog input	Input	P10 to P15
PWM0 to PWM2	Output	PWM output	—	P132 to P134
EO0, EO1	Output	Error out output from charge pump of the PLL frequency synthesizer	—	—
VCOL	Input	Inputs PLL local band oscillation frequency (In HF, MF mode).	—	—
VCOH	Input	Inputs PLL local band oscillation frequency (In VHF mode).	—	—
AMIFC	Input	Inputs AM intermediate frequency counter.	—	—
FMIFC	Input	Inputs FM intermediate frequency counter.	—	—
$\overline{\text{RESET}}$	Input	System reset input	—	—
X1	Input	Crystal resonator connection for system clock oscillation	—	—
X2	—		—	—
REGOSC	—	Regulator for oscillator. Connected to GND via a 0.1-μF capacitor.	—	—
REGCPU	—	Regulator for CPU power supply. Connected to GND via a 0.1-μF capacitor.	—	—
V_{DD}	—	Positive power supply	—	—
GND	—	Ground	—	—
V_{DD}PORT	—	Positive power supply for port block	—	—
GNDPORT	—	Ground for port block	—	—
V_{DD}PLL	—	Positive power supply for PLL	—	—
GNDPLL	—	Ground for PLL	—	—

(2) Non-port pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
V_{PP}	—	High-voltage applied during program write/verification. Connected directly to GND in normal operating mode.	—	—

1.2 Pins in PROM Programming Mode

Pin Name	I/O	Function
$\overline{RESET}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to V_{PP} pin and a low-level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/verification.
A0 to A16	Input	Address bus
D0 to D7	I/O	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input in PROM programming mode.
V_{DD}	—	Positive power supply
GND	—	Ground potential

1.3 Pins Input/Output Circuits and Recommended Connection of Unused Pins

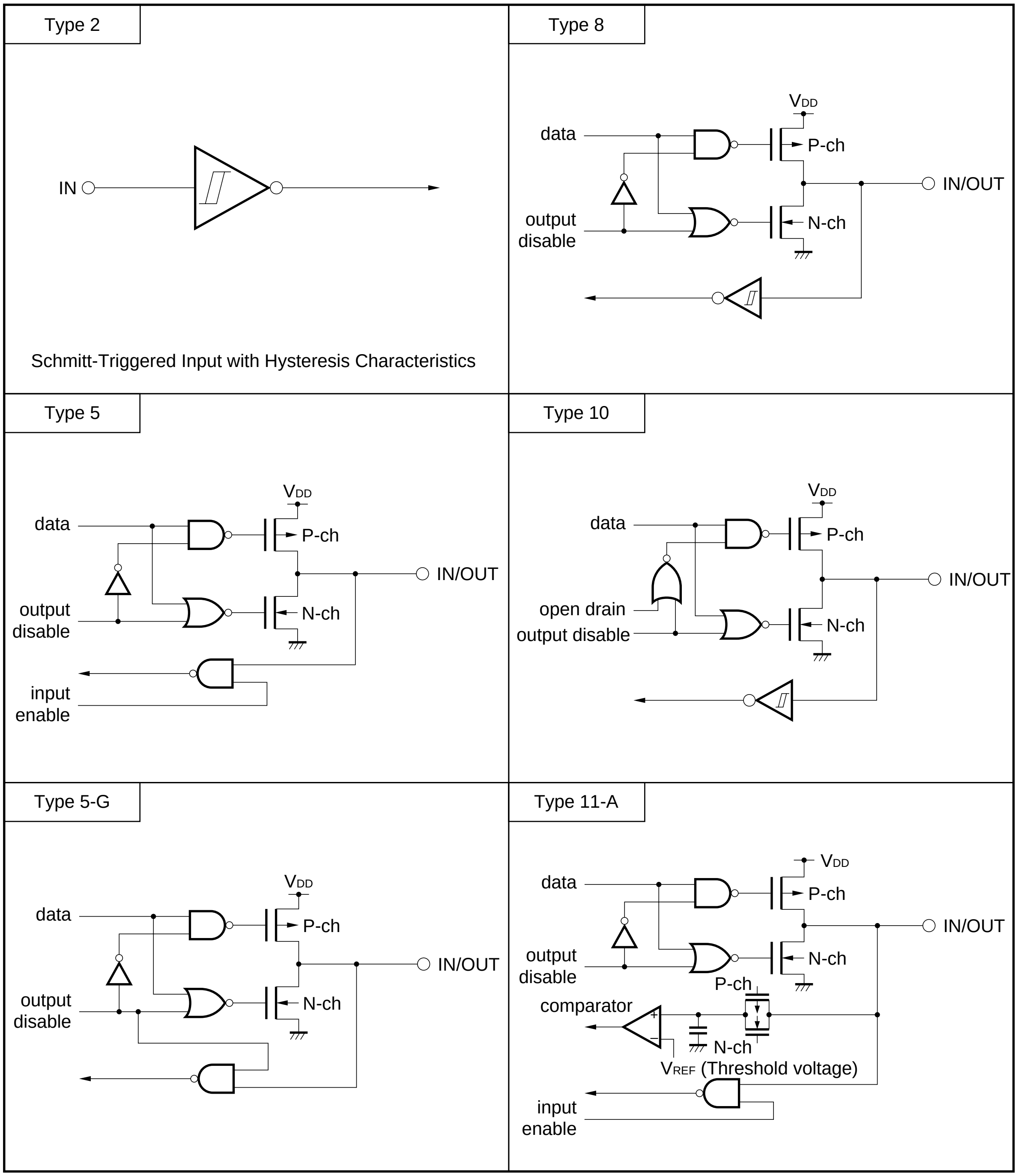
Table 1-1 shows the input/output circuit types of pins and the recommended conditions for unused pins.

Refer to Figure 1-1 for the configuration of the input/output circuit of each type.

Table 1-1. Type of I/O Circuit of Each Pin

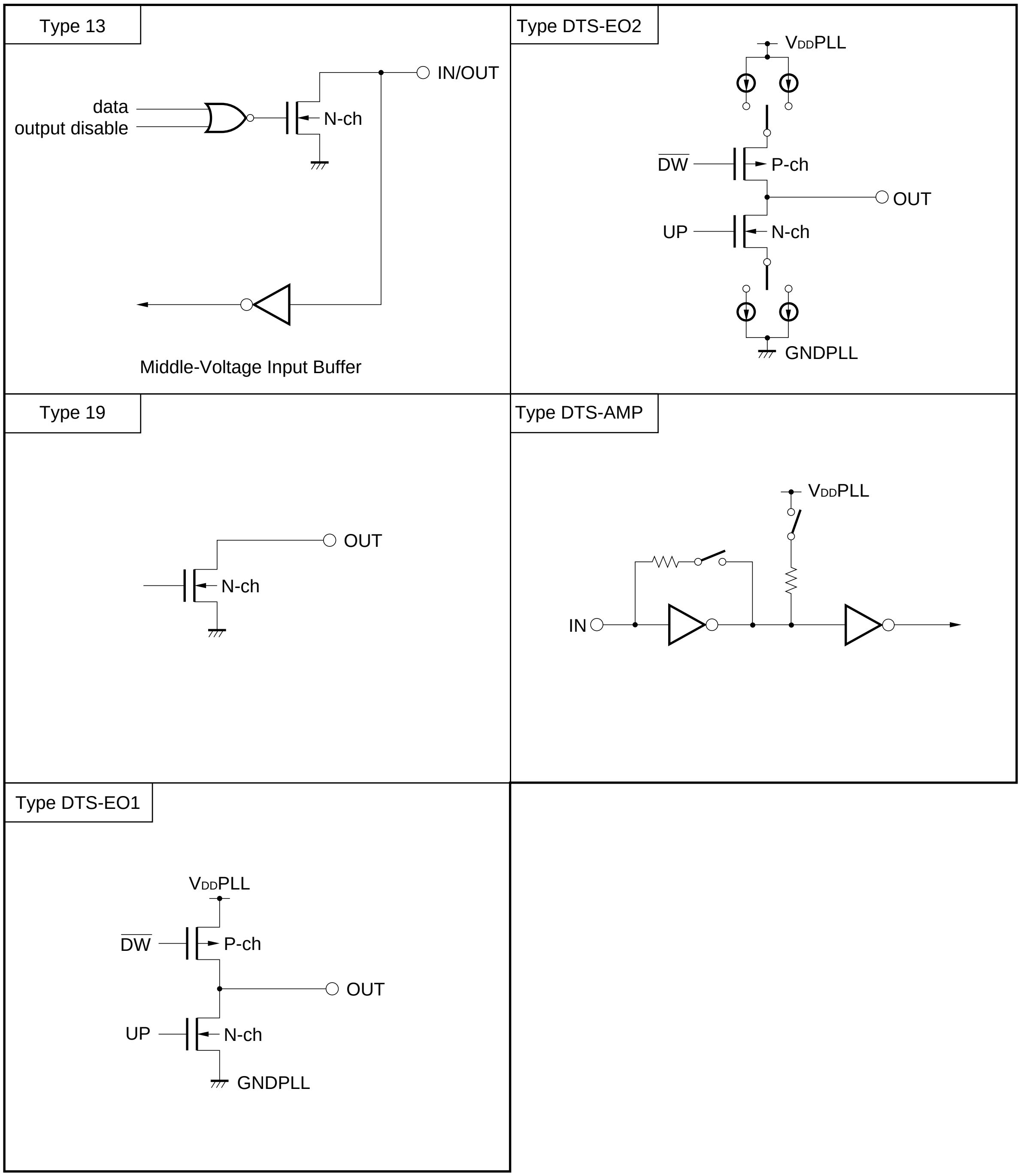
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	2	Input	Connected to GND or GNDPORT
P01/INTP1 to P06/INTP6	8	I/O	Set in general-purpose input port mode by software and individually connected to V_{DD}, V_{DD}PORT, GND, or GNDPORT via a resistor.
P10/ANI0 to P15/ANI5	11-A		
P20/SI1	8		
P21/SO1	5		
P22/$\overline{SCK1}$	8		
P23/STB	5		
P24/BUSY	8		
P25/SI0/SB0/SDA0 P26/SO0/SB1/SDA1 P27/$\overline{SCK0}$/SCL	10		
P30 to P32	5		
P33/TI1, P34/TI2	8		
P35 P36/BEEP P37	5		
P40 to P47	5-G		
P50 to P57	5		
P60 to P63	13		
P64 to P67	5		
P120 to P125			
P132/PWM0 to P134/PWM2	19	Output	Set to the low-level output by software and open
EO0	DTS-EO1		Open
EO1	DTS-EO2		
VCOL, VCOH	DTS-AMP	Input	Set to disabled status by software and open
AMIFC, FMIFC			
V_{PP}	—	—	Connected to GND or GNDPORT directly

Figure 1-1. Types of Pin Input/Output Circuits (1/2)



Remark All V_{DD} and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V_{DD}PORT and GNDPORT, respectively.

Figure 1-1. Types of Pin Input/Output Circuits (2/2)



Remark All V_{DD} and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V_{DD}PORT and GNDPORT, respectively.

2. PROM PROGRAMMING

The μPD178P018 has an internal 60-Kbyte PROM as a program memory. For programming, set the PROM programming mode with the V_{PP} and $\overline{\text{RESET}}$ pins. For the connection of unused pins, refer to **"PIN CONFIGURATIONS (TOP VIEW) (2) PROM programming mode."**

Caution Programs must be written in addresses 0000H to EFFFH (the last address EFFFH must be specified). They cannot be written by a PROM writer which cannot specify the write address.

2.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{\text{RESET}}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 2-1 when the $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{PGM}}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 2-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{\text{RESET}}$	V_{PP}	V_{DD}	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				x	H	H	High-impedance
				x	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	x	High-impedance
Standby				H	x	x	High-impedance

Remark x : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L and $\overline{OE}$ = L are set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD178P018s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, and $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H and $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L and $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X times ($X \leq 10$) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L and $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X times ($X \leq 10$) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, and $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly after the write.

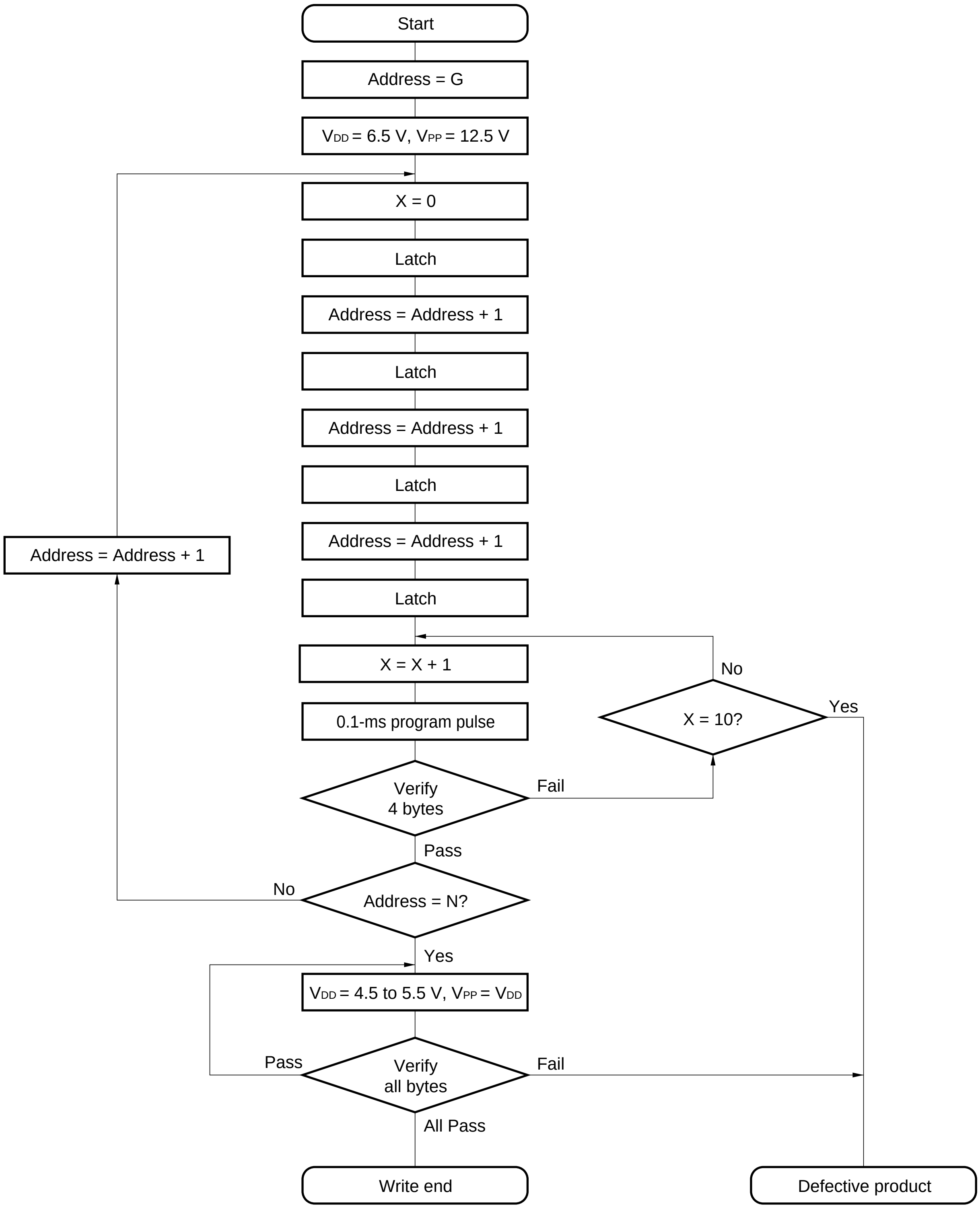
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin, and D0 to D7 pins of multiple μPD178P018s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

2.2 PROM Write Procedure

Figure 2-1. Page Program Mode Flow Chart



Remark G = Start address
N = Program last address

Figure 2-2. Page Program Mode Timing

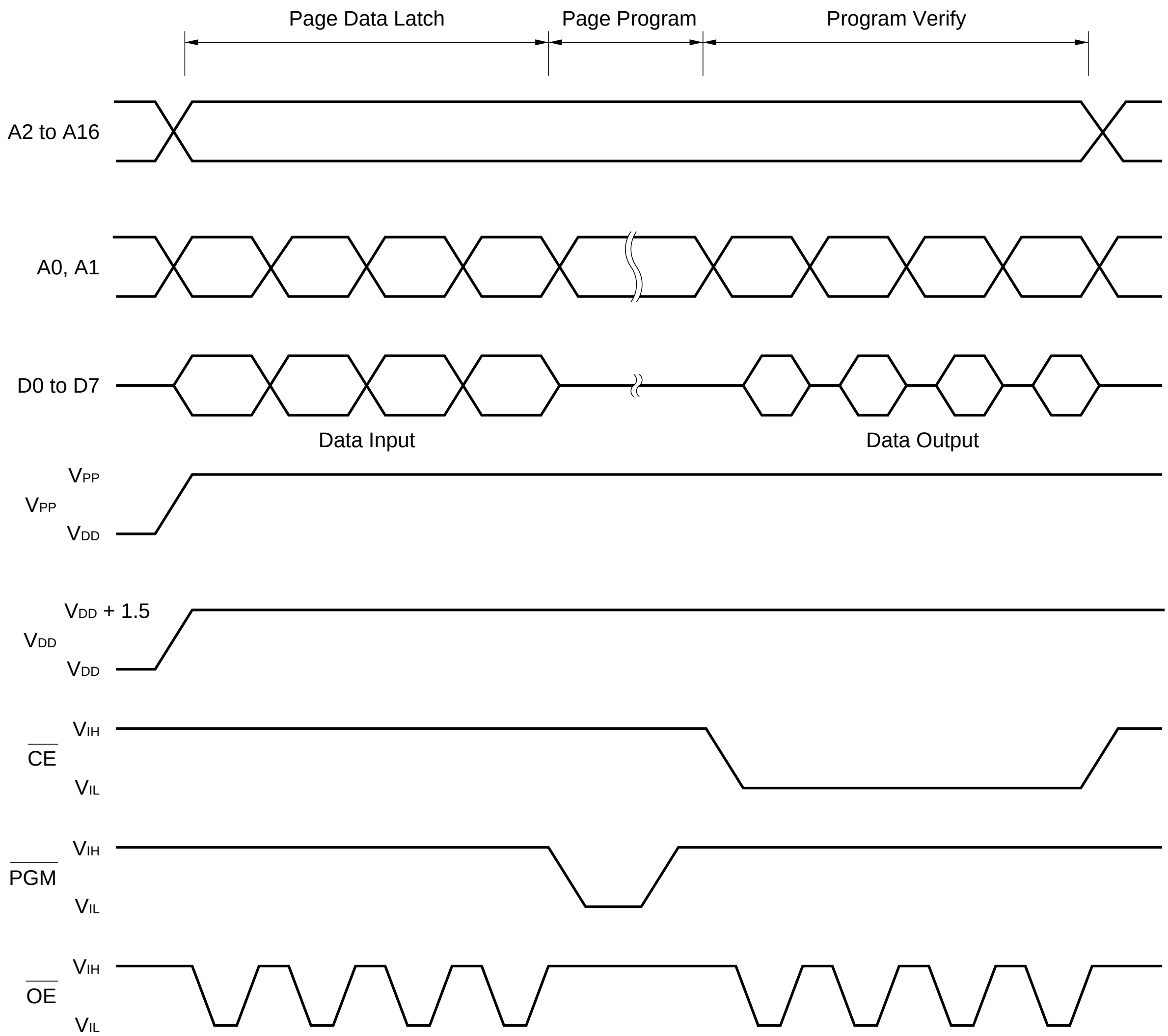
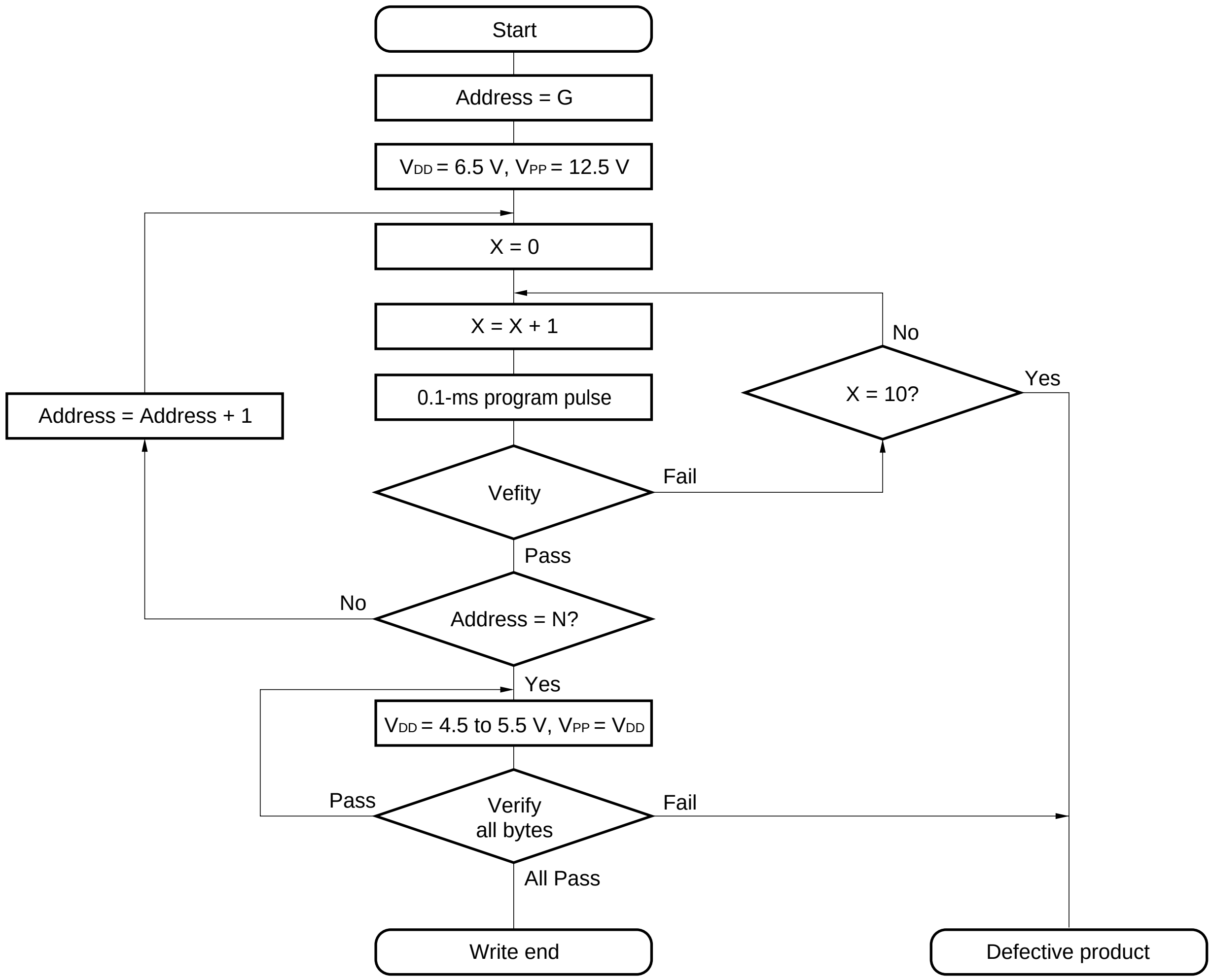
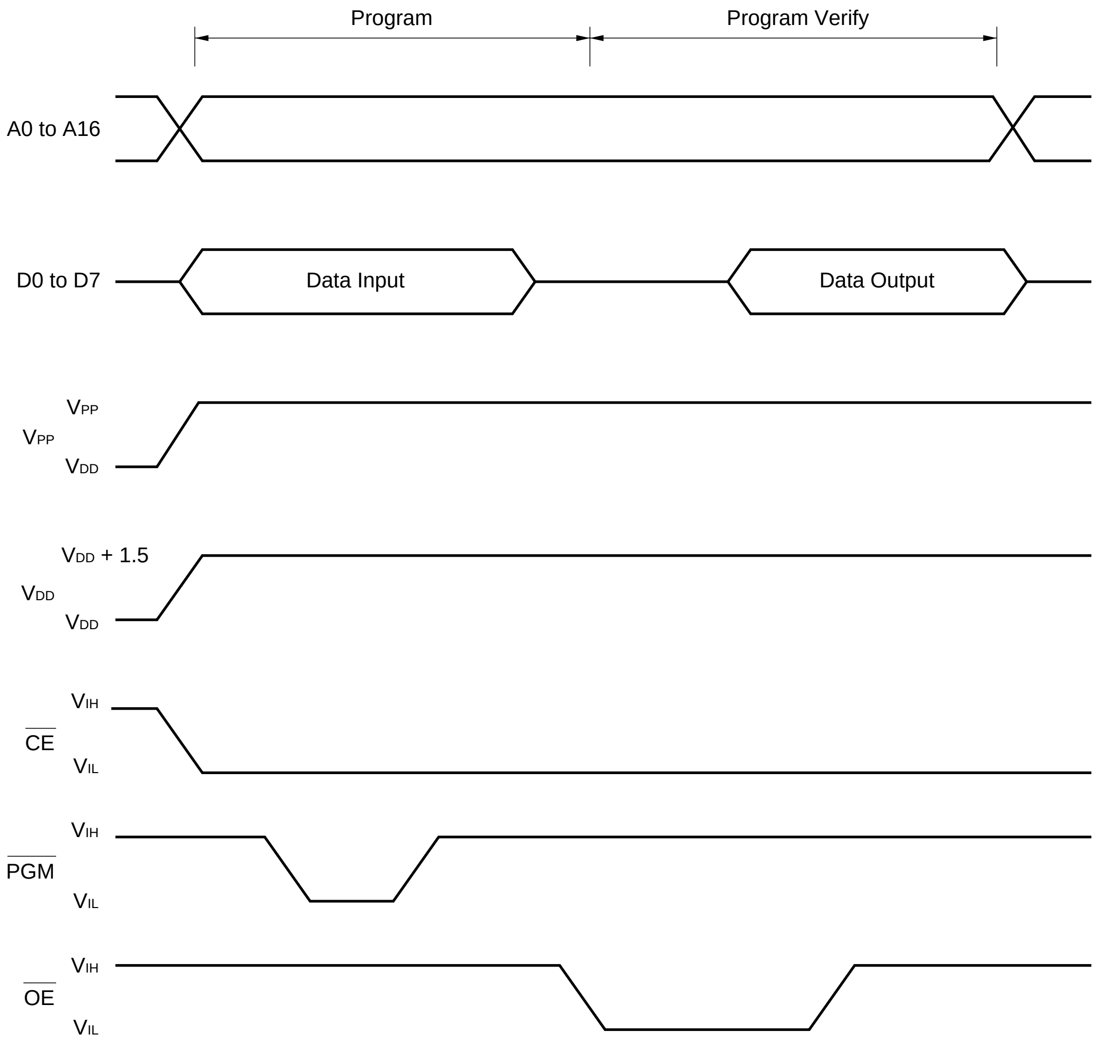


Figure 2-3. Byte Program Mode Flow Chart



Remark G = Start address
N = Program last address

Figure 2-4. Byte Program Mode Timing



Cautions

1. **V_{DD} should be applied before V_{PP}, and removed after V_{PP}.**
2. **V_{PP} must not exceed +13.5 V including overshoot.**
3. **Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.**

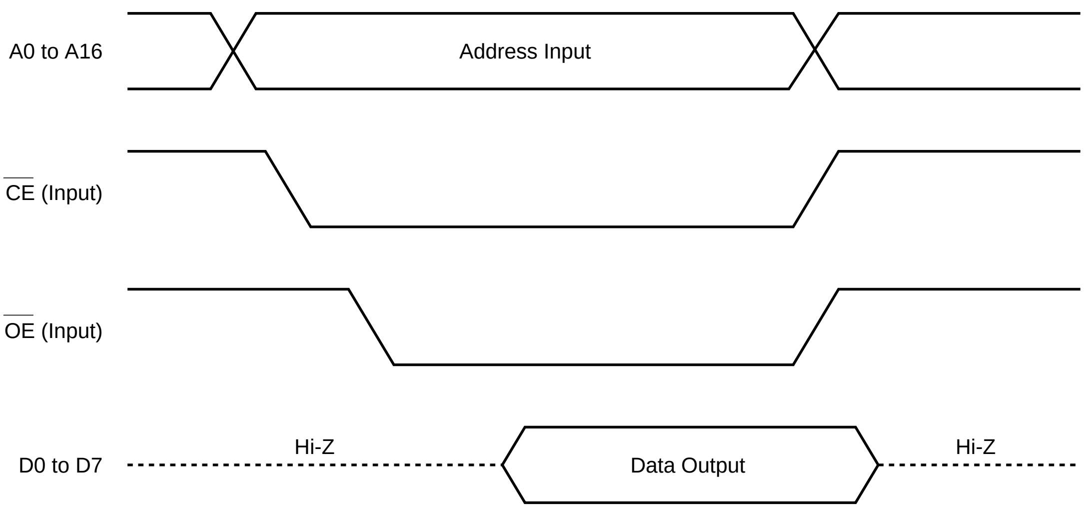
2.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **"PIN CONFIGURATIONS (TOP VIEW) (2) PROM programming mode".**
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of read data into the A0 to A16 pins.
(4) Read mode
(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 2-5.

Figure 2-5. PROM Read Timings



3. PROGRAM ERASURE (μPD178P018KK-T ONLY)

The μPD178P018KK-T is capable of erasing (FFH) the data written in a program memory and rewriting.

To erase the programmed data, expose the erasure window to light having a wavelength shorter than about 400 nm. Normally, irradiate ultraviolet rays of 254-nm wavelength. The amount of exposure required to completely erase the programmed data is as follows:

- UV intensity x erasure time: 30 W•s/cm^2 or more
- Erasure time: 40 min. or more (When a UV lamp of 12,000 μW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, soiled erasure window, etc.)

When erasing the contents of the data, set up the UV lamp within 2.5 cm from the erasure window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

4. OPAQUE FILM ON ERASURE WINDOW (μPD178P018KK-T ONLY)

To protect from an intentional erasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, cover the erasure window with an opaque film when EPROM contents erasure is not performed.

5. ONE-TIME PROM VERSION SCREENING

The one-time PROM version (μPD178P018GC-3B9) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125°C	24 hours

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Test Conditions			Ratings	Unit
Power supply voltage	V_{DD}				–0.3 to +7.0	V
	V_{PP}				–0.3 to +13.5	V
Input voltage	V_{I1}	Excluding P60 to P63			–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	N-ch open-drain		–0.3 to +16	V
	V_{I3}	A9	PROM programming mode		–0.3 to +13.5	V
Output voltage	V_O				–0.3 to V_{DD} + 0.3	V
Output withstand voltage	V_{BDS}	P132 to P134	N-ch open-drain		16	V
Analog input voltage	V_{AN}	P10 to P15	Analog input pin		–0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	1 pin			–10	mA
		P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P125 total			–15	mA
		P10 to P15, P20 to P27, P40 to P47, P50 to P55, P132 to P134 total			–15	mA
Output current low	I_{OL} Note	1 pin		Peak value	15	mA
				r.m.s. value	7.5	mA
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–65 to +150	°C

Note r.m.s. (root mean square) value should be calculated as follows: [r.m.s value] = [Peak value] × $\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of an alternate-function pin and a port pin are the same unless specified otherwise.

RECOMMENDED SUPPLY VOLTAGE RANGES (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD1}	During CPU operation and PLL operation.	4.5		5.5	V
	V_{DD2}	While the CPU is operating and the PLL is stopped. Cycle Time: $T_{CY} \geq 0.89\ \mu s$	3.5		5.5	V
	V_{DD3}	While the CPU is operating and the PLL is stopped. Cycle Time: $T_{CY} = 0.44\ \mu s$	4.5		5.5	V

Remark T_{CY}: Cycle Time (Minimum instruction execution time)

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(1/3)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P15, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch open-drain)		0.7V_{DD}		15	V
Input voltage low	V_{IL1}	P10 to P15, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125		0		0.3V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0		0.15V_{DD}	V
	V_{IL3}	P60 to P63	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
		(N-ch open-drain)	3.5 V ≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
Output voltage high	V_{OH1}		4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 5.5 V, I_{OH} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P120 to P125, P132 to P134	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, N-ch open-drain pulled-up (R = 1 KΩ)			0.2V_{DD}	V

Remark The characteristics of an alternate-function pin and a port pin are the same unless specified otherwise.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(2/3)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	P00 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125, $\overline{\text{RESET}}$	$V_{IN} = V_{DD}$			3	μA
	I_{LIH2}	P60 to P63	V_{IN} = 15 V			80	μA
Input leakage current low	I_{LIL1}	P00 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	P60 to P63				–3[Note]	μA
Output leakage current high	I_{LOH}	P132 to P134	V_{OUT} = 15 V			3	μA
Output leakage current low	I_{LOL}	P132 to P134	V_{OUT} = 0 V			–3	μA
Output off leak current	I_{LOF}	EO0, EO1	$V_{OUT} = V_{DD}$, V_{OUT} = 0 V			±1	μA

Note When an input instruction is executed, the low-level input leakage current for P60 to P63 becomes –200 μA (MAX.) only in one clock cycle (at no wait). It remains at –3 μA (MAX.) for other than an input instruction.

Remark The characteristics of an alternate-function pin and a port pin are the same unless specified otherwise.

REFERENCE CHARACTERISTICS (T_A = 25°C, V_{DD} = 5 V)

(1/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output current high	I_{OH1}	EO0	$V_{OUT} = V_{DD}$ – 1 V		–4		mA
		EO1 (EOCON0 = 1)			–6		mA
		EO1 (EOCON0 = 0)			–2		mA
Output current low	I_{OL1}	EO0	V_{OUT} = 1 V		6		mA
		EO1 (EOCON0 = 1)			8		mA
		EO1 (EOCON0 = 0)			3		mA

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(3/3)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	While the CPU is operating and the PLL is stopped	T_{CY} = 0.89 μs[Note 2]		2.5	15	mA
	I_{DD2}	f_X = 4.5-MHz operation	T_{CY} = 0.44 μs[Note 3] V_{DD} = 4.5 to 5.5 V		4.0	27	mA
	I_{DD3}	While the CPU is operating and the PLL is stopped HALT Mode.	T_{CY} = 0.89 μs[Note 2]		1	4	mA
	I_{DD4}	Pin X1 sine wave input V_{IN} = V_{DD} f_X = 4.5-MHz operation	T_{CY} = 0.44 μs[Note 3] V_{DD} = 4.5 to 5.5 V		1.6	6	mA
Data hold power supply voltage	V_{DDR1}	When the crystal is oscillating	T_{CY} = 0.44 μs	4.5		5.5	V
	V_{DDR2}		T_{CY} = 0.89 μs	3.5		5.5	V
	V_{DDR3}	When the crystal oscillation is stopped When power off by Power On Clear is detected		2.7		5.5	V
Data hold power supply current	I_{DDR1}	While the crystal oscillation is stopped	T_A = 25°C, V_{DD} = 5V		2	4	μA
	I_{DDR2}				2	30	μA

Notes 1. The port current is not included.

2. When the Processor Clock Control register (PCC) is set at 00H, and the Oscillation Mode Select register (OSMS) is set to 00H.

3. When PCC is set to 00H and OSMS is set to 01H.

Remarks 1. T_{CY}: Cycle Time (Minimum instruction execution time)

2. fx: System clock oscillation frequency.

REFERENCE CHARACTERISTICS (T_A = 25°C, V_{DD} = 5 V)

(2/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD5}	During CPU operation and PLL operation. VCOH pin sine wave input f_{IN} = 130 MHz, V_{IN} = 0.15 V_{p-p}	T_{CY} = 0.44 μs[Note]		7		mA

Note When the Processor Clock Control register (PCC) is set to 00H, and the Oscillation Mode Select register (OSMS) is set to 01H.

Remark T_{CY}: Cycle Time (Minimum instruction execution time)

AC CHARACTERISTICS

(1) BASIC OPERATION (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	$f_{XX} = f_X/2$ Note 1, f_X = 4.5-MHz operation		0.89		14.22	μs
		$f_{XX} = f_X$ Note 2, f_X = 4.5-MHz operation	$4.5 \le V_{DD} \le 5.5$ V	0.44		7.11	μs
			$3.5 \le V_{DD} < 4.5$ V	0.89		7.11	μs
TI1, TI2 input frequency	f_{TI}	$4.5 \le V_{DD} \le 5.5$ V		0		4.5	MHz
		$3.5\ V \le V_{DD} < 4.5$ V		0		275	kHz
TI1, TI2 input high/ low-level width	t_{TIH}, t_{TIL}	$4.5 \le V_{DD} \le 5.5$ V		111			ns
		$3.5\ V \le V_{DD} < 4.5$ V		1.8			μs
Interrupt input high/ low-level width	T_{INTH}, T_{INTL}	INTP0		$8/f_{sam}$ Note 3			μs
		INTP1 to INTP6		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. When the Oscillation Mode Selection register (OSMS) is set to 00H.

2. When OSMS is set to 01H.

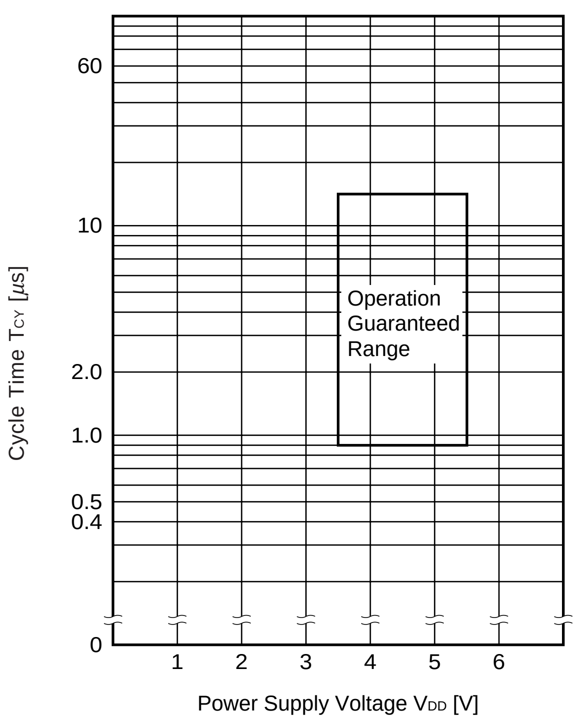
3. In combination with bits 0 (SCS0) and 1 (SCS1) of the Sampling Clock Select register (SCS), selection of f_{sam} is possible among $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, and $f_{XX}/128$ (when N = 0 to 4).

Remarks 1. f_{XX}: System clock frequency (f_X or $f_X/2$)

2. f_X: System clock oscillation frequency

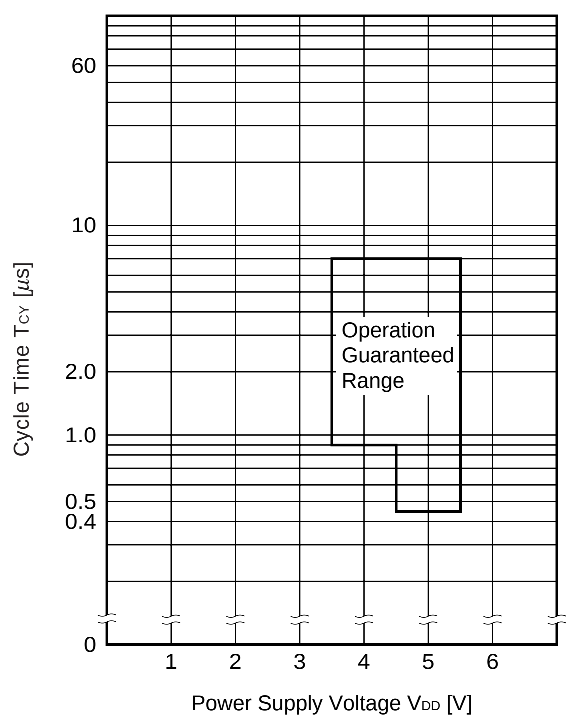
T_{CY} vs V_{DD}

(when system clock f_{XX} is operating at $f_X/2$)



T_{CY} vs V_{DD}

(when system clock f_{XX} is operating at f_X)



(2) SERIAL INTERFACE (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1},	4.5 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 50			ns
	t_{KL1}	3.5 V ≤ V_{DD} < 4.5 V	t_{KCY1}/2 – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		3.5 V ≤ V_{DD} < 4.5 V	150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF Note			300	ns

Note C is the load capacitance of the SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2},	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
	t_{KL2}	3.5 V ≤ V_{DD} < 4.5 V	800			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF Note			300	ns
$\overline{SCK0}$ rising or falling edge time	t_{R2}, t_{F2}				1000	ns

Note C is the load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	$4.5\ V \le V_{DD} \le 5.5\ V$		800			ns
		$3.5\ V \le V_{DD} < 4.5\ V$		3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3},	$4.5\ V \le V_{DD} \le 5.5\ V$		$t_{KCY3}/2 - 50$			ns
	t_{KL3}	$3.5\ V \le V_{DD} < 4.5\ V$		$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	$4.5\ V \le V_{DD} \le 5.5\ V$		100			ns
		$3.5\ V \le V_{DD} < 4.5\ V$		300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ	$4.5\ V \le V_{DD} \le 5.5\ V$	0		250	ns
		C = 100 pF[Note]	$3.5\ V \le V_{DD} < 4.5\ V$	0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(iv) SBI mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	$4.5\ V \le V_{DD} \le 5.5\ V$		800			ns
		$3.5\ V \le V_{DD} < 4.5\ V$		3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4},	$4.5\ V \le V_{DD} \le 5.5\ V$		400			ns
	t_{KL4}	$3.5\ V \le V_{DD} < 4.5\ V$		1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	$4.5\ V \le V_{DD} \le 5.5\ V$		100			ns
		$3.5\ V \le V_{DD} < 4.5\ V$		300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ	$4.5\ V \le V_{DD} \le 5.5\ V$	0		300	ns
		C = 100 pF[Note]	$3.5\ V \le V_{DD} < 4.5\ V$	0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rising or falling edge time	t_{R4}, t_{F4}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ		1600			ns
$\overline{SCK0}$ high-level width	t_{KH5}	C = 100 pF[Note]		$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		$4.5 V \le V_{DD} \le 5.5 V$	$t_{KCY5}/2 - 50$			ns
			$3.5 V \le V_{DD} < 4.5 V$	$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		$4.5 V \le V_{DD} \le 5.5 V$	300			ns
			$3.5 V \le V_{DD} < 4.5 V$	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ	$4.5 V \le V_{DD} \le 5.5 V$	0		300	ns
		C = 100 pF[Note]	$3.5 V \le V_{DD} < 4.5 V$	0		500	ns
$\overline{SCK0}$ at rising or falling edge time	t_{R6}, t_{F6}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(vii) I²C bus mode (SCL ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY7}	R = 1 kΩ		10			μs
SCL high-level width	t_{KH7}	C = 100 pF Note		t_{KCY7} – 160			ns
SCL low-level width	t_{KL7}			t_{KCY7} – 50			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK7}			200			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI7}			0			ns
SDA0, SDA1 output delay time (from SCL↓)	t_{KSO7}		4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			3.5 V ≤ V_{DD} < 4.5 V	0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the SCL, SDA0, and SDA1 output lines.

(viii) I²C bus mode (SCL ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY8}			1000			ns
SCL high-/low-level width	t_{KH8}, t_{KL8}			400			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK8}			200			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI8}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO8}	R = 1 kΩ	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
		C = 100 pF Note	3.5 V ≤ V_{DD} < 4.5 V	0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns
SCL rising or falling edge time	t_{R8}, t_{F8}					1000	ns

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output lines.

(b) **Serial interface channel 1**

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9},	4.5 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY9}/2 - 50$			ns
	t_{KL9}	3.5 V ≤ V_{DD} < 4.5 V	$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		3.5 V ≤ V_{DD} < 4.5 V	150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time (from $\overline{SCK1}$↓)	t_{KSO9}	C = 100 pF Note			300	ns

Note C is the load capacitance of the SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10},	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
	t_{KL10}	3.5 V ≤ V_{DD} < 4.5 V	800			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}		400			ns
SO1 output delay time (from $\overline{SCK1}$↓)	t_{KSO10}	C = 100 pF Note			300	ns
$\overline{SCK1}$ rising or falling edge time	t_{R10}, t_{F10}				1000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY11}	$4.5\ V \le V_{DD} \le 5.5\ V$	800			ns
		$3.5\ V \le V_{DD} < 4.5\ V$	1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH11}, t_{KL11}	$4.5\ V \le V_{DD} \le 5.5\ V$	$t_{KCY11}/2 - 50$			ns
		$3.5\ V \le V_{DD} < 4.5\ V$	$t_{KCY11}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK11}	$4.5\ V \le V_{DD} \le 5.5\ V$	100			ns
		$3.5\ V \le V_{DD} < 4.5\ V$	150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI11}		400			ns
SO1 output delay time (from $\overline{SCK1}\downarrow$)	t_{KSO11}	C = 100 pF[Note]			300	ns
STB$\uparrow$ from $\overline{SCK1}\uparrow$	t_{SBD}		$t_{KCY11}/2 - 100$		$t_{KCY11}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY11} - 30$		$t_{KCY11} + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	$4.5\ V \le V_{DD} \le 5.5\ V$	100			ns
		$3.5\ V \le V_{DD} < 4.5\ V$	150			ns
$\overline{SCK1}\downarrow$ from busy inactive	t_{SPS}				$2t_{KCY11}$	ns

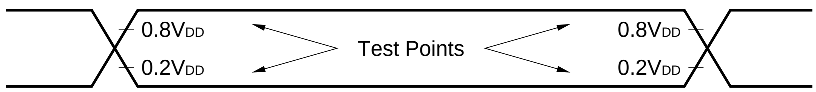
Note C is the load capacitance of the SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... external clock input)

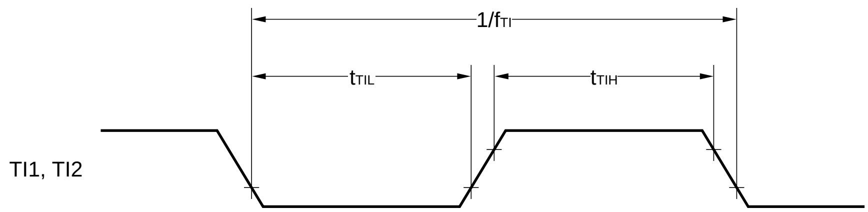
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY12}	$4.5\ V \le V_{DD} \le 5.5\ V$	800			ns
		$3.5\ V \le V_{DD} < 4.5\ V$	1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH12}, t_{KL12}	$4.5\ V \le V_{DD} \le 5.5\ V$	400			ns
		$3.5\ V \le V_{DD} < 4.5\ V$	800			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK12}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI12}		400			ns
SO1 output delay time (from $\overline{SCK1}\downarrow$)	t_{KSO12}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rising or falling edge time	t_{R12}, t_{F12}				1000	ns

Note C is the load capacitance of the SO1 output line.

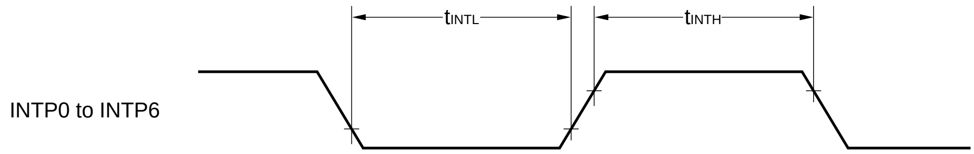
AC Timing Test Point (Excluding X1 Input)



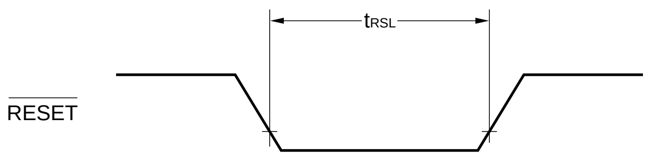
TI Timing



Interrupt Input Timing

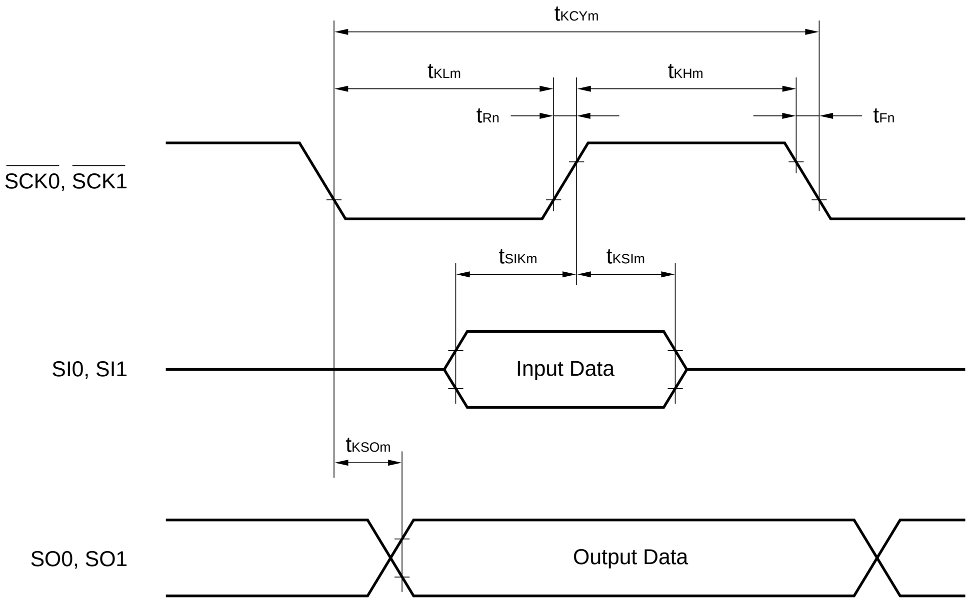


$\overline{\text{RESET}}$ Input Timing



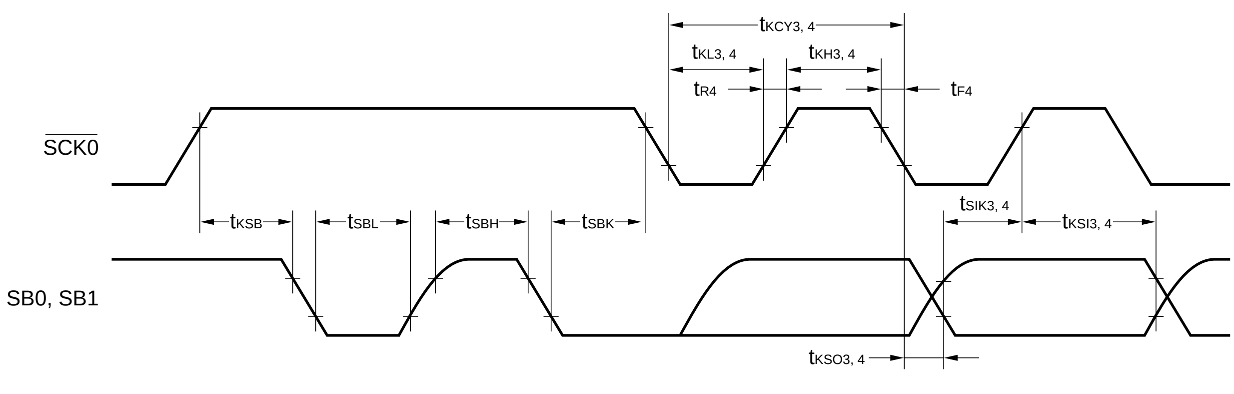
Serial Transfer Timing

3-Wire Serial I/O Mode:

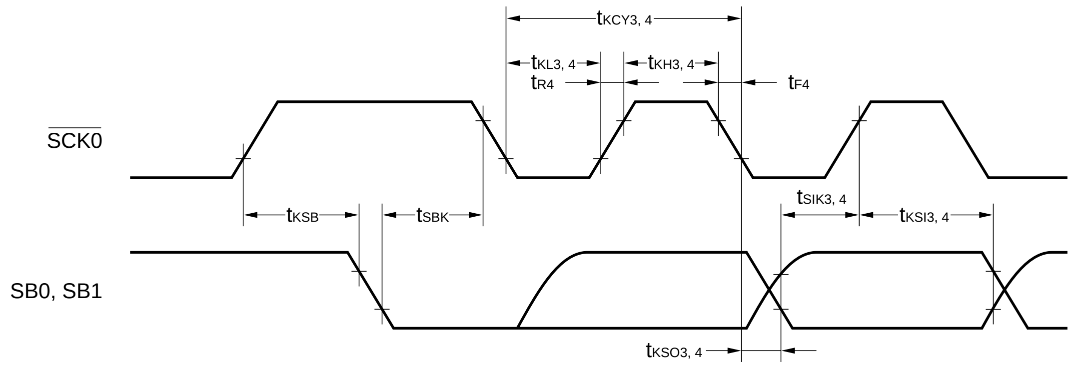


Remark m = 1, 2, 9, 10
n = 2, 10

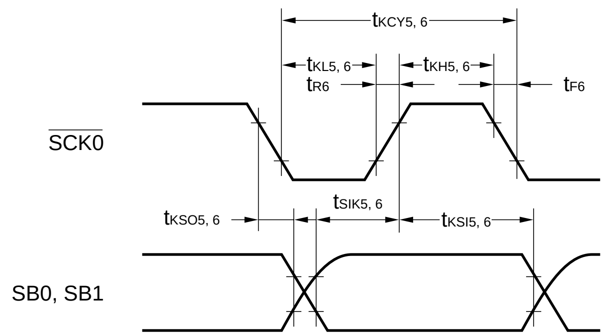
SBI Mode (Bus Release Signal Transfer):



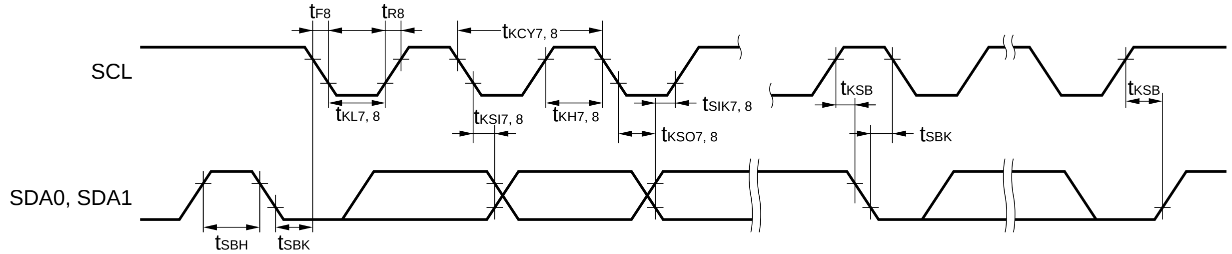
SBI Mode (Command Signal Transfer):



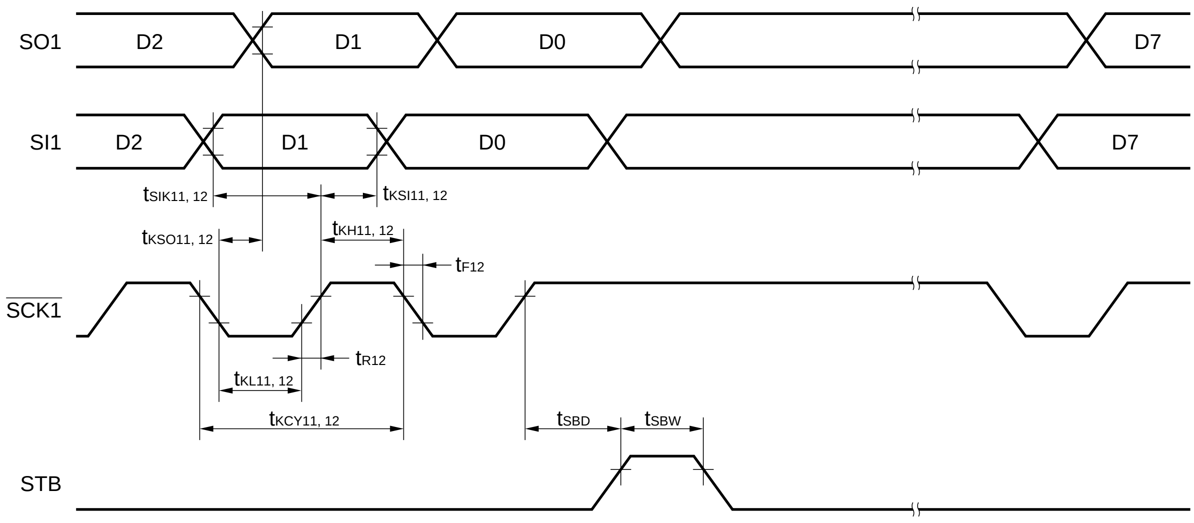
2-Wire Serial I/O Mode:



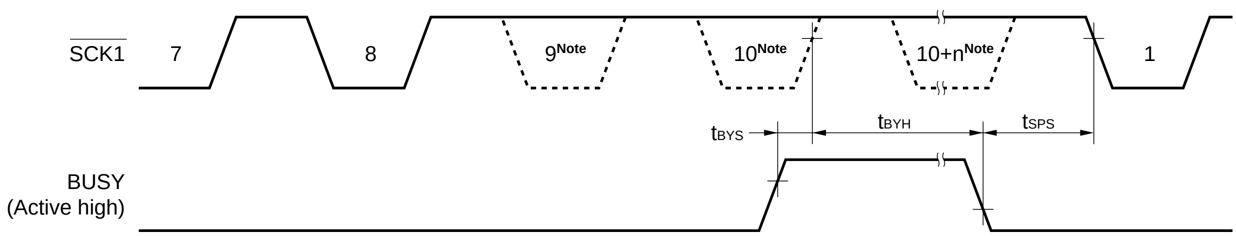
I²C Bus Mode:



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function:



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function (Busy Processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Conversion total error					±3.0	LSB
Conversion time	t_{CONV}		22.2		44.4	μs
Sampling time	t_{SAMP}		$15/f_{XX}$			μs
Analog input voltage	V_{IAN}		0		V_{DD}	V

Remarks 1. f_{XX}: System clock frequency (f_X/2)

2. f_X: System clock oscillation frequency

PLL CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN1}	VCOL Pin MF Mode Sine wave input V_{IN} = 0.1 $V_{p\text{-}p}$	0.5		3	MHz
	f_{IN2}	VCOL Pin HF Mode Sine wave input V_{IN} = 0.2 $V_{p\text{-}p}$	9		55	MHz
	f_{IN3}	VCOH Pin VHF Mode Sine wave input V_{IN} = 0.15 $V_{p\text{-}p}$	60		160	MHz

IFC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN4}	AMIFC Pin AMIF Count Mode Sine wave input V_{IN} = 0.1 $V_{p\text{-}p}$ Note	0.4		0.5	MHz
	f_{IN5}	FMIFC Pin FMIF Count Mode Sine wave input V_{IN} = 0.1 $V_{p\text{-}p}$ Note	10		11	MHz
	f_{IN6}	FMIFC Pin AMIF Count Mode Sine wave input V_{IN} = 0.1 $V_{p\text{-}p}$ Note	0.4		0.5	MHz

Note The condition of a sine wave input of V_{IN} = 0.1 $V_{p\text{-}p}$ is the standard value for operation of this device during stand-alone operation, so in consideration of the effect of noise, it is recommended that operation be at an input amplitude condition of V_{IN} = 0.15 $V_{p\text{-}p}$.

PROM PROGRAMMING CHARACTERISTICS

DC CHARACTERISTICS

(1) PROM Write Mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		$0.3V_{DD}$	V
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM} = V_{IL}$			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		$0.3V_{DD}$	V
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	$0 \leq V_{OUT} \leq V_{DD}$, $\overline{OE} = V_{IH}$	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	$V_{PP} = V_{DD}$			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$			50	mA

Note Corresponding μPD27C1001A symbol.

AC CHARACTERISTICS

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}$ ↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}$ ↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}$ ↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}$ ↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}$ ↑	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}$ ↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}$ ↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}$ ↓	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}$ ↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ set time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}$ ↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}$ ↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}$ ↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}$ ↑	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}$ ↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}$ ↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}$ ↓	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol.

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

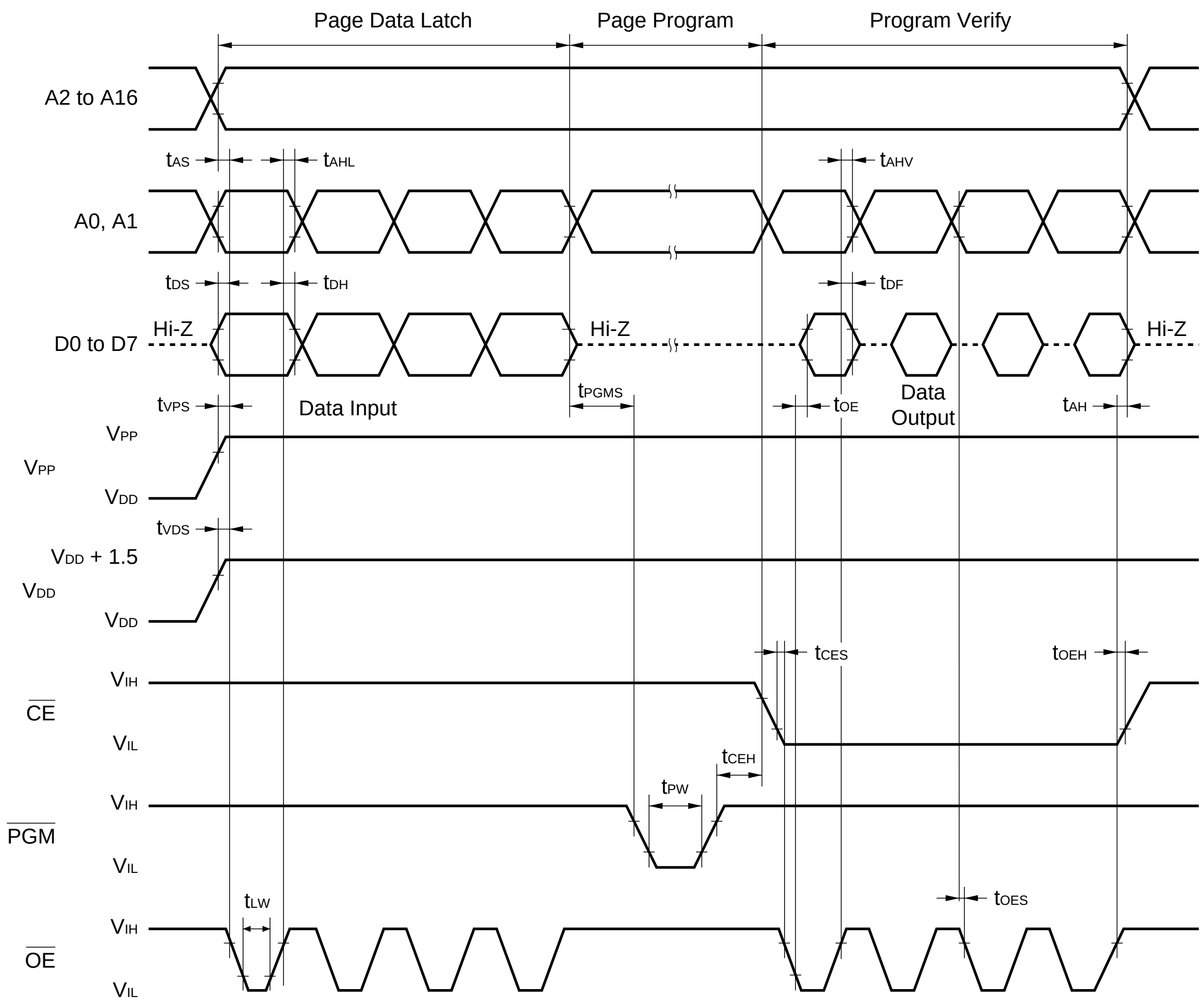
Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			800	ns
Data output delay time $\overline{CE}$ ↓	t_{CE}	t_{CE}	$\overline{OE} = V_{IL}$			800	ns
Data output delay time $\overline{OE}$ ↓	t_{OE}	t_{OE}	$\overline{CE} = V_{IL}$			200	ns
Data output float delay time from $\overline{OE}$ ↑	t_{DF}	t_{DF}	$\overline{CE} = V_{IL}$	0		60	ns
Data hold time to address	t_{OH}	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note Corresponding μPD27C1001A symbol.

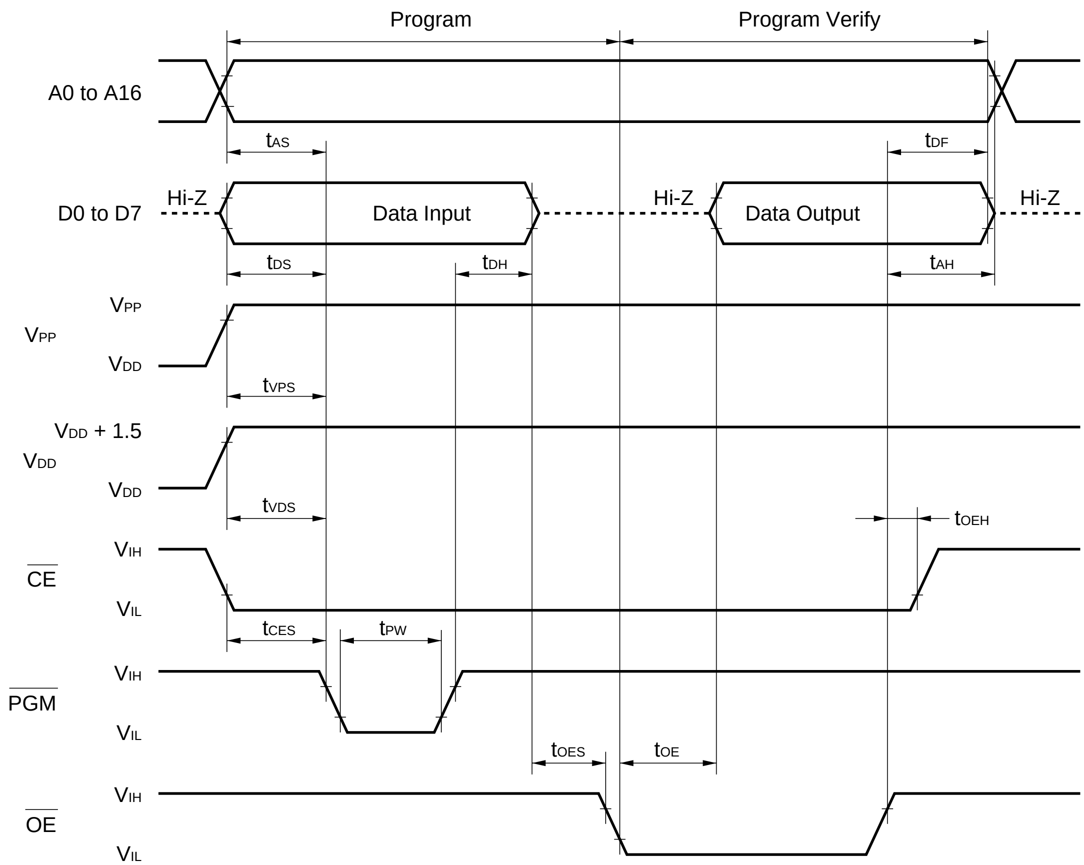
(3) PROM Programming Mode Setting (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (page program mode)



PROM Write Mode Timing (byte program mode)

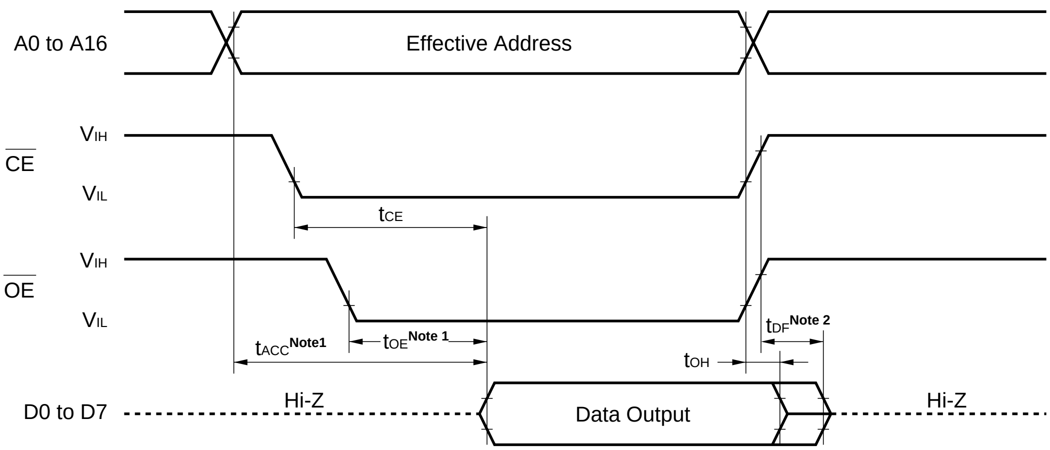


Cautions 1. VDD should be applied before VPP, and removed after VPP.

2. VPP must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while + 12.5 V is being applied to VPP.

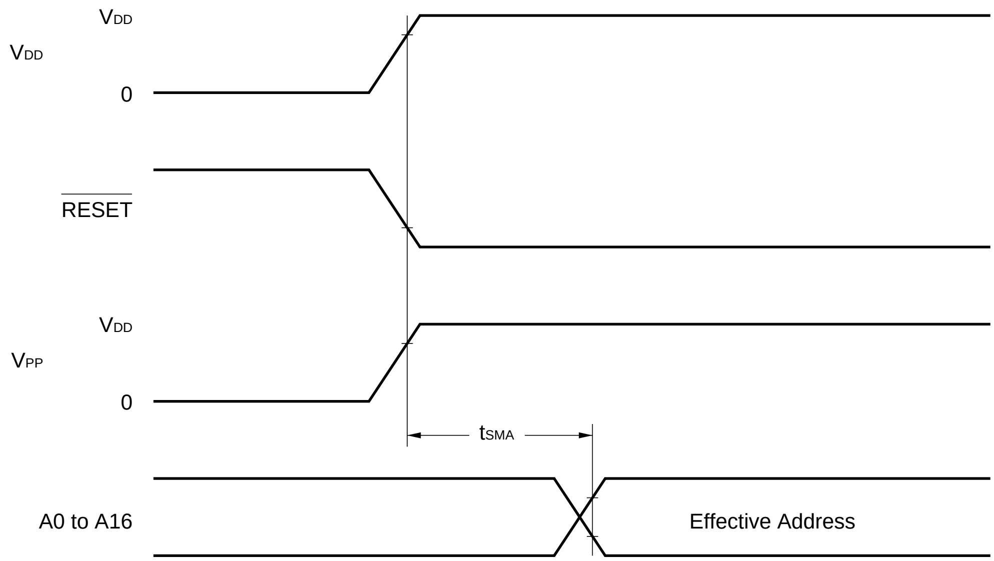
PROM Read Mode Timing



Notes 1. If you want to read within the range of tACC, make the $\overline{\text{OE}}$ input delay time from the fall of $\overline{\text{CE}}$ a maximum of tACC – tOE.

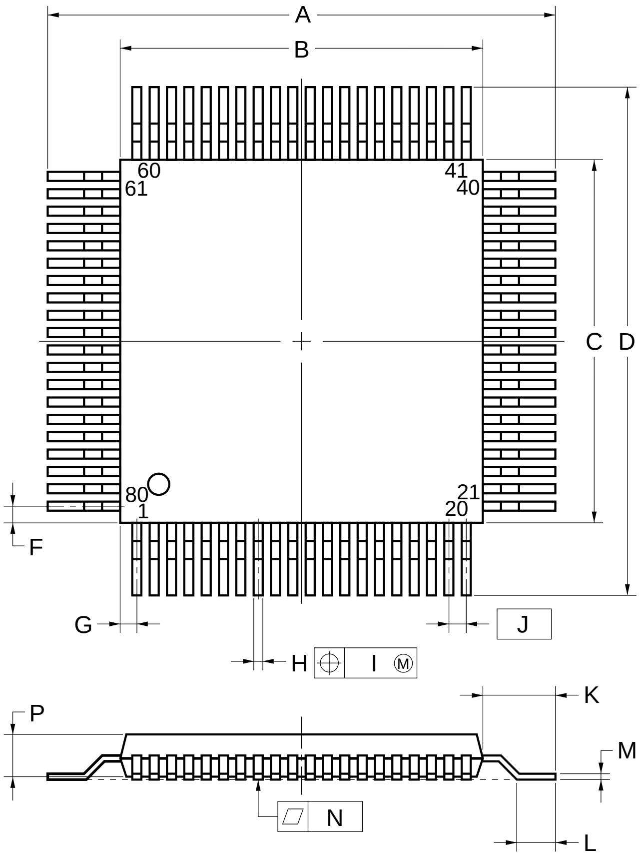
2. tDF is the time from when either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ first reaches VIH.

PROM Programming Mode Setting Timing

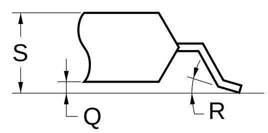


7. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



detail of lead end



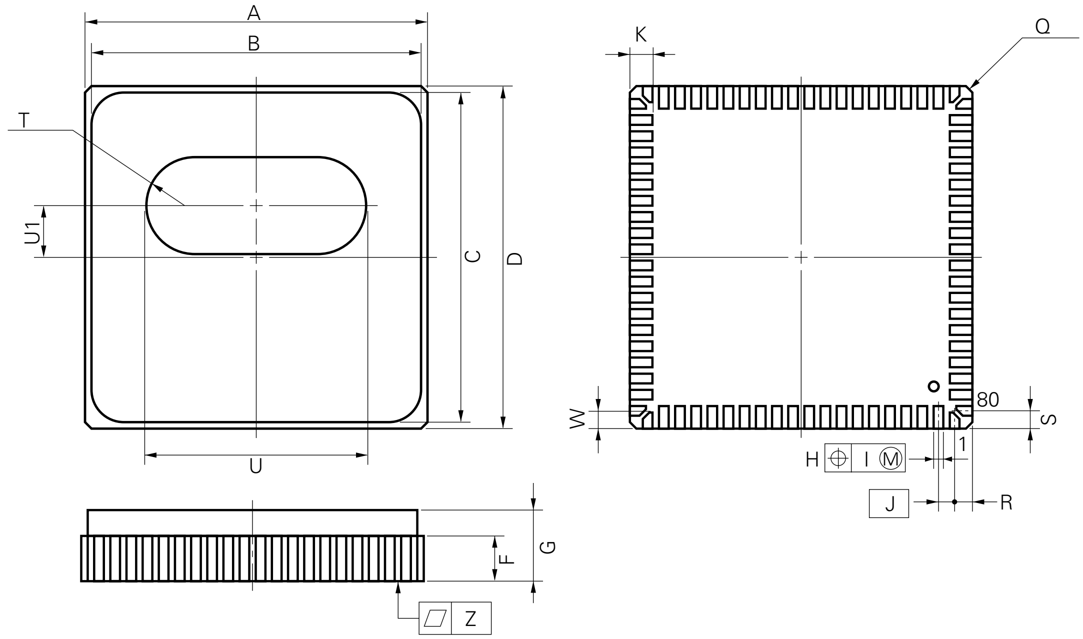
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

80 PIN CERAMIC WQFN



X80KW-65A-1

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	13.6	0.535
C	13.6	0.535
D	14.0±0.2	0.551±0.008
F	1.84	0.072
G	3.6 MAX.	0.142 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65 (T.P.)	0.024 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C 0.3	C 0.012
R	0.825	0.032
S	0.825	0.032
T	R 2.0	R 0.079
U	9.0	0.354
U1	2.1	0.083
W	0.75±0.15	$0.030^{+0.006}_{-0.007}$
Z	0.10	0.004

8. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 8-1. Surface Mounting Type Soldering Conditions

μPD178P018GC-3B9: 80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Three times max. Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125°C afterwards) (Points to note) Do not bake components in any packaging except heat-resistant trays, that is components in magazines, tape, or non-heat-resistant trays.	IR35-207-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Three times max. Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125°C afterwards) (Points to note) Do not bake components in any packaging except heat-resistant trays, that is components in magazines, tape, or non-heat-resistant trays.	VP15-207-3
Wave soldering	Solder bath temperature : 260°C max., Duration : 10 sec. max., Number of times : once, Preheating temperature : 120°C max. (package surface temperature) Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125°C afterwards) (Points to note) Do not bake components in any packaging except heat-resistant trays, that is components in magazines, tape, or non-heat-resistant trays.	WS60-207-1
Partial heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per pin row)	—

Note Exposure limit before soldering after the dry pack package is opened. Storage conditions: 25°C and relative humidity at 65% or less.

Caution Do not use different soldering method together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD178P018 Subseries.

LANGUAGE PROCESSING SOFTWARE

RA78K/0 Notes 1, 2, 3, 4	78K/0 Series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 Series common C compiler package
DF178018 Notes 1, 2, 3, 4	μPD178018 Subseries common device file
CC78K/0-L Notes 1, 2, 3, 4	78K/0 Series common C compiler library source file

PROM WRITING TOOLS

PG-1500	PROM writer
PG-178P018GC	Program writer adapters connected to a PG-1500
PA-178P018KK-T	
PG-1500 controller Notes 1, 2	PG-1500 control program

DEBUGGING TOOLS

IE-78000-R	In-circuit emulator common to 78K/0 Series
IE-78000-R-A	In-circuit emulator common to 78K/0 Series (for the integrated debugger)
IE-78000-R-BK	Break board common to 78K/0 Series
IE-178018-R-EM	Emulation board common to μPD178018 Subseries
EP-78230GC-R	Emulation probe common to μPD78234 Subseries
EV-9200GC-80	Socket for mounting on target system board created for 80-pin plastic QFP (GC-3B9 type)
EV-9900	Jig used when removing the μPD178P018KK-T from the EV-9200GC-80.
SM78K0 Notes 5, 6, 7	78K/0 series common system simulator
ID78K0 Notes 4, 5, 6, 7	Integrated debugger for IE-78000-R-A
SD78K/0 Notes 1, 2	IE-78000-R screen debugger
DF178018 Notes 1, 2, 4, 5, 6, 7	μPD178018 Subseries device file

REAL-TIME OS

RX78K/0 Notes 1, 2, 3, 4	78K/0 Series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 Series OS

Notes
1. PC-9800 Series (MS-DOS™) based
2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based

FUZZY INFERENCE DEVELOPMENT SUPPORT SYSTEM

FE9000[Note 1]/FE9200[Note 2]	Fuzzy knowledge data creation tool
FT9080[Note 1]/FT9085[Note 3]	Translator
FI78K0[Notes 1, 3]	Fuzzy inference module
FD78K0[Notes 1, 3]	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS) based

2. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based

3. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS) based

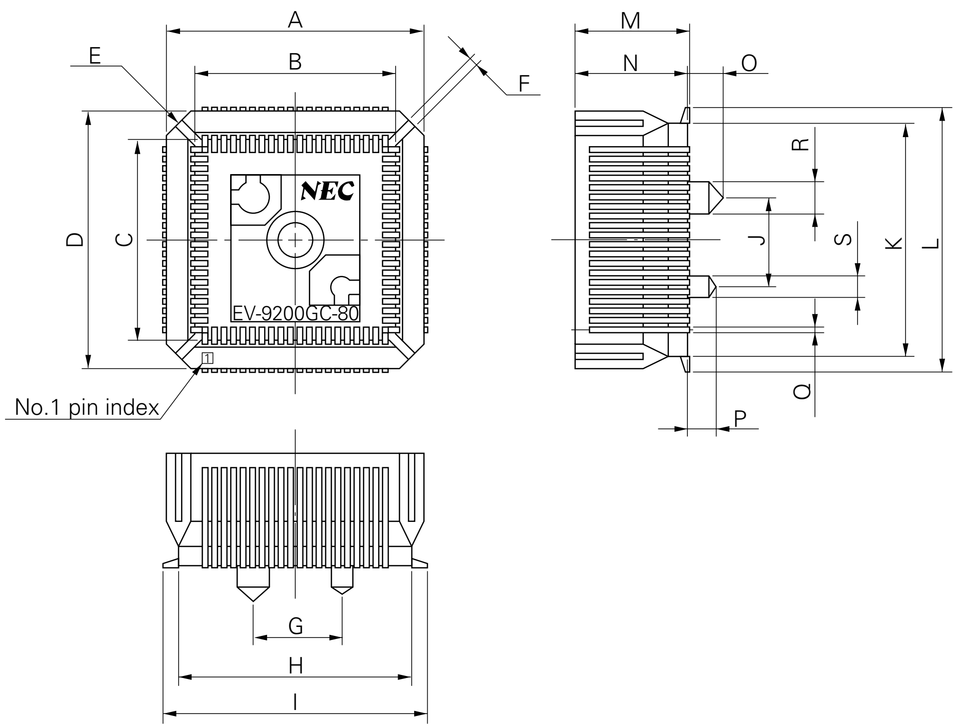
Remarks 1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.

2. The RA78K/0, CC78K/0, SD78K/0, ID78K/0, SM78K/0, and RX78K/0 are used in combination with the DF178018.

CONVERSION SOCKET DRAWING AND RECOMMENDED FOOTPRINT

Figure A-1. Drawing of EV-9200GC-80 (for Reference only)

Based on EV-9200GC-80
(1) Package drawing (in mm)

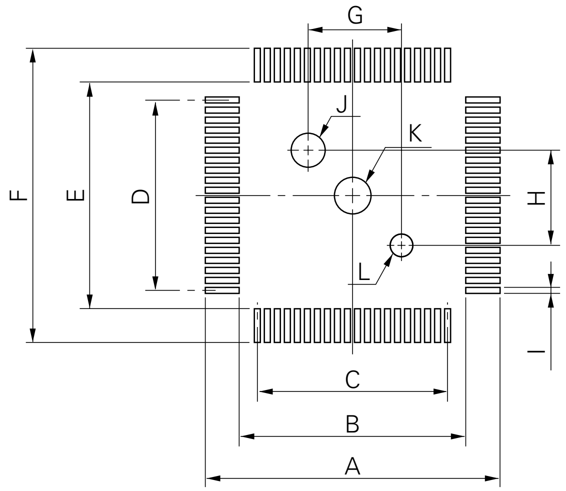


EV-9200GC-80-G1E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. Recommended Footprint of EV-9200GC-80 (for Reference only)

Based on EV-9200GC-80
(2) Pad drawing (in mm)



EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
D	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0±0.05	$0.236^{+0.003}_{-0.002}$
H	6.0±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	φ2.3	φ0.091
L	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX B. RELATED DOCUMENTS

DEVICE DOCUMENTS

Title		Document No. (Japanese)	Document No. (English)
μPD178018 Subseries User's Manual		U11410J	U11410E
78K/0 Series User's Manual—Instruction		U12326J	IEU-1372
78K/0 Series Instruction Set		U10904J	—
78K/0 Series Instruction Table		U10903J	—
μPD178018 Subseries Special Function Register Table		To be prepared	—
78K/0 Series Application Note	Basics (II)	U10121J	U10121E

Development Tool Documents (User's Manual)

Title		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	—
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		U11376J	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-178018-R-EM		U10668J	U10668E
EP-78230		EEU-985	EEU-1515
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	U10539E
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	U11279E

Caution The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.

RELATED DOCUMENTS FOR EMBEDDED SOFTWARE (USER'S MANUAL)

Title		Document No. (Japanese)	Document No. (English)
78K/0 Series Realtime OS	Basics	U11537J	—
	Installation	U11536J	—
	Technical	U11538J	—
78K/0 Series OS MX78K0	Basics	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System—Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System—Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System —Fuzzy Inference Debugger		EEU-921	EEU-1458

OTHER DOCUMENTS

Title	Document No. (Japanese)	Document No. (English)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Guides on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability and Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Device Quality Assurance Guide	C11893J	C11893E
Microcomputer-related Product Guide (Products by other Manufacturers)	U11416J	—

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[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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