NEC

MOS INTEGRATED CIRCUIT

μPD31172

VRC4172™
COMPANION CHIP FOR VR4121™

DESCRIPTION

The μPD31172 (commercial name: VRC4172) is a companion chip designed for NEC's μPD30121 microprocessor (commercial name: VR4121).

The VRC4172 has the following functions available on chip: a USB host controller, an IEEE1284 parallel controller, a 16550 serial controller, a PS/2 controller, general-purpose ports (GPIO), programmable chip select (PCS), and a PWM controller (a duty modulated light pulse generation function for LCD backlighting).

The VRC4172 can be directly connected to the VR4121, allowing a reduction in the man-hours required for development of a Windows™ CE system.

Detailed function descriptions are provided in the following user's manual. Be sure to read it before designing.

- **VRC4172 User's Manual (U14386E)**

FEATURES

- Directly connectable to VR4121
- On-chip USB host controller
  - USB ports: 2
  - Compliant with the USB OpenHCI specifications, release 1.0
  - Communicates with USB device asynchronously with host CPU
  - Full-speed (12 Mbps) and low-speed (1.5 Mbps) modes supported
  - System clock: 48 MHz
- On-chip PS/2 controller
- On-chip IEEE1284 parallel controller
- On-chip 16550 serial controller
- General-purpose ports (GPIO): 24
- On-chip PWM controller
  - Duty modulated light pulse generation function for LCD backlighting
- Internal maximum operating frequency: 48 MHz
- Power supply voltage: V_{DD} = 3.3 V ± 0.3 V
- Package: 208-pin plastic FBGA

APPLICATIONS

- Battery-driven portable information devices
- Peripheral devices for PCs, etc.

Document No. U14388EJ2V0DS00 (2nd edition)
Date Published May 2000 N CP(K)
Printed in Japan

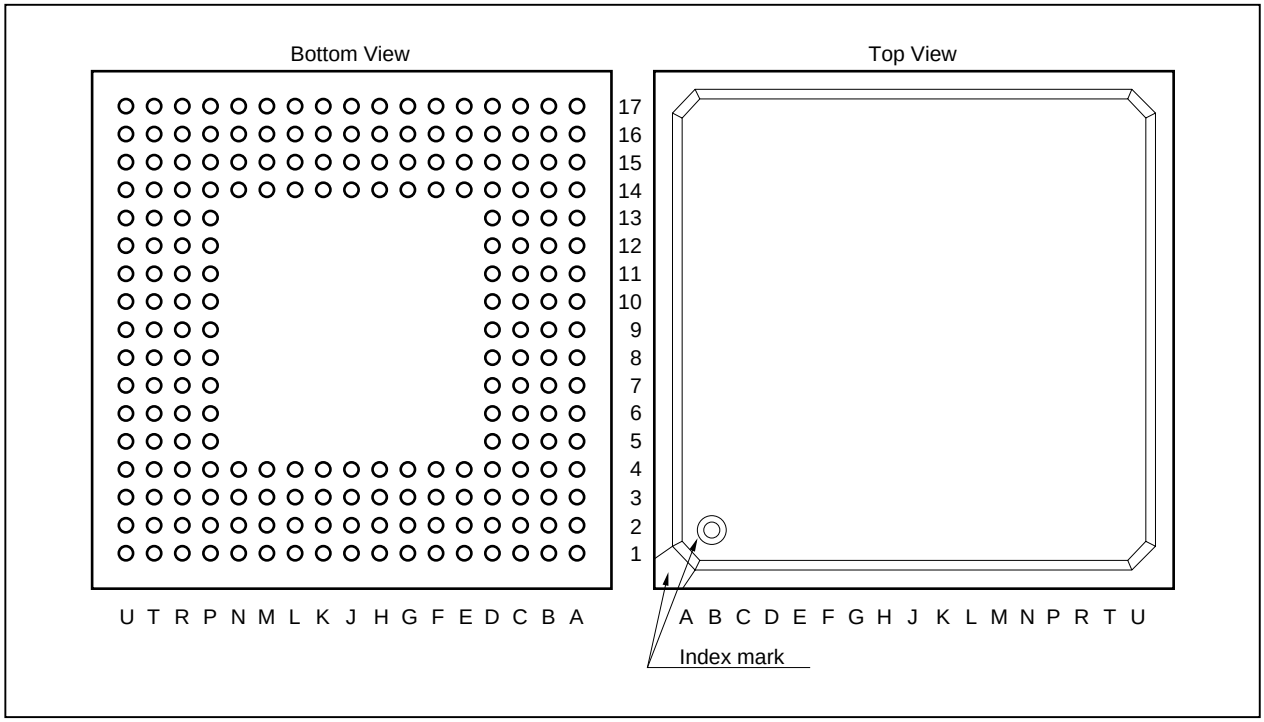
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package	Internal Maximum Operating Frequency
μPD31172F1-48-FN	208-pin plastic FBGA (15 × 15)	48 MHz

PIN CONFIGURATION

- 208-pin plastic FBGA (15 × 15)
  μPD31172F1-48-FN



Symbol	Name	Symbol	Name	Symbol	Name	Symbol	Name
A1	GND	C2	GND	E3	CD3	J15	GND
A2	AUTOFEED#	C3	STROBE#	E4	CD7	J16	UUCAS#
A3	PE	C4	ACK#	E14	GND	J17	ROMCS3#
A4	INIT#	C5	ERROR#	E15	PPON1	K1	GPIO14
A5	IOCHRDY	C6	AD6	E16	OCI2	K2	GPIO10
A6	AD19	C7	AD7	E17	USBRST#	K3	GPIO7
A7	AD20	C8	AD8	F1	GPIO22	K4	GPIO3
A8	AD21	C9	V_{DD}	F2	GPIO18	K14	EXCS3#
A9	AD22	C10	AD9	F3	CD2	K15	EXCS0#
A10	AD23	C11	AD10	F4	CD6	K16	SCAS#
A11	AD24	C12	AD11	F14	SCLK	K17	SRAS#
A12	Reserved[Note 1]	C13	LCDBAK	F15	PPON2	L1	GPIO13
A13	Reserved[Note 1]	C14	SMI#	F16	LCAS#	L2	GPIO9
A14	DP1	C15	USBINT#	F17	MRAS0#	L3	GPIO6
A15	DN2	C16	GND	G1	GPIO21	L4	GPIO2
A16	DP2	C17	RD#	G2	GPIO17	L14	EXCS4#
A17	LCDRDY	D1	GND	G3	CD1	L15	EXCS1#
B1	PS2CLK	D2	SELECTIN#	G4	CD5	L16	Reserved (0)[Note 2]
B2	V_{DD}	D3	DIR1284	G14	Reserved[Note 1]	L17	GND
B3	V_{DD}	D4	PS2INT	G15	Reserved[Note 1]	M1	GPIO12
B4	BUSY	D5	SELECT	G16	UCAS#	M2	GPIO8
B5	GND	D6	AD0	G17	MRAS1#	M3	GPIO5
B6	AD12	D7	AD1	H1	GPIO20	M4	GPIO1
B7	AD13	D8	AD2	H2	GPIO16	M14	EXCS5#
B8	AD14	D9	GND	H3	CD0	M15	EXCS2#
B9	AD15	D10	AD3	H4	CD4	M16	Reserved (0)[Note 2]
B10	AD16	D11	AD4	H14	Reserved[Note 1]	M17	CKE
B11	AD17	D12	AD5	H15	ARBCLKSEL	N1	RESET
B12	AD18	D13	V_{DD}	H16	ULCAS#	N2	BUSRQ0#
B13	GND	D14	IEN	H17	ROMCS2#	N3	GPIO4
B14	DN1	D15	WAKE	J1	GPIO15	N4	GPIO0
B15	V_{DD}	D16	OCI1	J2	GPIO11	N14	GND
B16	GND	D17	LCDCS#	J3	V_{DD}	N15	DSR#
B17	WR#	E1	GPIO23	J4	GND	N16	RXD
C1	PS2DATA	E2	GPIO19	J14	V_{DD}	N17	RI#

Notes 1. Either leave pins A12, A13, G14, G15, and H14 open, or input 0 V.

2. Always input 0 V to pins L16 and M16.

Remark # indicates active low.

Symbol	Name	Symbol	Name	Symbol	Name	Symbol	Name
P1	HOLDRQ#	R1	HOLDAK#	T1	BUSCLK	U1	IOCS16#
P2	BUSAK0#	R2	GND	T2	GND	U2	IRQ
P3	BUSRQ1#	R3	BUSAK1#	T3	V_{DD}	U3	IOR#
P4	GND	R4	DATA23	T4	V_{DD}	U4	IOW#
P5	DATA31	R5	DATA22	T5	DATA15	U5	GND
P6	DATA30	R6	V_{DD}	T6	DATA14	U6	DATA7
P7	DATA29	R7	DATA21	T7	GND	U7	DATA6
P8	DATA28	R8	DATA20	T8	DATA13	U8	DATA5
P9	V_{DD}	R9	GND	T9	DATA12	U9	DATA4
P10	DATA27	R10	DATA19	T10	DATA11	U10	DATA3
P11	DATA26	R11	DATA18	T11	DATA10	U11	DATA2
P12	DATA25	R12	V_{DD}	T12	GND	U12	DATA1
P13	DATA24	R13	DATA17	T13	DATA9	U13	DATA0
P14	CLKOUT48M	R14	DATA16	T14	DATA8	U14	GND
P15	DCD#	R15	CTS#	T15	V_{DD}	U15	DTR#
P16	TXD	R16	GND	T16	V_{DD}	U16	RTS#
P17	INTRP	R17	XOUT48M	T17	XIN48M	U17	GND

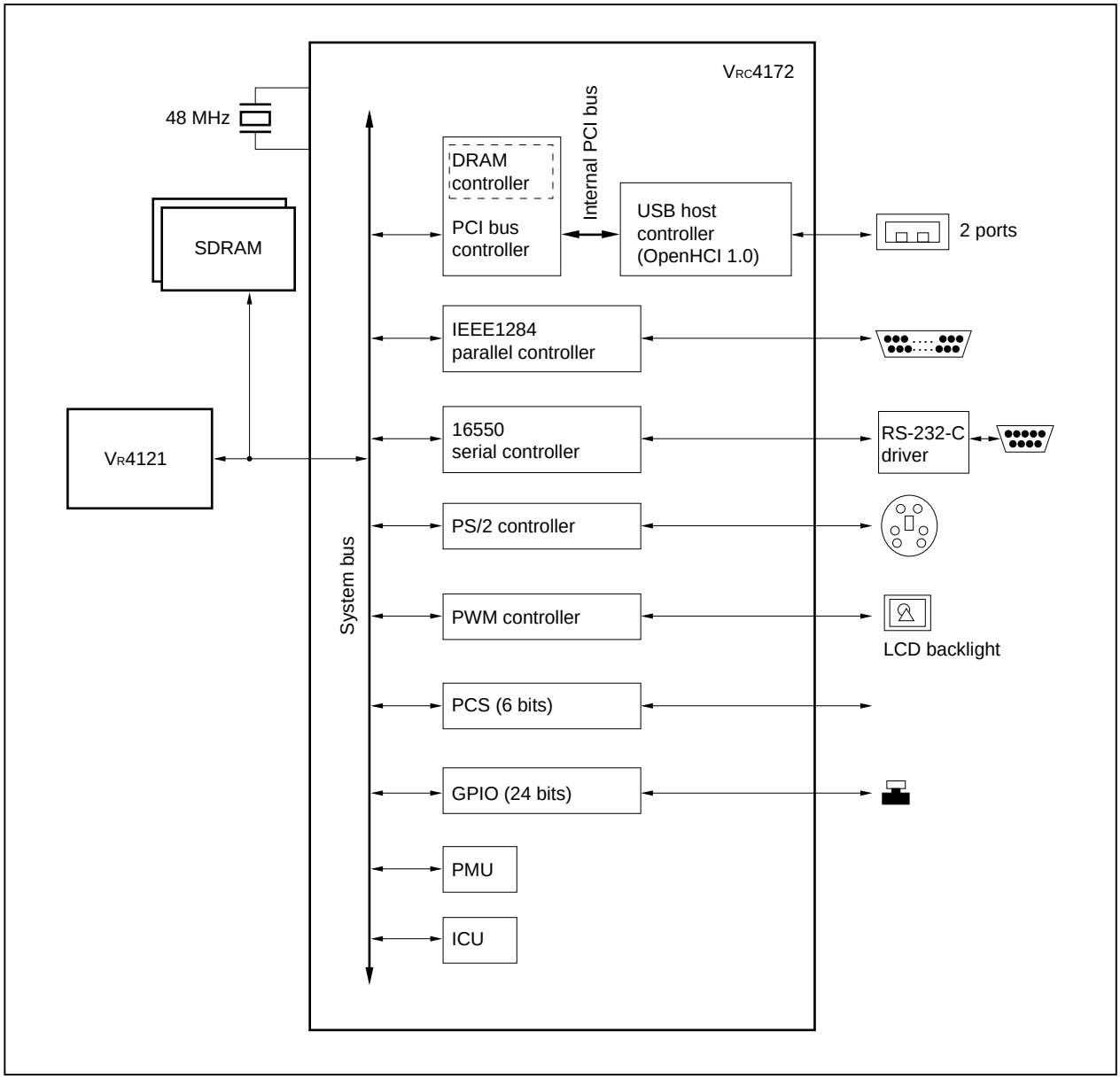
Remark # indicates active low.

PIN IDENTIFICATION

ACK#:	Acknowledge
AD (0:24):	Address Bus
ARBCLKSEL:	Arbitration Clock Select
AUTOFEED#:	Autofeed
BUSAK (0:1)#:	Bus Acknowledge
BUSCLK:	System Bus Clock
BUSRQ (0:1)#:	Bus Request
BUSY:	Busy
CD (0:7):	Centronics Data
CKE:	Clock Enable
CLKOUT48M:	Clock Out of 48 MHz
CTS#:	Clear to Send
DATA (0:31):	Data Bus
DCD#:	Data Carrier Detect
DIR1284:	Direction of 1284
DN (1:2):	USB D–
DP (1:2):	USB D+
DSR#:	Data Set Ready
DTR#:	Data Terminal Ready
ERROR#:	Error
EXCS (0:5)#:	External CS
GND:	Ground
GPIO (0:23):	General Purpose I/O
HOLDAK#:	Hold Acknowledge
HOLDRQ#:	Hold Request
IEN:	USB Input Enable
INIT#	Initialize
INTRP:	Interrupt
IOCHRDY:	I/O Channel Ready
IOCS16#:	IO Chip Select 16
IOR#:	I/O Read
IOW#:	I/O Write
IRQ:	I/O Request
LCAS#:	Lower Column Address Strobe
LCDBAK:	LCD Back Light
LCDCS#:	LCD Chip Select
LCDRDY:	LCD Ready
MRAS (0:1)#:	DRAM Row Address Strobe
OCI (1:2):	Over Current Interrupt
PE:	Paper End
PPON (1:2):	Port Power ON
PS2CLK:	PS2 Clock
PS2DATA:	PS2 Data
PS2INT:	PS2 Interrupt
RD#:	Read
RESET:	Reset
RI#:	Ring Indicator
ROMCS (2:3)#:	ROM Chip Select
RTS#:	Request to Send
RXD:	Receive Data
SCAS#:	Column Address Strobe for SDRAM
SCLK:	SDRAM Clock
SELECT:	Select
SELECTIN#:	Select in
SMI#:	USB System Interrupt
SRAS#:	Row Address Strobe for SDRAM
STROBE#:	Strobe
TXD:	Transmit Data
UCAS#:	Upper Column Address Strobe
ULCAS#:	Lower Byte of Upper Column Address Strobe
USBINT#:	USB Interrupt
USBRST#:	USB Reset
UUCAS#:	Upper Byte of Upper Column Address Strobe
V_{DD}:	Power Supply Voltage
WAKE:	Wake Up Interrupt
WR#:	Write
XIN48M:	Clock In of 48 MHz
XOUT48M:	Clock Out of 48 MHz

Remark # indicates active low.

INTERNAL BLOCK DIAGRAM AND EXTERNAL BLOCK CONNECTION EXAMPLE



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1. PIN FUNCTIONS

1.1 Pin Function List

(1) System bus interface signals

Signal Name	I/O	Function
SCLK	I/O	This is the SDRAM operating clock.
AD (0:24)	I/O	These form a 25-bit address bus.
DATA (0:31)	I/O	These form a 32-bit data bus.
LCDCS#	Input	This is the LCD chip select signal. This signal becomes active when the VR4121 accesses the LCD using the AD or data bus.
RD#	I/O	• Output: This signal becomes active when the VRC4172 accesses SDRAM. • Input: This signal becomes active when the VR4121 reads data from the VRC4172's PCI host bridge.
WR#	I/O	• Output: This signal becomes active when the VRC4172 writes data to SDRAM. • Input: This signal becomes active when the VR4121 writes data to the VRC4172's PCI host bridge.
LCDRDY	Output	This is the LCD ready signal. This signal becomes active when a state is entered whereby the VRC4172 can acknowledge an access to the LCD area from the VR4121.
ROMCS (2:3)#	I/O	This is an SDRAM chip select signal.
CKE	I/O	This is the SDRAM clock enable signal.
UUCAS#	I/O	This is an SDRAM DQM signal. This signal controls the I/O buffers for the DATA (24:31) pins.
ULCAS#	I/O	This is an SDRAM DQM signal. This signal controls the I/O buffers for the DATA (16:23) pins.
MRAS (0:1)#	I/O	This is an SDRAM chip select signal.
UCAS#	I/O	This is an SDRAM DQM signal. This signal controls the I/O buffers for the DATA (8:15) pins.
LCAS#	I/O	This is an SDRAM DQM signal. This signal controls the I/O buffers for the DATA (0:7) pins.
IOR#	Input	This is the system bus I/O read signal. This signal becomes active when any resource except the USB inside the VRC4172 is accessed.
IOW#	Input	This is the system bus I/O write signal. This signal becomes active when any resource except the USB inside the VRC4172 is accessed.
RESET	Input	This is the system bus reset signal.
IOCS16#	Output	This is the dynamic bus-sizing request signal.
IOCHRDY	Output	This is the system bus ready signal.
HOLDRQ#	Output	This is the system bus access right request signal.
HOLDAK#	Input	This is the system bus access enable signal.
SRAS#	I/O	This is the SDRAM RAS signal.
SCAS#	I/O	This is the SDRAM CAS signal.
BUSRQ (0:1)#	Input	This is a signal input from the external bus master requesting access to the system bus.
BUSAK (0:1)#	Output	This is a signal output to the external bus master permitting access to the system bus.
INTRP	Output	This is an interrupt request signal from the 16550 serial controller or the IEEE1284 parallel controller.
IRQ	Output	This is an interrupt request signal from the general-purpose ports (GPIO (0:23)) or the IEEE1284 parallel controller.
USBINT#	Output	This is an interrupt request signal from the USB host controller.
PS2INT	Output	This is an interrupt request signal from the PS/2 controller.
BUSCLK	Input	This is the system bus clock.
ARBCLKSEL	Input	This is a clock select signal for arbitrating the system bus (controls the HOLDRQ# signal) (1: Internal clock used, 0: BUSCLK used)

(2) USB Interface Signals

Signal Name	I/O	Function
DP (1:2)	I/O	This is the positive data signal.
DN (1:2)	I/O	This is the negative data signal.
PPON (1:2)	Output	This is the USB route-hub-port power supply control signal.
OCI (1:2)	Input	This is the USB route-hub-port over-current status signal. Make this signal active when the current flowing through the Vbus line of the USB exceeds the reference value.
IEN	Input	This is the USB buffer input enable signal. Make this signal active when the input signal to the USB port is validated.
WAKE	Output	This is a wakeup interrupt request signal.
SMI#	Output	This is a system interrupt request signal.
USBRST#	Input	This is the reset signal for the USB clock.

(3) IEEE1284 Interface Signals

Signal Name	I/O	Function
CD (0:7)	I/O	These are data signals
STROBE#	I/O	This is the data strobe signal.
ACK#	I/O	This is the acknowledge signal.
BUSY	I/O	This is the busy signal.
PE	I/O	This is the paper-end signal.
SELECT	I/O	This is the select signal.
AUTOFEED#	I/O	This is the autofeed signal.
SLECTIN#	I/O	This is the select input signal.
ERROR#	I/O	This is the fault signal.
INIT#	I/O	This is the initialization signal.
DIR1284	Output	This signal outputs the transfer direction status.

(4) RS-232-C Interface Signals

Signal Name	I/O	Function
RXD	Input	This is the receive data signal.
CTS#	Input	This is the transmit enable signal.
DSR#	Input	This is the data set ready signal.
TXD	Output	This is the transmit data signal.
RTS#	Output	This is the transmit request signal.
DTR#	Output	This is the terminal equipment ready signal.
DCD#	Input	This is the carrier detection signal.
RI#	Input	This is the call display signal.

(5) PS/2 Interface Signals

Signal Name	I/O	Function
PS2CLK	I/O	This is the PS/2 clock signal.
PS2DATA	I/O	This is the PS/2 data signal.

(6) General-Purpose Port Signals

Signal Name	I/O	Function
GPIO (0:23)	I/O	These are general-purpose I/O signals.

(7) General-Purpose Chip Select Signals

Signal Name	I/O	Function
EXCS (0:5)#	Output	These are general-purpose chip select signals.

(8) LCD Interface Signals

Signal Name	I/O	Function
LCDBAK	Output	These are signals for controlling the LCD backlighting.

(9) Clock Signals

Signal Name	I/O	Function
XIN48M	Input	This is the 48 MHz oscillator input pin. Connect to one side of a crystal resonator.
XOUT48M	Output	This is the 48 MHz oscillator output pin. Connect to the other side of the crystal resonator.
CLKOUT48M	Output	This is the 48 MHz clock output for the FIR of the V_R4121.

1.2 Special Status Pins

(1/2)

Signal Name	After Reset	When HOLDAK# = 1
SCLK	Hi-Z	Hi-Z
AD (0:24)	Hi-Z	Hi-Z
DATA (0:31)	Hi-Z	Hi-Z
LCDCS#	–	–
RD#	Hi-Z	Hi-Z
WR#	Hi-Z	Hi-Z
LCDRDY	Hi-Z	Hi-Z
ROMCS (2:3)#	Hi-Z	Hi-Z
CKE	Hi-Z	Hi-Z
UUCAS#	Hi-Z	Hi-Z
ULCAS#	Hi-Z	Hi-Z
MRAS (0:1)#	Hi-Z	Hi-Z
UCAS#	Hi-Z	Hi-Z
LCAS#	Hi-Z	Hi-Z
IOR#	–	–
IOW#	–	–
RESET	–	–
IOCS16#	Hi-Z	Hi-Z
IOCHRDY	Hi-Z	Hi-Z
HOLDRQ#	1	1
HOLDAK#	–	–
SRAS#	Hi-Z	Hi-Z
SCAS#	Hi-Z	Hi-Z
BUSRQ (0:1)#	–	–
BUSAK (0:1)#	1	Normal operation
INTRP	0	Normal operation
IRQ	0	Normal operation
USBINT#	1	Normal operation
PS2INT	0	Normal operation
BUSCLK	–	–
ARBCLKSEL	–	–
DP (1:2)	1	Normal operation
DN (1:2)	0	Normal operation
PPON (1:2)	0	Normal operation
OCI (1:2)	–	–
IEN	–	–
WAKE	0	Normal operation

Remark 0: Low level, 1: High level, Hi-Z: High impedance

(2/2)

Signal Name	After Reset	When HOLDAK# = 1
SMI#	1	Normal operation
USBRST#	–	–
CD (0:7)	Hi-Z	Normal operation
STROBE#	Hi-Z	Normal operation
ACK#	Hi-Z	Normal operation
BUSY	Hi-Z	Normal operation
PE	Hi-Z	Normal operation
SELECT	Hi-Z	Normal operation
AUTOFEED#	Hi-Z	Normal operation
SELECTIN#	Hi-Z	Normal operation
ERROR#	Hi-Z	Normal operation
INIT#	Hi-Z	Normal operation
DIR1284	0	Normal operation
RXD	–	–
CTS#	–	–
DSR#	–	–
TXD	1	Normal operation
RTS#	1	Normal operation
DTR#	1	Normal operation
DCD#	–	–
RI#	–	–
PS2CLK	0	Normal operation
PS2DATA	Hi-Z	Normal operation
GPIO (0:23)	Hi-Z	Normal operation
EXCS (0:5)#	1	Normal operation
LCDBAK	0	Normal operation
CLKOUT48M	1	Normal operation

Remark 0: Low level, 1: High level, Hi-Z: High impedance

1.3 External Processing of Pins and Drive Capacity

When using the VRC4172, process the pins externally, as shown in the table below.

(1/2)

Signal Name	External Processing	Drive Capacity	Tolerance
SCLK	–	80 pF	3 V
AD (0:24)	–	80 pF	3 V
DATA (0:31)	–	80 pF	3 V
LCDCS#	Pull up	–	3 V
RD#	Pull up Note 1	80 pF	3 V
WR#	Pull up Note 1	80 pF	3 V
LCDRDY	Pull up	40 pF	3 V
ROMCS (2:3)#	Pull up	80 pF	3 V
CKE	Pull down	80 pF	3 V
UUCAS#	Pull up Note 1	80 pF	3 V
ULCAS#	Pull up Note 1	80 pF	3 V
MRAS (0:1)#	Pull up Note 1	80 pF	3 V
UCAS#	Pull up Note 1	80 pF	3 V
LCAS#	Pull up Note 1	80 pF	3 V
IOR#	Pull up Note 1	–	3 V
IOW#	Pull up Note 1	–	3 V
RESET	–	–	3 V
IOCS16#	Pull up	40 pF	3 V
IOCHRDY	Pull up	40 pF	3 V
HOLDRQ#	–	40 pF	3 V
HOLDAK#	Pull up	–	3 V
SRAS#	Pull up Note 1	80 pF	3 V
SCAS#	Pull up Note 1	80 pF	3 V
BUSRQ (0:1)#	–	–	3 V
BUSAK (0:1)#	–	40 pF	3 V
INTRP	–	40 pF	3 V
IRQ	–	40 pF	3 V
USBINT#	–	40 pF	3 V
PS2INT	–	40 pF	3 V
BUSCLK	–	–	3 V
ARBCLKSEL	–	–	3 V
DP (1:2)	–	**Note 2**	5 V
DN (1:2)	–	**Note 2**	5 V

Notes 1. The same specification has been made for these pins in the VR4121. If these pins have been processed in the VR4121, there is no need to perform this processing in the VRC4172.

2. In full-speed mode: 50 pF, In low-speed mode: 350 pF

Remark There is no need to perform external processing if no particular external processing has been specified (–).

(2/2)

Signal Name	External Processing	Drive Capacity	Tolerance
PPON (1:2)	–	40 pF	3 V
OCI (1:2)	–	–	3 V
IEN	–	–	3 V
WAKE	–	40 pF	3 V
SMI#	–	40 pF	3 V
USBRST#	–	–	3 V
CD (0:7)	–	40 pF	3 V
STROBE#	Pull up	40 pF	3 V
ACK#	Pull up	40 pF	3 V
BUSY	Pull down	40 pF	3 V
PE	Pull down	40 pF	3 V
SELECT	Pull down	40 pF	3 V
AUTOFEED#	Pull up	40 pF	3 V
SELECTIN#	Pull up	40 pF	3 V
ERROR#	Pull up	40 pF	3 V
INIT#	Pull up	40 pF	3 V
DIR1284	–	40 pF	3 V
RXD	–	–	3 V
CTS#	–	–	3 V
DSR#	–	–	3 V
TXD	–	40 pF	3 V
RTS#	–	40 pF	3 V
DTR#	–	40 pF	3 V
DCD#	–	–	3 V
RI#	–	–	3 V
PS2CLK	Pull up	40 pF	5 V
PS2DATA	Pull up	40 pF	5 V
GPIO (0:23)	Pull up/pull down	40 pF	3 V
EXCS (0:5)#	–	40 pF	3 V
LCDBAK	–	40 pF	3 V
CLKOUT48M	–	40 pF	3 V

Remark There is no need to perform external processing if no particular external processing has been specified (–).

1.4 Recommended Connection of Unused Pins

Connect unused pins as shown in the table below.

Signal Name	Recommended Connection	Signal Name	Recommended Connection
SCLK	Pull up	PPON (1:2)	Leave open
AD (0:24)	–	OCI (1:2)	Pull down
DATA (0:31)	–	IEN	Pull down
LCDCS#	Pull up	WAKE	Leave open
RD#	Pull up	SMI#	Leave open
WR#	Pull up	USBRST#	Pull down
LCDRDY	Leave open	CD (0:7)	Pull down
ROMCS (2:3)#	Pull up	STROBE#	Pull up
CKE	Pull down	ACK#	Pull up
UUCAS#	Pull up	BUSY	Pull down
ULCAS#	Pull up	PE	Pull down
MRAS (0:1)#	Pull up	SELECT	Pull down
UCAS#	Pull up	AUTOFEED#	Pull up
LCAS#	Pull up	SELECTIN#	Pull up
IOR#	–	ERROR#	Pull up
IOW#	–	INIT#	Pull up
RESET	–	DIR1284	Leave open
IOCS16#	–	RXD	Pull down
IOCHRDY	–	CTS#	Pull up
HOLDRQ#	Leave open	DSR#	Pull up
HOLDAK#	Pull up	TXD	Leave open
SRAS#	Pull up	RTS#	Leave open
SCAS#	Pull up	DTR#	Leave open
BUSRQ (0:1)#	Pull up	DCD#	Pull up
BUSAK (0:1)#	Leave open	RI#	Pull up
INTRP	Leave open	PS2CLK	Pull up
IRQ	Leave open	PS2DATA	Pull up
USBINT#	Leave open	GPIO (0:23)	Pull down
PS2INT	Leave open	EXCS (0:5)#	Leave open
BUSCLK	Pull up	LCDBAK	Leave open
ARBCLKSEL	Pull down	XIN48M	Pull up
DP (1:2)	Pull down	XOUT48M	Leave open
DN (1:2)	Pull down	CLKOUT48M	Leave open

Remark Pins with no particular specification (–) cannot be left unconnected.

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage	V_I	$V_I < V_{DD}$ + 0.5 V	–0.5 to +4.6	V
		$V_I < V_{DD}$ + 3.0 V, DP (2:1), DN (2:1), PS2CLK, PS2DATA pins	–0.5 to +6.6	V
Output voltage	V_O	$V_O < V_{DD}$ + 0.5 V	–0.5 to +4.6	V
		$V_O < V_{DD}$ + 3.0 V, DP (2:1), DN (2:1), PS2CLK, PS2DATA pins	–0.5 to +6.6	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not simultaneously short multiple outputs.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions displayed in DC Characteristics and AC Characteristics in this section indicate the ranges in which normal operation and product quality can be guaranteed.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz Unmeasured pins returned to 0 V.		8	pF
Output capacitance	C_{O1}			8	pF
Output capacitance[Note]	C_{O2}			12	pF

Note Applicable to DP (2:1), DN (2:1), PS2CLK, and PS2DATA pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 ± 0.3 V)

(1) Pins except for DP (2:1), DN (2:1)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –6 mA	2.4		V
Output voltage, low	V_{OL1}	I_{OL} = 6 mA		0.4	V
Output voltage, high[Note 1]	V_{OH2}	I_{OH} = –9 mA	2.4		V
Output voltage, low[Note 1]	V_{OL2}	I_{OL} = 9 mA		0.4	V
Output voltage, high[Note 2]	V_{OH3}	I_{OH} = –3 mA	2.4		V
Output voltage, low[Note 2]	V_{OL3}	I_{OL} = 3 mA		0.4	V
Input voltage, high	V_{IH1}		2.0	V_{DD}	V
Input voltage, high[Note 2]	V_{IH2}		2.0	5.5	V
Input voltage, low	V_{IL}		0	0.8	V
Power supply current	I_{DD}			300	mA
Input leakage current	I_{LI}	V_I = V_{DD}, GND		±10	μA
Input leakage current, high	I_{LIH}	V_I = V_{DD}, ARBCLKSEL pin		141	μA
Output leakage current	I_{LO}	V_O = V_{DD}, GND		±10	μA

Notes 1. Applicable to SCLK, AD (24:0), DATA (31:0), RD#, WR#, ROMCS (3:2)#, CKE#, UUCAS#, ULCAS#, MRAS (1:0)#, UCAS#, LCAS#, SRAS#, and SCAS# pins.

2. Applicable to PS2CLK and PS2DATA pins.

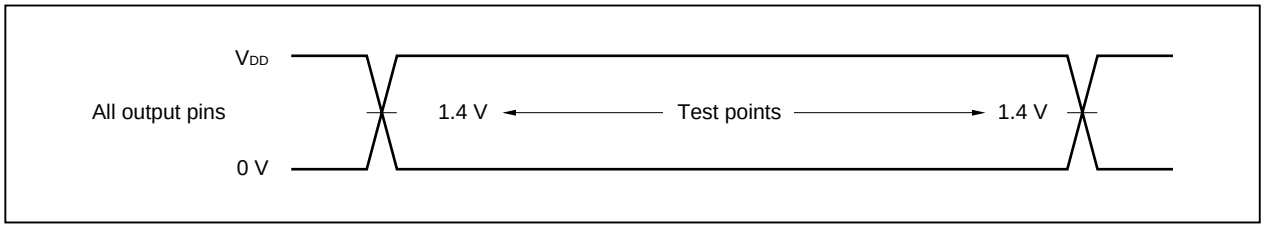
(2) DP (2:1), DN (2:1) pins

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V_{OH}	R_L = 15 kΩ (connected to GND)	2.8	3.6	V
Output voltage, low	V_{OL}	R_L = 1.5 kΩ (connected to V_{DD})		0.3	V
Differential input sensitivity	V_{DI}		0.2		V
Differential common mode range	V_{CM}	V_{DI} < 200 mV	0.8	2.5	V
Input voltage, high	V_{IH_USB}		2.0		V
Input voltage, low	V_{IL_USB}			0.8	V

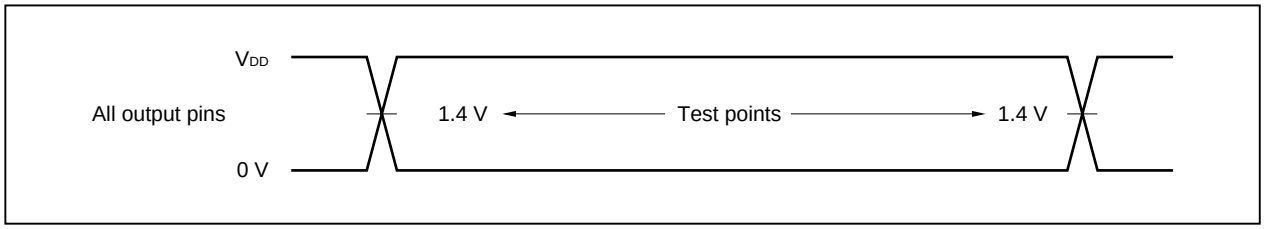
Remark Refer to the USB specification, revision 1.0, for details.

AC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 ± 0.3 V)

AC test input waveform

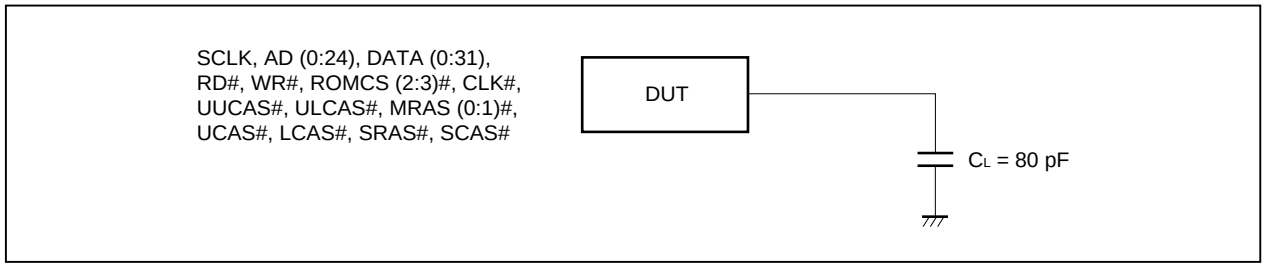


AC test output test points

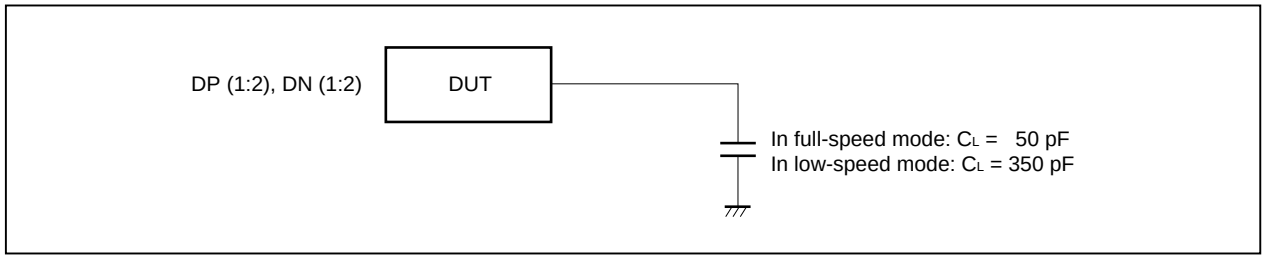


Load Conditions

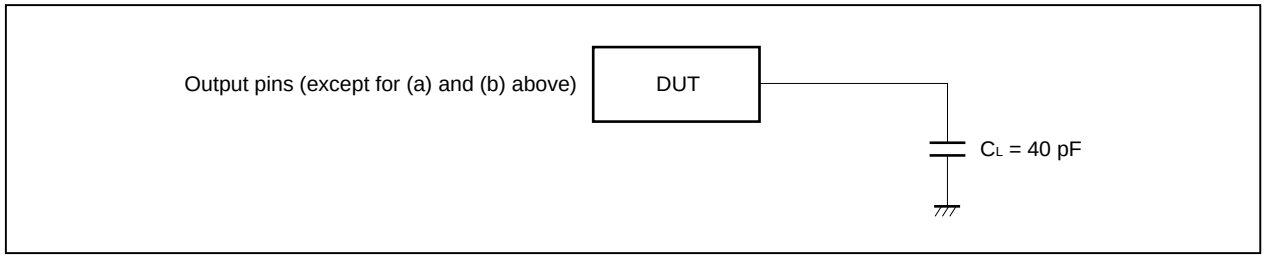
(a) SCLK, AD (0:24), DATA (0:31), RD#, WR#, ROMCS (2:3)#, CLK#, UUCAS#, ULCAS#, ULCAS#, MRAS (0:1)#, UCAS#, LCAS#, SRAS#, SCAS#



(b) DP (1:2), DN (1:2)



(c) Other output pins



(1) Clock parameters

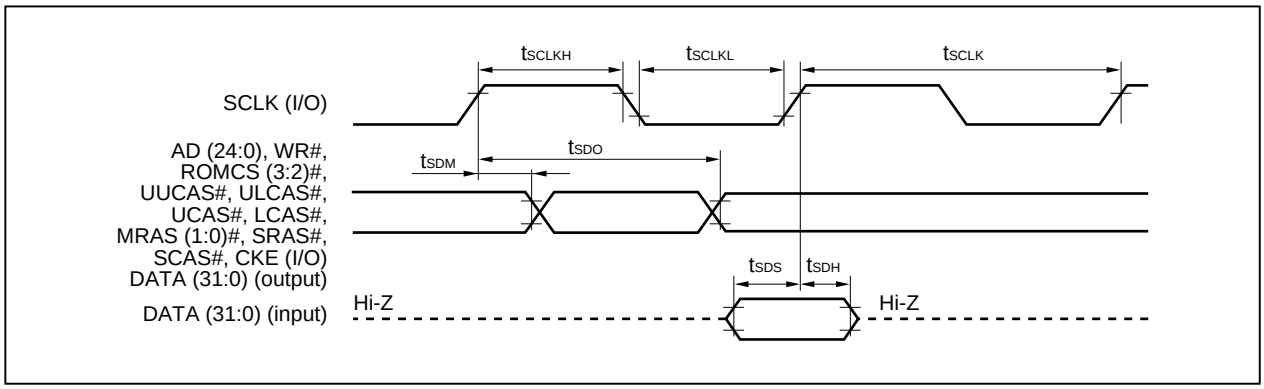
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ XIN48M clock frequency	f_{CLK}			48.0	50.0	MHz

(2) Reset parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RESET signal high-level width	t_{RST}		30		ns
USBRST# signal low-level width	t_{USBRST}		30		ns

(3) SDRAM interface parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLK cycle	t_{SCLK}		20.8		ns
SCLK high-level width	t_{SCLKH}		8		ns
SCLK low-level width	t_{SCLKL}		8		ns
Data output hold time	t_{SDM}		2		ns
Data output delay time	t_{SDO}			15	ns
Data input setup time	t_{SDS}		9.5		ns
Data input hold time	t_{SDH}		2		ns

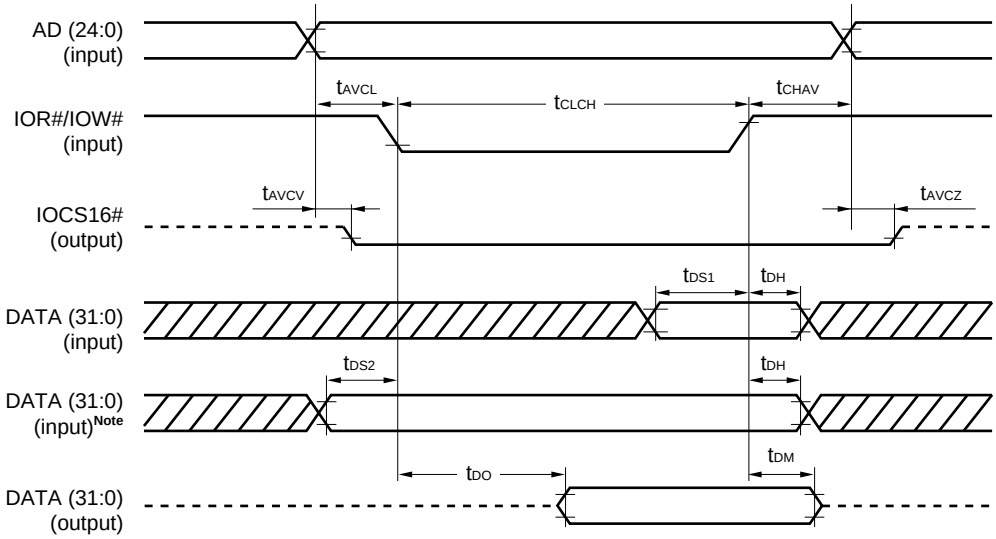


(4) System bus interface parameters

(a) Access to I/O area

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Command signal low-level width	t_{CLCH}		130		ns
Address setup time (to command signal)	t_{AVCL}		10		ns
Address hold time (from command signal)	t_{CHAV}		10		ns
IOCS16# valid delay time	t_{AVCV}			12	ns
IOCS16# floating delay time	t_{AVCZ}			10	ns
Data output hold time	t_{DM}		6	25	ns
Data output delay time	t_{DO}			30	ns
Data input setup time	t_{DS1}		10		ns
Data input setup time[Note]	t_{DS2}		10		ns
Data input hold time	t_{DH}		10		ns

Note During 16550-compatible serial communication



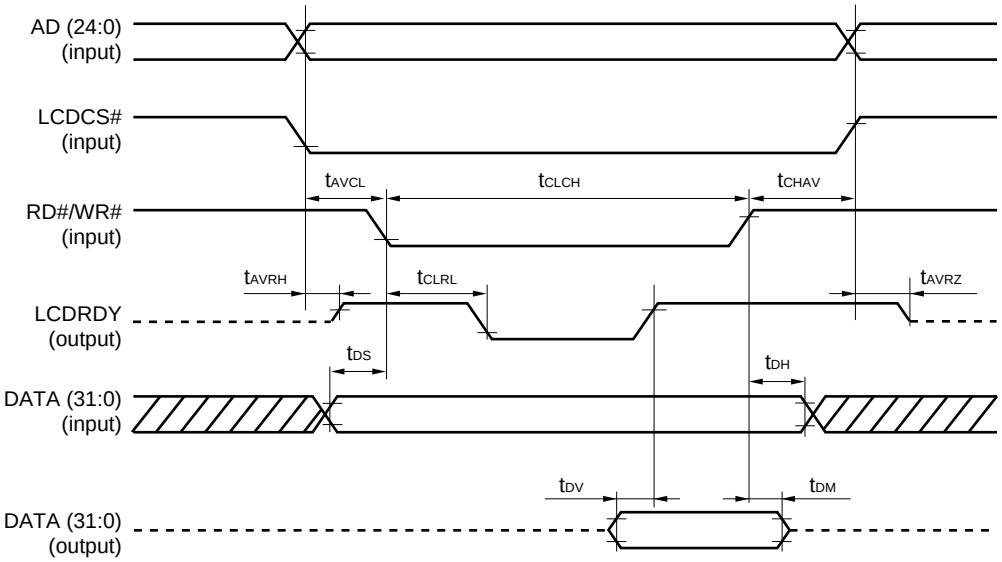
Note During 16550-compatible serial communication

Remark The broken lines indicate high impedance

(b) Access to LCD area

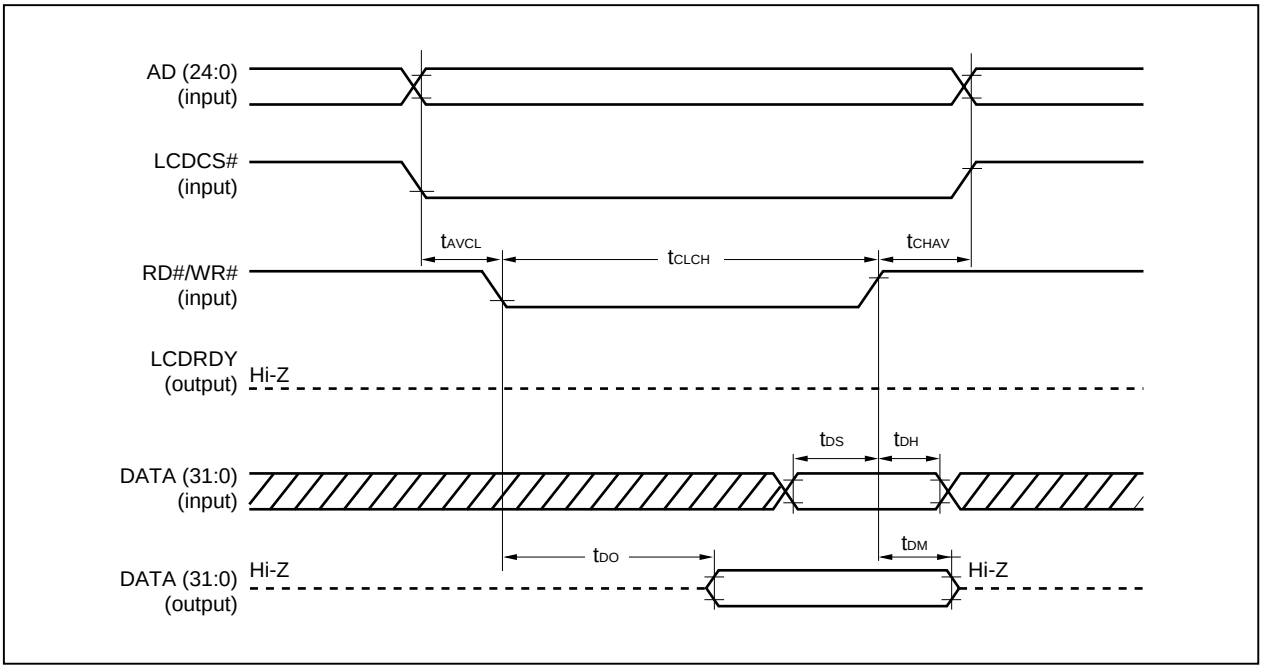
	Parameter	Symbol	Conditions	MIN.	MAX.	Unit
	Command signal low-level width	t_{CLCH}		90		ns
	Address setup time (to command signal)	t_{AVCL}		10		ns
	Address hold time (from command signal)	t_{CHAV}		10		ns
★	LCDRDY valid delay time	t_{AVRH}			15	ns
	LCDRDY set delay time	t_{CLRL}			12	ns
	LCDRDY floating delay time	t_{AVRZ}			10	ns
	Data output hold time	t_{DM}		6	25	ns
	Data output delay time	t_{DO}			30	ns
★	Data output valid time	t_{DV}		10		ns
	Data input setup time	t_{DS}		10		ns
	Data input hold time	t_{DH}		10		ns

(i) When accessing the internal PCI bus



Remark The broken lines indicate high impedance

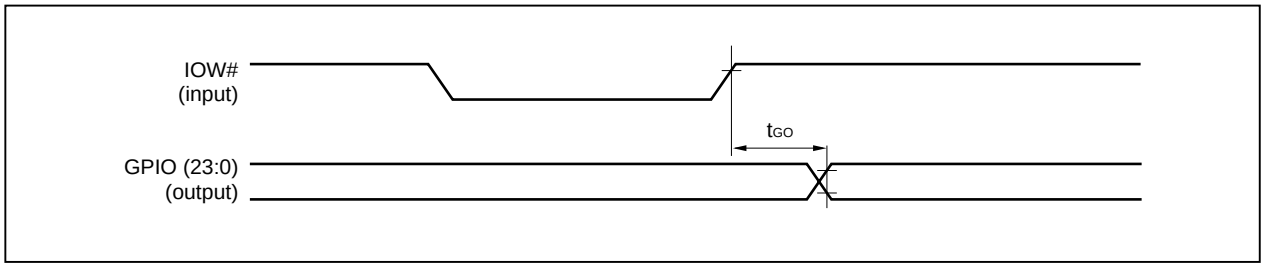
(ii) When accessing the configuration register of the PCI host controller



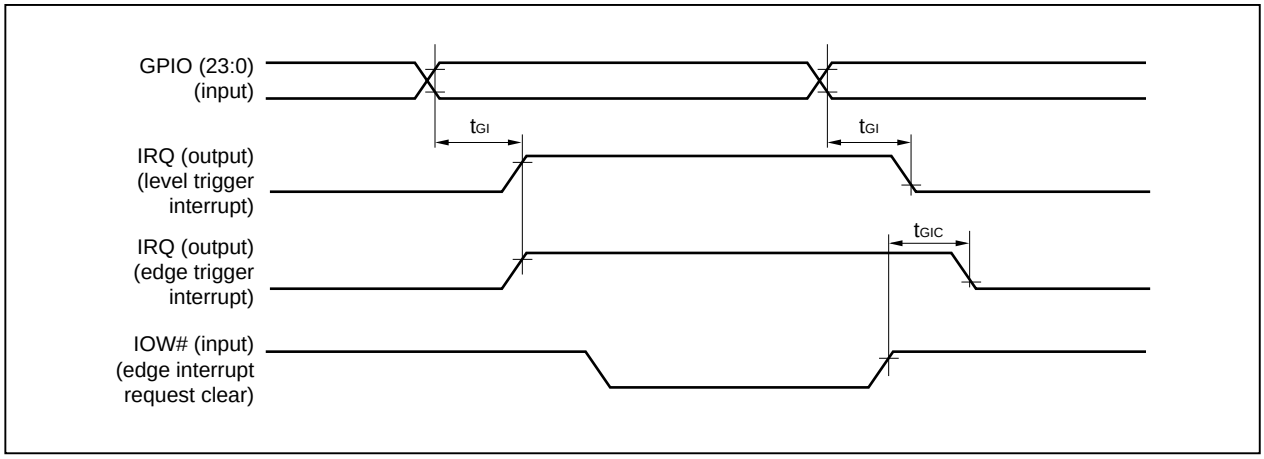
(5) GPIO parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
GPIO (23:0) output delay time	t_{GO}			30	ns
GPIO (23:0) interrupt request generation time	t_{GI}			30	ns
GPIO (23:0) interrupt request clear time	t_{GIC}			35	ns

(a) In output mode

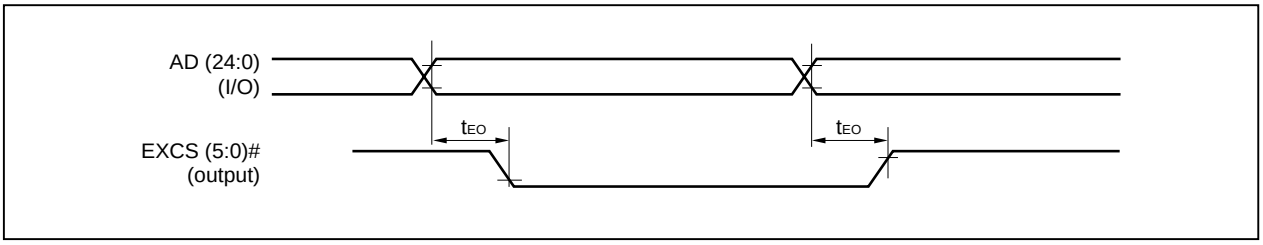


(b) In input mode



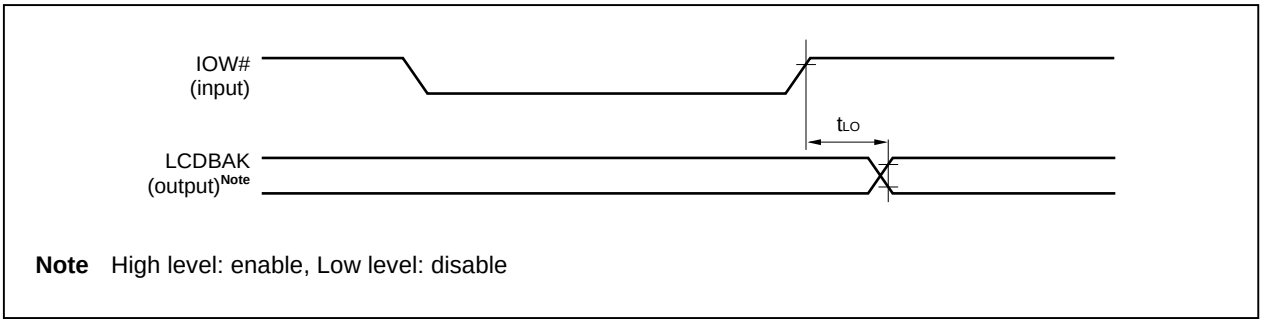
(6) PCS (Programmable Chip Select) parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
EXCS output delay time	t_{EO}			30	ns



(7) PWM (Pulse Width Modulation) parameters

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
LCDBAK output delay time	t_{LO}			8 t_{SCLK}	ns



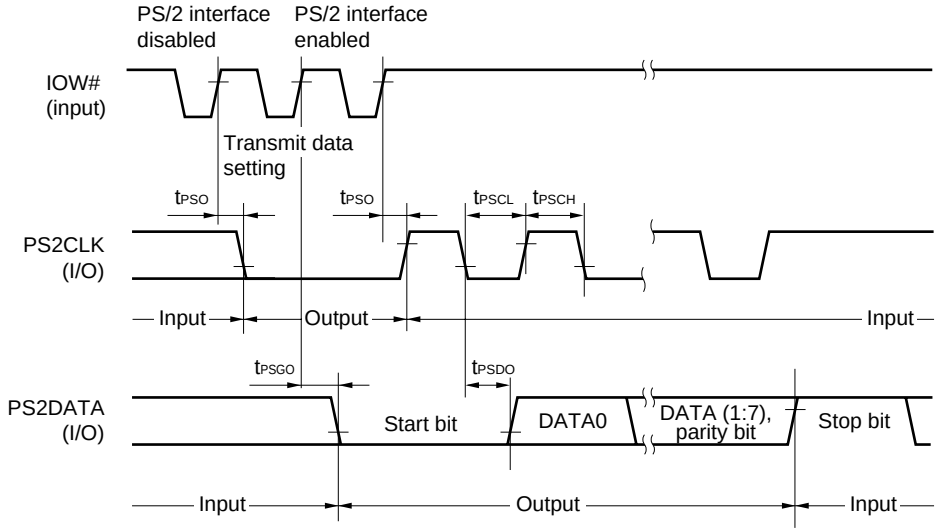
Note High level: enable, Low level: disable

(8) PS/2 parameters

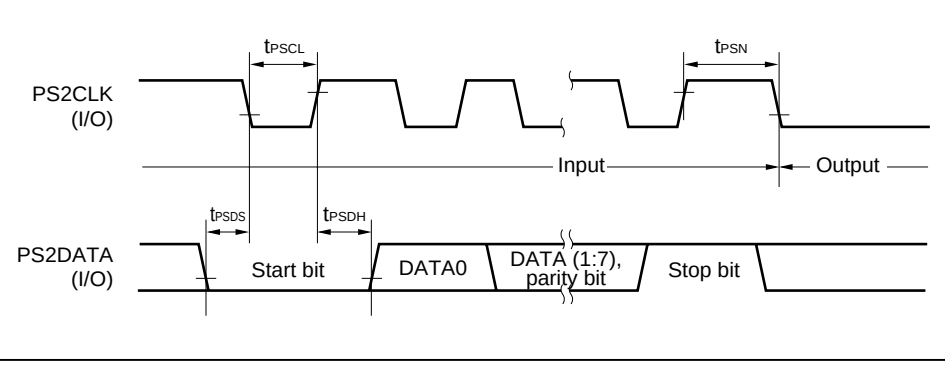
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
PS2CLK clock high-level width	t_{PSCH}		3 T		ns
PS2CLK clock low-level width	t_{PSCL}		3 T		ns
PS2CLK output delay time	t_{PSO}			T + 20	ns
Transmission start time	t_{PSGO}			20	ns
Transmit data output delay time	t_{PSDO}			3 T + 20	ns
Receive data setup time	t_{PSDS}		0		ns
Receive data hold time	t_{PSDH}		4 T		ns
Receive disable setup time	t_{PSN}			3 T	ns

Remark T = 125 ns (cycle of internal clock for controlling PS/2)

(a) Transmission



(b) Reception



(9) 16550-compatible serial interface parameters

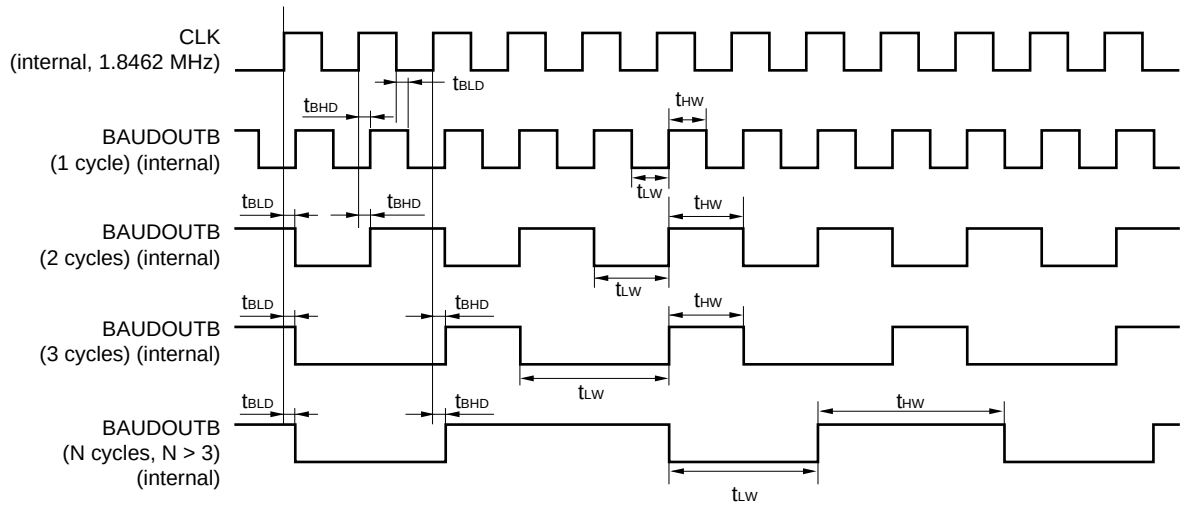
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Transmit clock division ratio	N		1		$2^{16} - 1$	
	Transmit clock rising edge delay time (from CLK[Note 1])	t_{BHD}				10	ns
	Transmit clock falling edge delay time (from CLK[Note 1])	t_{BLD}				15	ns
★	Transmit clock pulse low-level width	t_{LW}	N = 1		0.5CLKC		ns
			N = 2		1CLKC		ns
			N = 3		2CLKC		ns
			N > 3		2CLKC		ns
★	Transmit clock pulse high-level width	t_{HW}	N = 1		0.5CLKC		ns
			N = 2		1CLKC		ns
			N = 3		1CLKC		ns
			N > 3		(N – 2) CLKC		ns
	Interrupt cancellation time (from IOR# ↑, when reading LSR register)	t_{RINT1}				40	ns
	Interrupt cancellation time (from IOR# ↓, when reading RBR register)	t_{RINT2}				30	ns
	Sample clock delay time (from RCLK)	t_{SCD}				10	ns
	Interrupt generation time (from valid data reception, reception error)	t_{SINT}				1 RCLKC + 20[Note 2]	ns
	Interrupt cancellation time (from IOW# ↓, when writing to THR register)	t_{HR}				30	ns
	Interrupt cancellation time (from IOR# ↑, when reading IIR register)	t_{IR}				40	ns
	Transmission start time	t_{IRS}		8 BAUC		24 BAUC + 20	ns
	Interrupt generation time (from IOW# ↑, when writing to THR register)	t_{SI}		16 BAUC		24 BAUC + 20	ns
	Interrupt generation time (from stop bit)	t_{STI}				8 BAUC + 20	ns
	RTS#, DTR delay time (from IOW# ↑, when writing to MCR register)	t_{MDO}				30	ns
	Interrupt cancellation time (from IOR# ↓, when reading MSR register)	t_{RIM}				30	ns
	Interrupt cancellation time (from RI# ↑, CTS#, DSR#, DCD#)	t_{SIM}				30	ns

Notes 1. CLK is the internal system clock of the 16550 serial controller, and has a frequency of 1.8462 MHz.

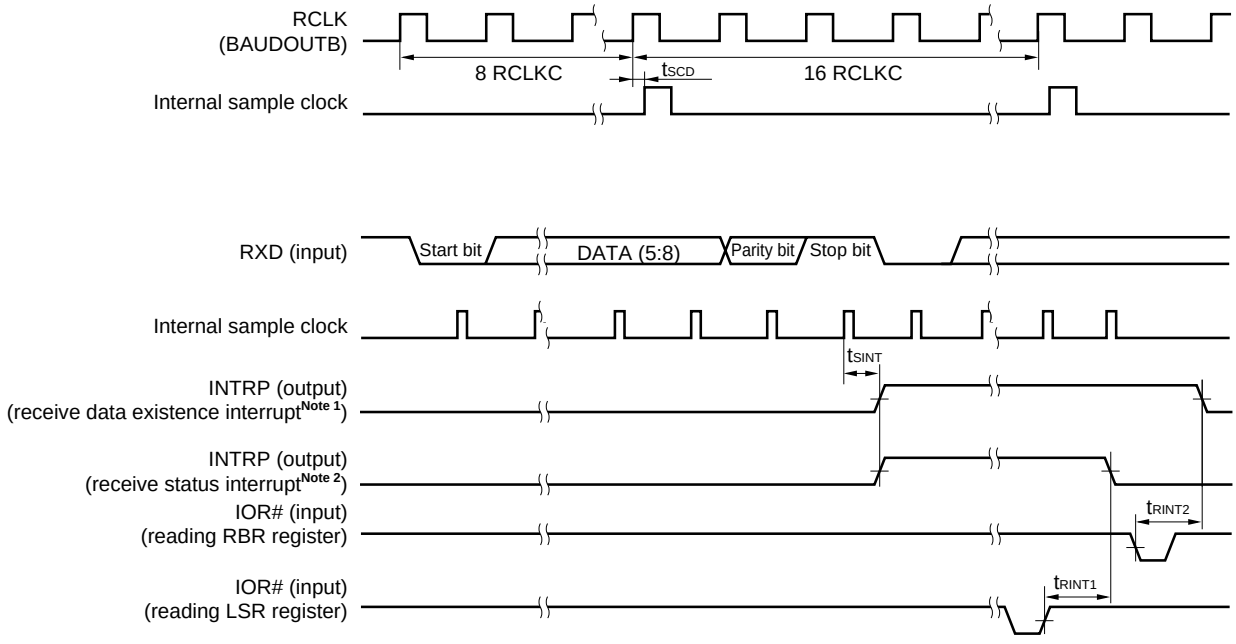
2. When bit 0 of the FCR register is 1, t_{SINT} = 3 RCLKC + 20 (ns).
During a timeout interrupt, t_{SINT} = 8 RCLKC + 20 (ns).

★ **Remark** CLKC: CLK (internal system clock of 16550 serial controller) cycle
RCLKC: RCLK (on-chip serial controller receive clock) cycle
BAUC: BAUDOUTB (on-chip serial controller transmit clock) cycle
RCLKC = BAUC in this case.

(a) Serial BAUDOUT timing



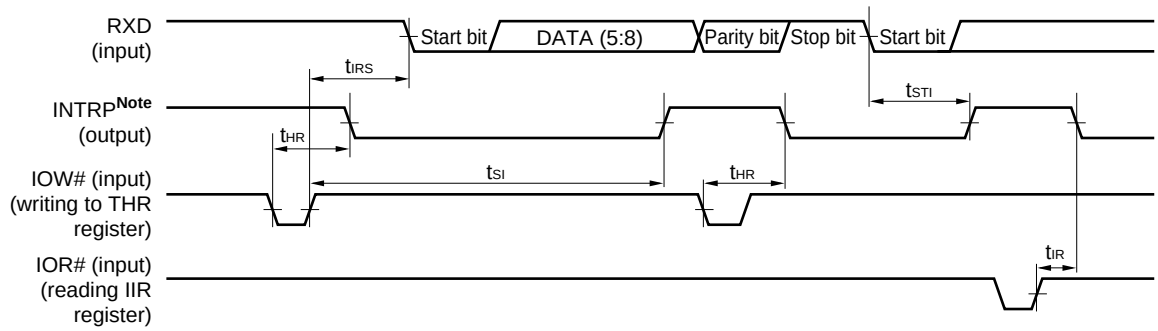
(b) Serial receive timing



Notes 1. Dependant on the existence of receive data. At this time, bit 0 of the IER register is 1, and bits 3 to 1 of the IIR register are 0, 1, 0, respectively.

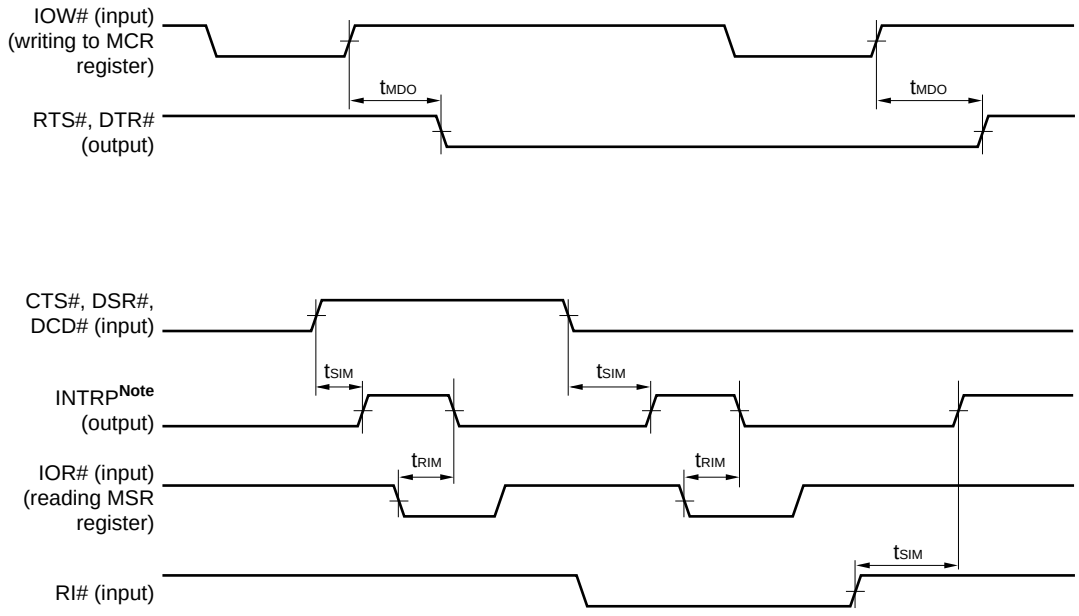
2. Dependant on the receive line status. At this time, bit 2 of the IER register is 1, and bits 3 to 1 of the IIR register are 0, 1, 1, respectively.

(c) Serial transmission timing



Note Dependant on whether the transmit buffer is empty. At this time, bit 1 of the IER register is 1, and bits 3 to 1 of the IIR register are 0, 0, 1, respectively.

(d) Serial modem control timing



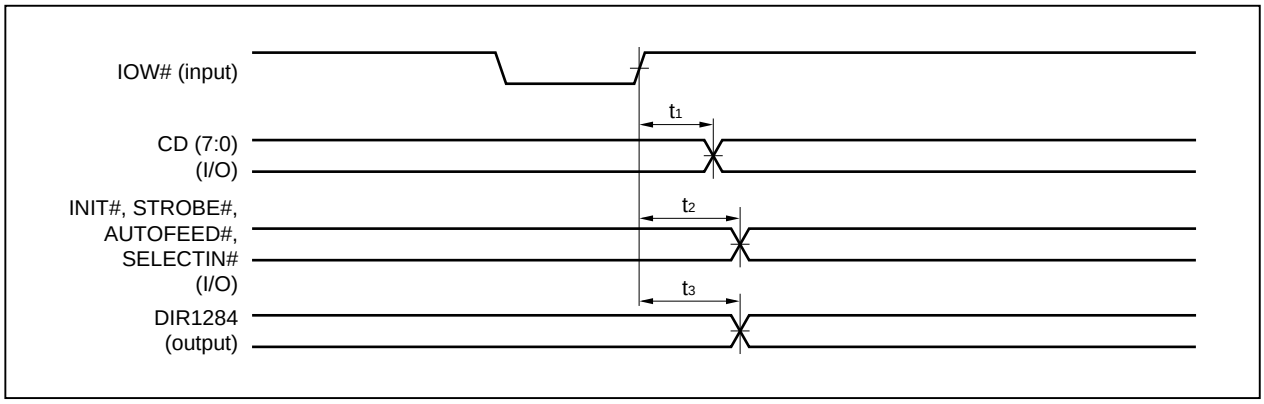
Note Dependant on the modem status. At this time, bit 3 of the IER register is 1, and bits 3 to 1 of the IIR register are 0, 0, 0, respectively.

(10) IEEE1284-compliant parallel interface parameters

(a) Parallel port control signal output

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Parallel interface internal clock frequency	$t_{CLK1284}$			24	MHz
CD (7:0) output delay time (writing to DATA register)	t_1			30	ns
INIT#, STROBE#, AUTOFEED#, SELECTIN# setup time	t_2			4 T	ns
DIR1284 setup time	t_3			5 T	ns

★**Remark** T: Parallel interface internal clock cycle (41.6 ns (MIN.))



★ (b) Compatible mode using FIFO

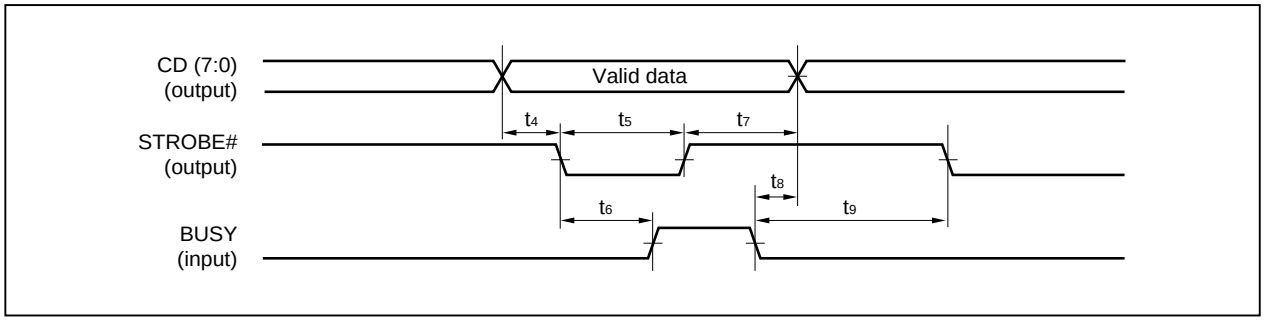
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CD (7:0) setup time	t_4		24 T		ns
STROBE# pulse width[Note 1]	t_5		24 T		ns
BUSY response time	t_6			12 T	ns
CD (7:0) hold time[Note 2] (from STROBE# ↑)	t_7		24 T		ns
CD (7:0) hold time[Note 2] (from BUSY ↓)	t_8		0		ns
STROBE# setup time[Note 3]	t_9		24 T		ns

Notes 1. When there is no reaction from BUSY at a low level, STROBE# continues to output a low level.

2. Data is held while BUSY is high level.

3. When the FIFO buffer is empty, this signal is held at a high level.

★**Remark** T: Parallel interface internal clock cycle (41.6 ns (MIN.))

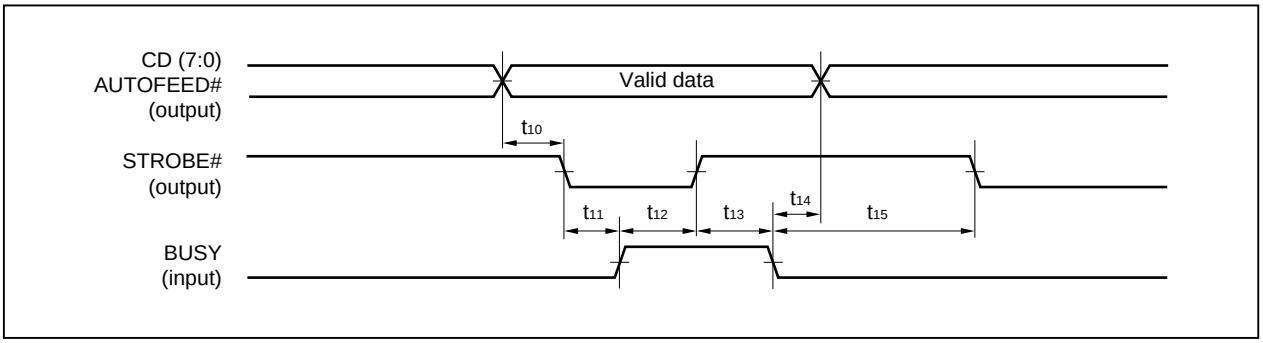


(c) During ECP normal-direction transfer

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CD (7:0), AUTOFEED# setup time	t_{10}		1 T	2 T	ns
BUSY response time (from STROBE# ↓)	t_{11}		0		ns
STROBE# response time	t_{12}		2 T	4 T	ns
BUSY response time (from STROBE# ↑)	t_{13}		0		ns
CD (7:0) hold time	t_{14}		2 T	4 T	ns
STROBE# setup time[Note]	t_{15}		3 T	6 T	ns

Note When the FIFO buffer is empty, this signal is held at a high level.

★ **Remark** T: Parallel interface internal clock cycle (41.6 ns (MIN.))

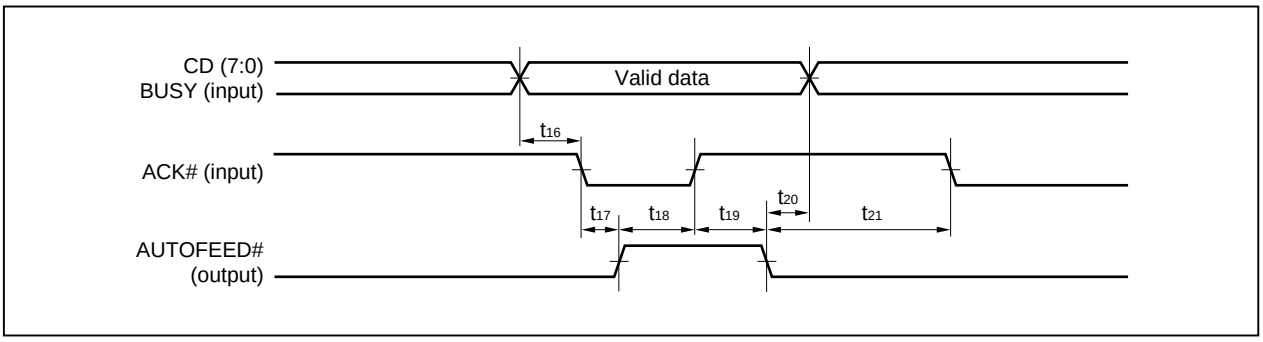


(d) During ECP reverse-direction transfer

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CD (7:0), BUSY setup time	t_{16}		0		ns
AUTOFEED# response time[Note] (from ACK# ↓)	t_{17}		3 T		ns
ACK# response time	t_{18}		0		ns
AUTOFEED# response time (from ACK# ↑)	t_{19}			5 T	ns
CD (7:0) hold time	t_{20}		0		ns
ACK# setup time	t_{21}		0		ns

Note When the FIFO buffer is full, this signal is held at a low level.

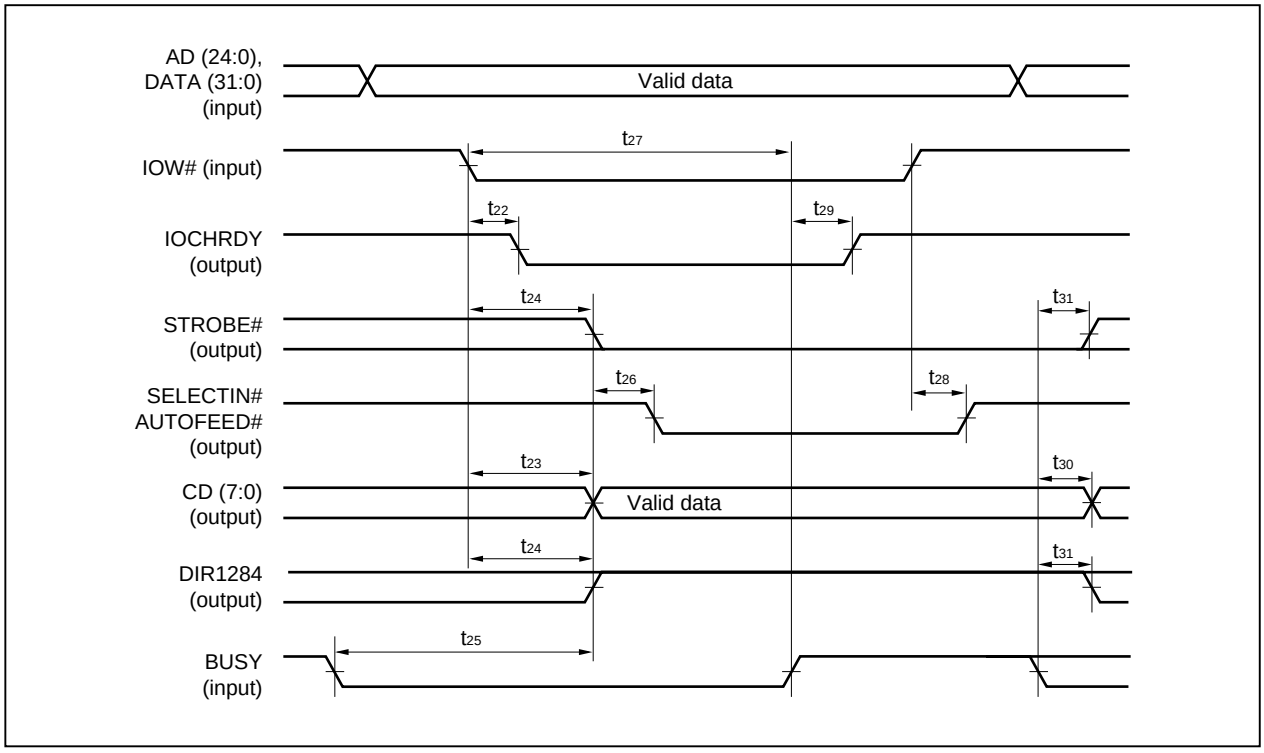
★ **Remark** T: Parallel interface internal clock cycle (41.6 ns (MIN.))



(e) Write timing in EPP1.9 mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
IOCHRDY setup time	t_{22}			3 T	ns
CD (7:0) output delay time	t_{23}			30	ns
STROBE# setup time, DIR1284 cancellation time (from IOW# ↓)	t_{24}			5 T	ns
STROBE# setup time, DIR1284 cancellation time (from BUSY ↓)	t_{25}			4 T	ns
SELECTIN#, AUTOFEED# setup time (from STROBE# ↓, valid data output)	t_{26}		0		ns
Timeout generation time	t_{27}			10	μs
SELECTIN#, AUTOFEED# cancellation time (from IOW# ↑)	t_{28}			3 T	ns
IOCHRDY cancellation time	t_{29}			4 T	ns
CD (7:0) hold time	t_{30}		1 T		ns
STROBE# cancellation time, DIR1284 setup time	t_{31}		1 T		ns

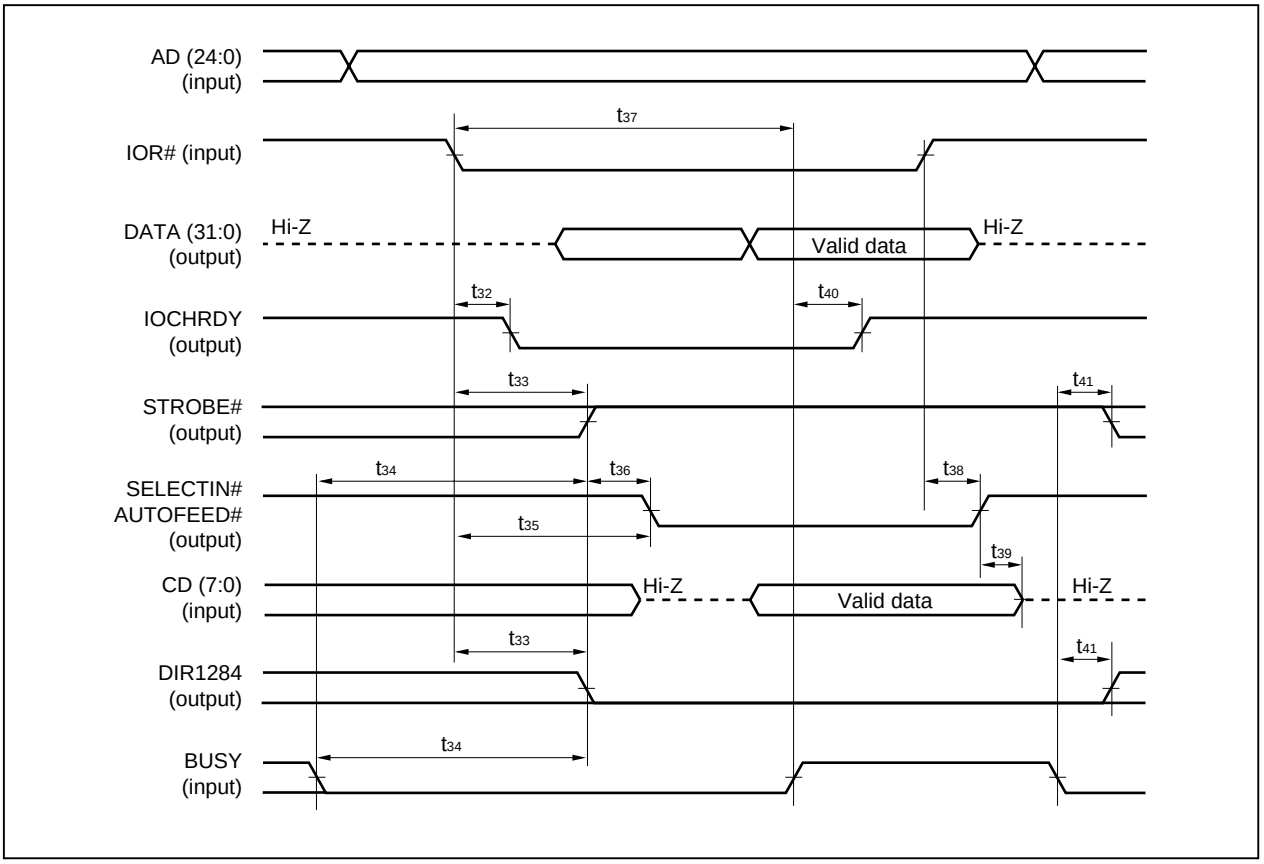
★**Remark** T: Parallel interface internal clock cycle (41.6 ns (MIN.))



(f) Read timing in EPP1.9 mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
IOCHRDY setup time	t_{32}			3 T	ns
STROBE# setup time, DIR1284 cancellation time (from IOR# ↓)	t_{33}			5 T	ns
STROBE# setup time, DIR1284 cancellation time (from BUSY ↓)	t_{34}			4 T	ns
SELECTIN#, AUTOFEED# setup time (from IOR# ↓)	t_{35}			6 T	ns
★ SELECTIN#, AUTOFEED# setup time (from DIR1284 ↑)	t_{36}		30		ns
Timeout generation time	t_{37}			10	μs
SELECTIN#, AUTOFEED# cancellation time (from IOR# ↑)	t_{38}			3 T	ns
CD (7:0) hold time	t_{39}		0		ns
IOCHRDY cancellation time	t_{40}			3 T	ns
STROBE# cancellation time, DIR1284 setup time	t_{41}		1 T		ns

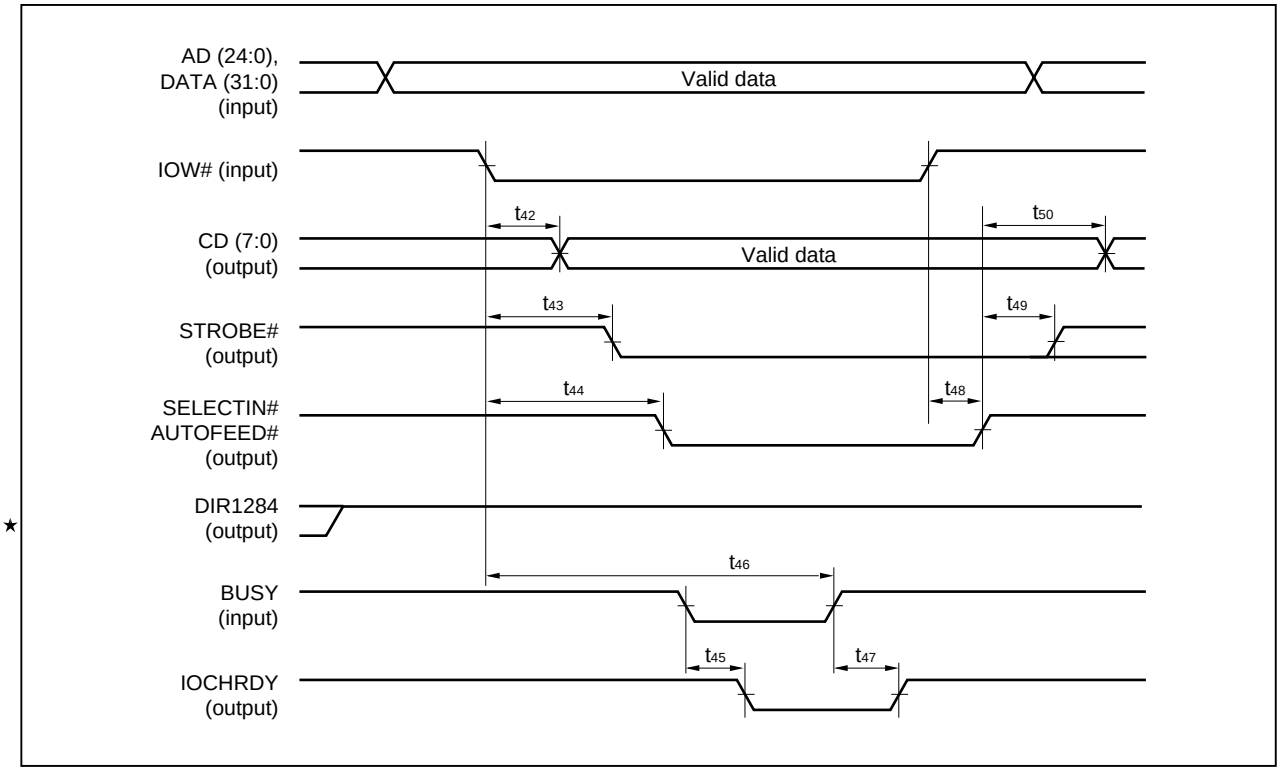
★ **Remark** T: Parallel interface internal clock cycle (41.6 ns (MIN.))



(g) Write timing in EPP1.7 mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CD (7:0) output delay time	t_{42}			30	ns
STROBE# setup time	t_{43}			3 T	ns
SELECTIN#, AUTOFEED# setup time	t_{44}			4 T	ns
IOCHRDY setup time	t_{45}			3 T	ns
Timeout generation time	t_{46}			10	μs
IOCHRDY cancellation time	t_{47}			3 T	ns
SELECTIN#, AUTOFEED# cancellation time	t_{48}			3 T	ns
STROBE# cancellation time	t_{49}		1 T		ns
★ CD (7:0) hold time	t_{50}		30		ns

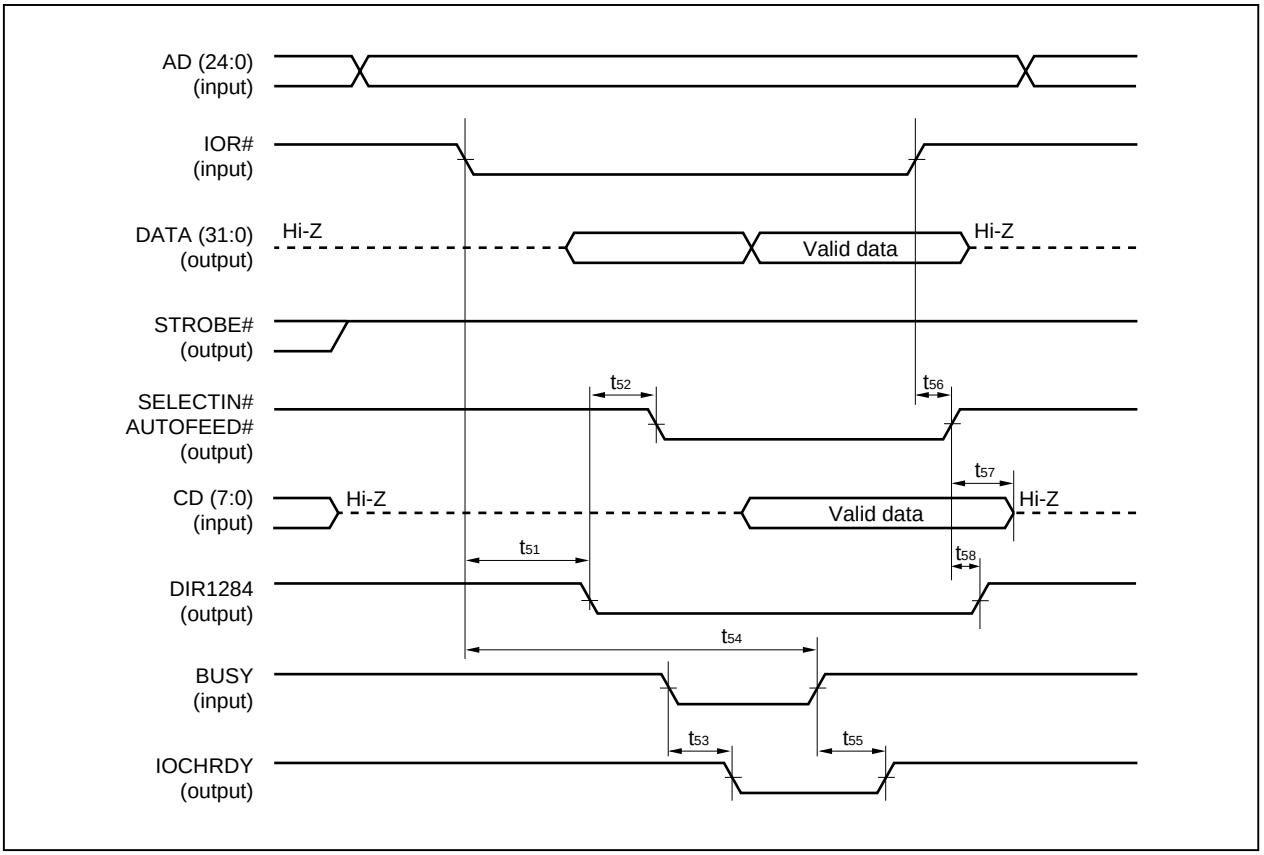
★**Remark** T: Parallel interface internal clock cycle (41.6 ns (MIN.))



(h) Read timing in EPP1.7 mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
DIR1284 setup time	t_{51}			3 T	ns
★ SELECTIN#, AUTOFEED# setup time	t_{52}		30		ns
IOCHRDY setup time	t_{53}			3 T	ns
Timeout generation time	t_{54}			10	μs
IOCHRDY cancellation time	t_{55}			3 T	ns
SELECTIN#, AUTOFEED# cancellation time	t_{56}			3 T	ns
CD (7:0) hold time	t_{57}		0		ns
DIR1284 cancellation time	t_{58}		1 T		ns

★ **Remark** T: Parallel interface internal clock cycle (41.6 ns (MIN.))

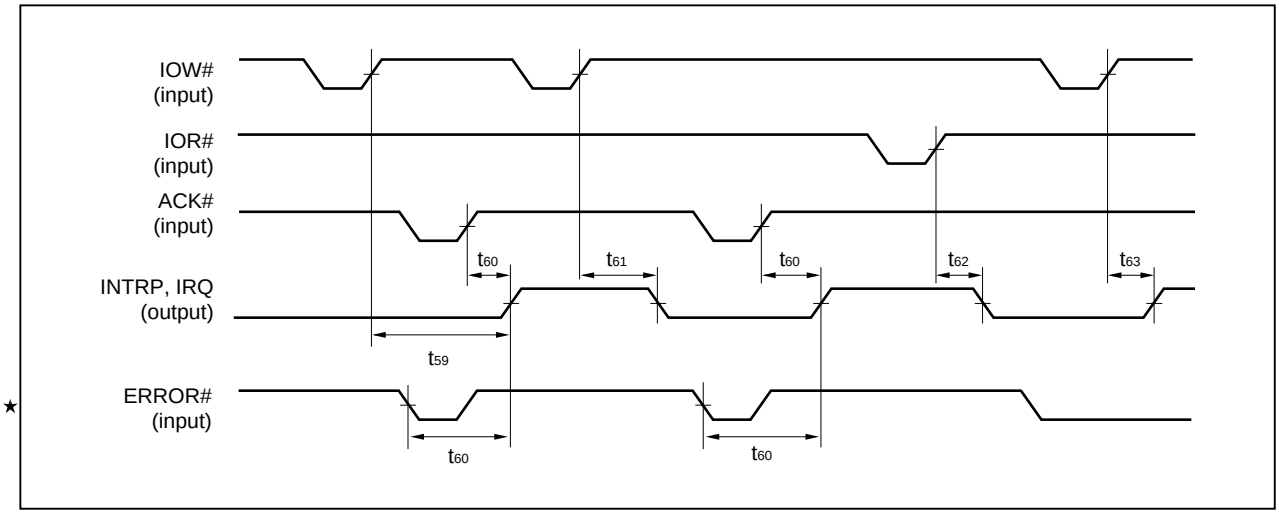


(i) Interrupt request timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Interrupt request setup time	t_{59}		4 T		ns
Interrupt request generation time (from ACK#↑, ERROR# ↓)	t_{60}			3 T	ns
Interrupt request cancellation time (from IOW# ↑)	t_{61}			5 T	ns
★ Interrupt request cancellation time[Note] (from IOR# ↑)	t_{62}			3 T	ns
Interrupt request generation time (from IOW# ↑)	t_{63}			5 T	ns

★ **Note** When bit 7 of the CNFGA register = 0

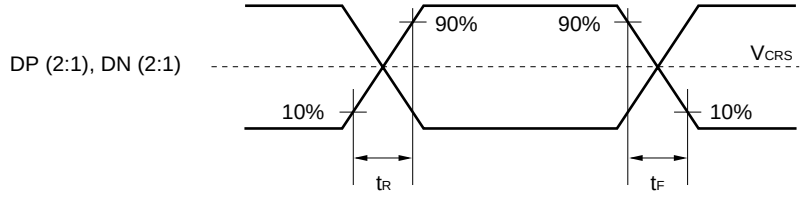
Remark T: Parallel interface internal clock cycle (41.6 ns (MIN.))



(11) USB interface

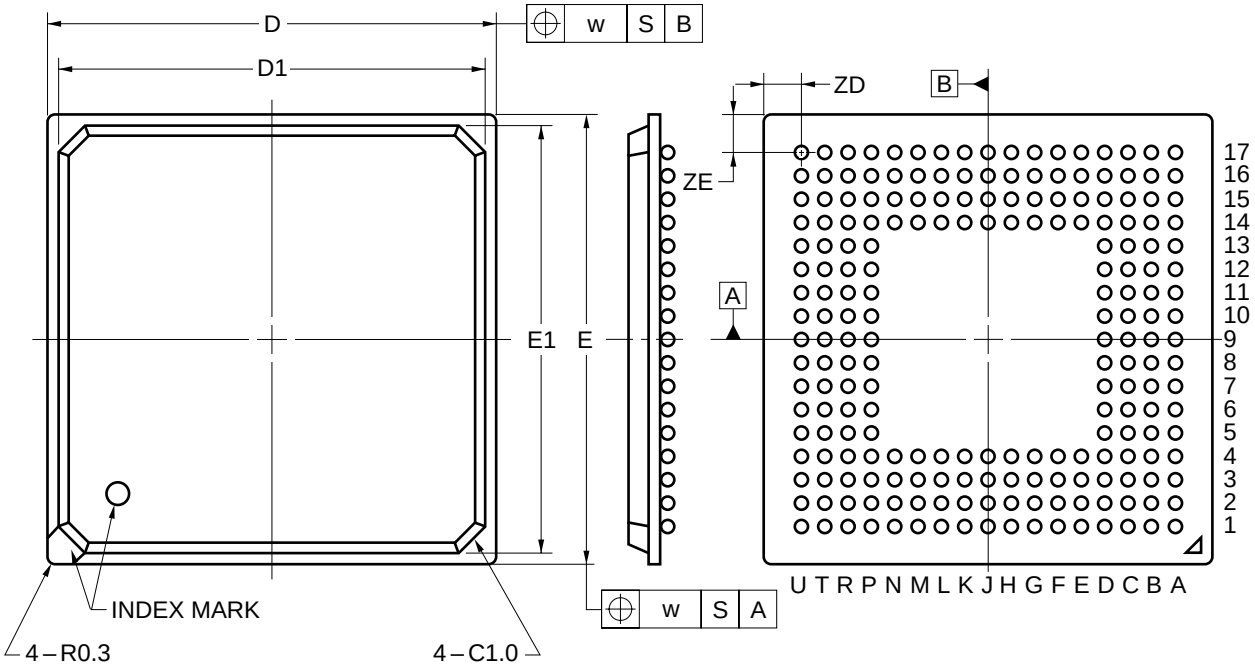
Applicable to the DP (2:1) and DN (2:1) pins. Refer to the USB specification, revision 1.0, for details.

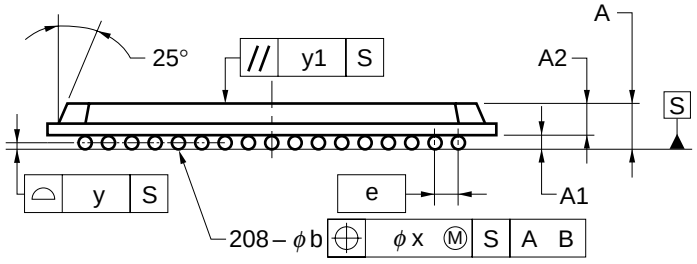
Parameter		Symbol	Conditions	MIN.	MAX.	Unit
Full-speed mode	Rise time	t_R	C_L = 50 pF	4	20	ns
	Fall time	t_F	C_L = 50 pF	4	20	ns
	t_R, t_F matching	t_{RFM}	t_R/t_F	90	110	%
	Differential output signal crossover point	V_{CRS}		1.3	2.0	V
Low-speed mode	Rise time	t_R	C_L = 50 pF	75		ns
			C_L = 350 pF		300	ns
	Fall time	t_F	C_L = 50 pF	75		ns
			C_L = 350 pF		300	ns
	t_R, t_F matching	t_{RFM}	t_R/t_F	80	120	%
	Differential output signal crossover point	V_{CRS}		1.3	2.0	V
Impedance		Imp.		28	43	Ω



3. PACKAGE DRAWING

208-PIN PLASTIC FBGA (15x15) OUTLINE DRAWINGS





ITEM	MILLIMETERS
D	15.00±0.10
D1	14.4
E	15.00±0.10
E1	14.4
w	0.20
e	0.80
A	1.51±0.15
A1	0.35±0.10
A2	1.16
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.1
ZE	1.1

P208S1-80-2C

★ 4. RECOMMENDED SOLDERING CONDITIONS

The μPD31172 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	VP15-107-3
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
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Tel: 01908-691-133
Fax: 01908-670-290

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Tel: 02-66 75 41
Fax: 02-66 75 42 99

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Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

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Related Documents: VRC4172 User's Manual (U14386E)
VR4121 User's Manual (U13569E)
VR4121 Data Sheet (U14691E)

Reference Materials: Electrical Characteristics for Microcomputer (IEI-601)

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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